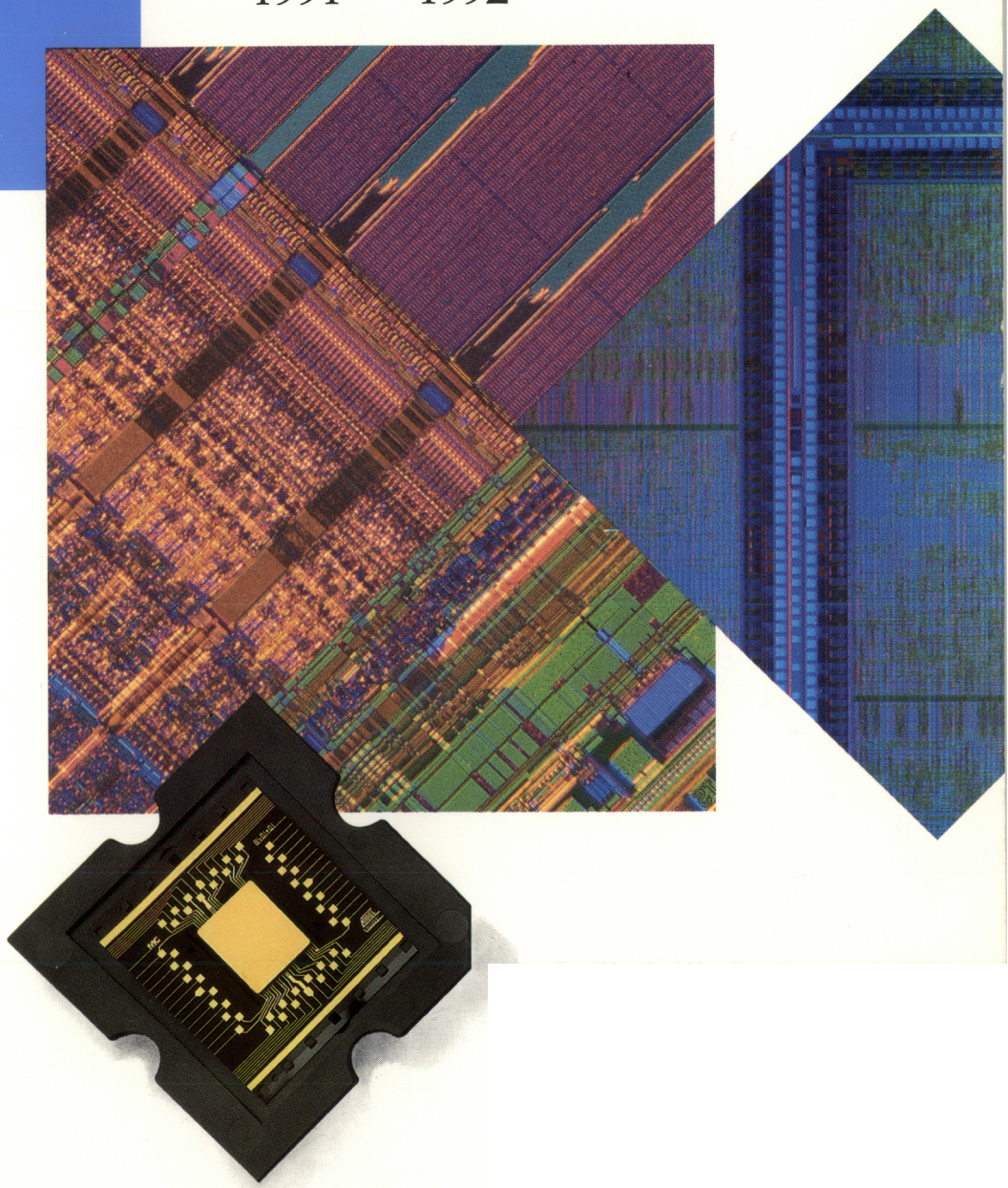
ATMEL

CMOS
Data Book
1991 • 1992



Atmel Corporation
CMOS Integrated Circuit
Data Book
1991 •1992

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Atmel Overview

Atmel Corporation designs, manufactures and markets high quality and high performance CMOS memory, logic and analog integrated circuits. Founded in 1984, the Company serves the manufacturers of computation, communications and instrumentation equipment in military and commercial environments.

Atmel's broad line of products provide customers with a variety of solutions to their memory applications. Atmel can offer high-density, high-speed memory and logic *standard* products as well as custom gate arrays.

Atmel guarantees quality and reliability by fabricating all products— no matter what their intended application— to meet or exceed the specifications of Military Standard 883.

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We thank you for considering Atmel semiconductors.

On The Cover...

The broad range of Atmel's technological prowess is exemplified by the three microphotographs on the cover of this data book. The ATV5000 (center photo) is Atmel's leading field programmable logic device that offers 5000 gates of user programmable logic. The ATL series gate array (to the right) shows Atmel's capability in designing large complex logic functions. Atmel has married these technologies together through Computer Aided Design methodologies to allow the system designer to prove designs quickly with field programmable logic and easily transition to mask programmable ASIC devices for volume production.

The AT28C010 (lower photo) offers one-million bits of electrically reprogrammable memory (EEPROM) on a single chip. The device is shown mounted on a Tape Automated Bonding (TAB) lead frame that offers the smallest footprint available. Atmel is a leader in the production of TAB devices for use in multi-chip modules or wherever small footprints are needed.

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CMOS E²PROM Product Selection Guide

AT24C01								see page 2–3
Organization: 128 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	Package S	Temperature Range	Option	Power Supply	I_{CC} (mA)	fMAX (kHz)
	10	•	•	C	-2.7, -2.5	10%	2.0	100
	10	•	•	I	-2.7, -2.5	10%	2.0	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)

CMOS E²PROM Product Selection Guide

AT24C02

see page 2–9

Organization: 256 x 8 No. of Pins: DIP 8, SOIC 8, 14	Speed (ms)	Package P	Package S1	Package S2	Temp. Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7, -2.5	10%	2.0	100
	10	•	•	•	I	-2.7, -2.5	10%	2.0	100

AT24C04

see page 2–9

Organization: 512 x 8 No. of Pins: DIP 8, SOIC 8, 14	Speed (ms)	Package P	Package S1	Package S2	Temp. Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7, -2.5	10%	2.0	100
	10	•	•	•	I	-2.7, -2.5	10%	2.0	100

AT24C08

see page 2–9

Organization: 1024 x 8 No. of Pins: DIP 8, SOIC 8, 14	Speed (ms)	Package P	Package S1	Package S2	Temp. Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7, -2.5	10%	2.0	100
	10	•	•	•	I	-2.7, -2.5	10%	2.0	100

AT24C16

see page 2–9

Organization: 2048 x 8 No. of Pins: DIP 8, SOIC 8, 14	Speed (ms)	Package P	Package S1	Package S2	Temp. Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7, -2.5	10%	2.0	100
	10	•	•	•	I	-2.7, -2.5	10%	2.0	100

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	14S, 14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)

CMOS E²PROM Product Selection Guide

AT93C46

see page 2-23

Organization: 64 x 16 or 128 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	S1	S2	Temperature Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7, R	10%	3.0	1000
	10	•	•	•	I	-2.7, R	10%	3.0	1000

AT93C56

see page 2-23

Organization: 128 x 16 or 256 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	S1	S2	Temp. Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7	10%	3.0	1000
	10	•	•	•	I	-2.7	10%	3.0	1000

AT93C66

see page 2-23

Organization: 256 x 16 or 512 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	S1	S2	Temp. Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	•	C	-2.7	10%	3.0	1000
	10	•	•	•	I	-2.7	10%	3.0	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S1	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
S2	8S2, 8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
R	Rotated Pinout

CMOS E²PROM Product Selection Guide

AT59C11

see page 2–31

Organization: 64 x 16 or 128 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	Package S	Temperature Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	C	-2.7	10%	3.0	1000
	10	•	•	I	-2.7	10%	3.0	1000

AT59C12

see page 2–31

Organization: 128 x 16 or 256 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	Package S	Temperature Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	C	-2.7	10%	3.0	1000
	10	•	•	I	-2.7	10%	3.0	1000

AT59C13

see page 2–31

Organization: 256 x 16 or 512 x 8 No. of Pins: DIP 8, SOIC 8	Speed (ms)	Package P	Package S	Temperature Range	Option	Power Supply	Icc (mA)	fMAX (kHz)
	10	•	•	C	-2.7	10%	3.0	1000
	10	•	•	I	-2.7	10%	3.0	1000

Package Type	
P	8P3, 8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S	8S1, 8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)

CMOS E²PROM Product Selection Guide

AT28C04

see page 2–39

Organization: 512 x 8
No. of Pins: DIP 24, LCC 32

Speed (ns)	Package D	L	P	W	Temperature Range	Option	Icc (mA) Active	Standby
150	•	•	•		C	E, F	30	0.1
150	•	•	•		I	E, F	45	0.1
150	•	•			M	E, F	45	0.1
150	•	•			M/883	E, F	45	0.1
200	•	•	•		C	E, F	30	0.1
200	•	•	•		I	E, F	45	0.1
200	•	•			M	E, F	45	0.1
200	•	•			M/883	E, F	45	0.1
250	•	•	•	•	C	E, F	30	0.1
250	•	•	•		I	E, F	45	0.1
250	•	•			M	E, F	45	0.1
250	•	•			M/883	E, F	45	0.1
300	•	•			M/883	E, F	45	0.1
350	•	•			M/883	E, F	45	0.1
450	•	•			M/883	E, F	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

CMOS E²PROM Product Selection Guide

AT28C16

see page 2–49

Organization: 2K x 8
No. of Pins: DIP 24, LCC 32

Speed (ns)	Package D	J	L	P	S	W	Temp. Range	Option	Icc (mA) Active	Standby
150	•	•	•	•	•		C	E, F	30	0.1
150	•	•	•	•	•		I	E, F	45	0.1
150	•		•				M	E, F	45	0.1
150	•		•				M/883	E, F	45	0.1
200	•	•	•	•	•		C	E, F	30	0.1
200	•	•	•	•	•		I	E, F	45	0.1
200	•		•				M	E, F	45	0.1
200	•		•				M/883	E, F	45	0.1
250	•	•	•	•	•	•	C	E, F	30	0.1
250	•	•	•	•	•		I	E, F	45	0.1
250	•		•				M	E, F	45	0.1
250	•		•				M/883	E, F	45	0.1
300	•		•				M/883	E, F	45	0.1
350	•		•				M/883	E, F	45	0.1
450	•		•				M/883	E, F	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

CMOS E²PROM Product Selection Guide

AT28HC16

see page 2–59

Organization: 2K x 8 Number of Pins: DIP 24	Speed (ns)	Package D3	Package D6	Package P3	Package P6	Temperature Range	Icc (mA) Active	Icc (mA) Standby
	45	•	•	•	•	C	80	60
	45	•	•	•	•	I	80	60
	55	•	•	•	•	C	80	60
	55	•	•	•	•	I	80	60
	55	•	•			M	80	60
	55	•	•			MB	80	60
	70	•	•	•	•	C	80	60
	70	•	•	•	•	I	80	60
	70	•	•			M	80	60
	70	•	•			MB	80	60
	90	•	•	•	•	C	80	60
	90	•	•	•	•	I	80	60
	90	•	•			M	80	60
	90	•	•			MB	80	60

Contact Factory: Not recommended for new designs.

Package Type	
D3	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
D6	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P3	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
P6	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB	Military (-55°C to 125°C) with Burn-In

CMOS E²PROM Product Selection Guide

AT28HC16L

see page 2–59

Organization: 2K x 8
Number of Pins: DIP 24

Speed (ns)	Package D3	D6	P3	P6	W	Temperature Range	Icc (mA) Active	Standby
55	•	•	•	•		C	80	0.5
55	•	•	•	•		I	80	0.5
55	•	•				M	80	0.5
55	•	•				MB	80	0.5
70	•	•	•	•		C	80	0.5
70	•	•	•	•		I	80	0.5
70	•	•				M	80	0.5
70	•	•				MB	80	0.5
90	•	•	•	•	•	C	80	0.5
90	•	•	•	•		I	80	0.5
90	•	•				M	80	0.5
90	•	•				MB	80	0.5

Contact Factory: Not recommended for new designs.

Package Type	
D3	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
D6	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P3	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
P6	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28C17

see page 2–71

Organization: 2K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	L	P	S	W	Temp. Range	Option	Icc (mA) Active	Standby
	150	•	•	•	•	•		C	E, F	30	0.1
	150	•	•	•	•	•		I	E, F	45	0.1
	150	•		•				M	E, F	45	0.1
	150	•		•				M/883	E, F	45	0.1
	200	•	•	•	•	•		C	E, F	30	0.1
	200	•	•	•	•	•		I	E, F	45	0.1
	200	•		•				M	E, F	45	0.1
	200	•		•				M/883	E, F	45	0.1
	250	•	•	•	•	•	•	C	E, F	30	0.1
	250	•	•	•	•	•		I	E, F	45	0.1
	250	•		•				M	E, F	45	0.1
	250	•		•				M/883	E, F	45	0.1
	300	•		•				M/883	E, F	45	0.1
	350	•		•				M/883	E, F	45	0.1
	450	•		•				M/883	E, F	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	24S, 24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

CMOS E²PROM Product Selection Guide

AT28C64

see page 2–81

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	F	J	K	L	P	S	W	Temp. Range	Option	Icc (mA) Active	Standby
	150	•	•	•		•	•	•		C	E, F	30	0.1
	150	•	•	•		•	•	•		I	E, F	45	0.1
	150	•	•			•				M	E, F	45	0.1
	150	•	•			•				M/883	E, F	45	0.1
	200	•	•	•		•	•	•		C	E, F	30	0.1
	200	•	•	•		•	•	•		I	E, F	45	0.1
	200	•	•			•				M	E, F	45	0.1
	200	•	•			•				M/883	E, F	45	0.1
	250	•	•	•		•	•	•	•	C	E, F	30	0.1
	250	•	•	•		•	•	•		I	E, F	45	0.1
	250	•	•			•				M	E, F	45	0.1
	250	•	•			•				M/883	E, F	45	0.1
	300	•	•			•				M/883	E, F	45	0.1
	350	•	•			•				M/883	E, F	45	0.1
	450	•	•			•				M/883	E, F	45	0.1
SMD Number for AT28C64													
5962-87514 17	150	•			•	•				M/883		45	0.1
5962-87514 16	200	•			•	•				M/883		45	0.1
5962-87514 15	250	•	•		•	•				M/883		45	0.1
5962-87514 14	300	•			•	•				M/883		45	0.1
5962-87514 13	350	•	•		•	•				M/883		45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

CMOS E²PROM Product Selection Guide

AT28C64X

see page 2–81

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	F	J	K	L	P	S	Temperature Range	Icc (mA) Active	Standby
	150	•	•	•		•	•	•	C	30	0.1
	150	•	•	•		•	•	•	I	45	0.1
	150	•	•			•			M	45	0.1
	150	•	•			•			M/883	45	0.1
	200	•	•	•		•	•	•	C	30	0.1
	200	•	•	•		•	•	•	I	45	0.1
	200	•	•			•			M	45	0.1
	200	•	•			•			M/883	45	0.1
	250	•	•	•		•	•	•	C	30	0.1
	250	•	•	•		•	•	•	I	45	0.1
	250	•	•			•			M	45	0.1
	250	•	•			•			M/883	45	0.1
	300	•	•			•			M/883	45	0.1
	350	•	•			•			M/883	45	0.1
	450	•	•			•			M/883	45	0.1
SMD Number for AT28C64X											
5962-87514 22	150	•			•	•			M/883	45	0.1
5962-87514 21	200	•			•	•			M/883	45	0.1
5962-87514 20	250	•	•		•	•			M/883	45	0.1
5962-87514 19	300	•			•	•			M/883	45	0.1
5962-87514 18	350	•			•	•			M/883	45	0.1

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
S	28S, 28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28HC64

see page 2–81

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	L	P	Temperature Range	Option	Icc (mA) Active	Standby
	55	•	•	•	•	C	E	80	60
	55	•	•	•	•	I	E	80	60
	70	•	•	•	•	C	E	80	60
	70	•	•	•	•	I	E	80	60
	70	•		•		M	E	80	60
	70	•		•		M/883	E	80	60
	90	•	•	•	•	C	E	80	60
	90	•	•	•	•	I	E	80	60
	90	•		•		M	E	80	60
	90	•		•		M/883	E	80	60
	120	•	•	•	•	C	E	80	60
	120	•	•	•	•	I	E	80	60
	120	•		•		M	E	80	60
	120	•		•		M/883	E	80	60

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28HC64L

see page 2–93

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	K	L	P	W	Temp. Range	Option	Icc (mA) Active	Standby
	70	•	•		•	•		C	E	80	0.1
	70	•	•		•	•		I	E	80	0.1
	90	•	•		•	•		C	E	80	0.1
	90	•	•		•	•		I	E	80	0.1
	90	•			•			M	E	80	0.2
	90	•			•			M/883	E	80	0.2
	120	•	•		•	•	•	C	E	80	0.1
	120	•	•		•	•		I	E	80	0.1
	120	•			•			M	E	80	0.2
	120	•			•			M/883	E	80	0.2
SMD Number for AT28HC64L											
5962-87514 12	70	•		•	•			M/883		80	0.2
5962-87514 11	90	•		•	•			M/883		80	0.2
5962-87514 10	120	•		•	•			M/883		80	0.2

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28PC64

see page 2–105

Organization: 8K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	K	L	P	W	Temp. Range	Option	Icc (mA) Active	Standby
	150	•	•		•	•		C	E	80	0.1
	150	•	•		•	•		I	E	80	0.1
	150	•			•			M	E	80	0.2
	150	•			•			M/883	E	80	0.2
	200	•	•		•	•		C	E	80	0.1
	200	•	•		•	•		I	E	80	0.1
	200		•		•			M	E	80	0.2
	200	•			•			M/883	E	80	0.2
	250	•	•		•	•	•	C	E	80	0.1
	250	•	•		•	•		I	E	80	0.1
	250	•			•			M	E	80	0.2
	250	•			•			M/883	E	80	0.2
	300	•			•			M/883	E	80	0.2
	350	•			•			M/883	E	80	0.2
SMD Number for AT28PC64											
5962-87514 09	200	•		•	•			M/883		80	0.2
5962-87514 08	250	•		•	•			M/883		80	0.2
5962-87514 07	300	•		•	•			M/883		80	0.2
5962-87514 06	350	•		•	•			M/883		80	0.2

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
K	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28C256

see page 2–117

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	F	J	L	P	U	W	Temp. Range	Option	Icc (mA) Active	Standby
	150	•	•	•	•	•	•		C	E, F	80	0.2
	150	•	•	•	•	•	•		I	E, F	80	0.2
	150	•	•		•		•		M	E, F	80	0.3
	150	•	•		•		•		M/883	E, F	80	0.3
	200	•	•	•	•	•	•		C	E, F	80	0.2
	200	•	•	•	•	•	•		I	E, F	80	0.2
	200	•	•		•		•		M	E, F	80	0.3
	200	•	•		•		•		M/883	E, F	80	0.3
	250	•	•	•	•	•	•	•	C	E, F	80	0.2
	250	•	•	•	•	•	•		I	E, F	80	0.2
	250	•	•		•		•		M	E, F	80	0.3
	250	•	•		•		•		M/883	E, F	80	0.3
	300	•	•		•		•		M/883	E, F	80	0.3
	350	•	•		•		•		M/883	E, F	80	0.3
SMD Number for AT28C256												
5962-88525 06	150	•	•		•		•		M/883		80	0.35
5962-88525 07	150	•	•		•		•		M/883	F	80	0.35
5962-88525 04	200	•	•		•		•		M/883		80	0.35
5962-88525 03	250	•	•		•		•		M/883		80	0.35
5962-88525 05	250	•	•		•		•		M/883	E	80	0.35
5962-88525 02	300	•	•		•		•		M/883		80	0.35
5962-88525 01	350	•	•		•		•		M/883		80	0.35

	Package Type
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
	Temperature Range
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3ms

CMOS E²PROM Product Selection Guide

AT28HC256

see page 2–129

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	F	J	L	P	U	Temp. Range	Option	Icc (mA) Active	Standby
	70	•		•	•	•		C	E, F	80	60
	70	•		•	•	•		I	E, F	80	60
	90	•	•	•	•	•	•	C	E, F	80	60
	90	•	•	•	•	•	•	I	E, F	80	60
	90	•	•		•		•	M	E, F	80	60
	90	•	•		•		•	M/883	E, F	80	60
	120	•	•	•	•	•	•	C	E, F	80	60
	120	•	•	•	•	•	•	I	E, F	80	60
	120	•	•		•		•	M	E, F	80	60
	120	•	•		•		•	M/883	E, F	80	60
SMD Number for AT28HC256											
5962-88634 03	90	•	•		•		•	M/883		80	60
5962-88634 04	90	•	•		•		•	M/883	F	80	60

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

CMOS E²PROM Product Selection Guide

AT28HC256L

see page 2–129

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	F	J	L	P	U	W	Temp. Range	Option	Icc (mA) Active	Standby
	90	•	•	•	•	•	•		C	E, F	80	0.3
	90	•	•	•	•	•	•		I	E, F	80	0.3
	120	•	•	•	•	•	•	•	C	E, F	80	0.3
	120	•	•	•	•	•	•		I	E, F	80	0.3
	120	•	•		•		•		M	E, F	80	0.3
	120	•	•		•		•		M/883	E, F	80	0.3
SMD Number for AT28HC256L												
5962-88634 01	120	•	•		•		•		M/883		80	0.3
5962-88634 02	120	•	•		•		•		M/883	F	80	0.3

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
F	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E²PROM Product Selection Guide

AT28C1024

see page 2–143

Organization: 64K x 16 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package B	L	V	W	Temperature Range	Icc (mA) Active	Standby
	120	•	•			C	100	0.4
	120	•	•			I	100	0.4
	150	•	•	•		C	100	0.4
	150	•	•	•		I	100	0.4
	150	•	•	•		M	100	0.4
	150	•	•			M/883	100	0.4
	200	•	•	•		C	100	0.4
	200	•	•	•		I	100	0.4
	200	•	•	•		M	100	0.4
	200	•	•			M/883	100	0.4
	250	•	•	•	•	C	100	0.4
	250	•	•	•		I	100	0.4
	250	•	•	•		M	100	0.4
	250	•	•			M/883	100	0.4

Package Type	
B	40B, 40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
L	44L, 44 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
V	Tape Automated Bond (TAB) Carrier
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28C010

see page 2–153

Organization: 128K x 8 No. of Pins: DIP 32, LCC 44	Speed (ns)	Package B	F	L	U	V	W	Temp. Range	Option	Icc (mA) Active	Standby
	120	•	•	•	•			C	E	80	0.3
	120	•	•	•	•			I	E	80	0.3
	120	•	•	•	•			M	E	80	0.3
	120	•	•	•	•			M/883	E	80	0.3
	150	•	•	•	•	•		C	E	80	0.3
	150	•	•	•	•	•		I	E	80	0.3
	150	•	•	•	•	•		M	E	80	0.3
	150	•	•	•	•			M/883	E	80	0.3
	200	•	•	•	•	•		C	E	80	0.3
	200	•	•	•	•	•		I	E	80	0.3
	200	•	•	•	•	•		M	E	80	0.3
	200	•	•	•	•			M/883	E	80	0.3
	250	•	•	•	•	•	•	C	E	80	0.3
	250	•	•	•	•	•		I	E	80	0.3
	250	•	•	•	•	•		M	E	80	0.3
	250	•	•	•	•			M/883	E	80	0.3
SMD Number for AT28C010											
5962-38267 07	120	•	•	•				M/883		80	0.3
5962-38267 05	150	•	•	•				M/883		80	0.3
5962-38267 03	200	•	•	•				M/883		80	0.3
5962-38267 01	250	•	•	•				M/883		80	0.3

Package Type	
B	32B, 32 Lead, 0.600" Wide Ceramic Side Braze Dual Inline (Side Braze)
F	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
L	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
U	30U, 30 Pin, Ceramic Pin Grid Array (PGA)
V	Tape Automated Bond (TAB) Carrier
W	Die
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

CMOS E^{2}PROM Product Selection Guide

AT28MC010

see page 2–163

Organization: 128K x 8
Number of Pins: DIP 32

Speed (ns)	Package M	Temperature Range	Icc (mA) Active	Icc (mA) Standby
120	•	C	100	0.5
120	•	I	100	0.5
120	•	M	100	0.5
120	•	MB	100	0.5
150	•	C	100	0.5
150	•	I	100	0.5
150	•	M	100	0.5
150	•	MB	100	0.5
200	•	C	100	0.5
200	•	I	100	0.5
200	•	M	100	0.5
200	•	MB	100	0.5
250	•	C	100	0.5
250	•	I	100	0.5
250	•	M	100	0.5
250	•	MB	100	0.5

Package Type	
M	32M1, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible LCC Multi-Chip Module (MCM)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB	MIL-STD-883C, Class B Components (-55°C to 125°C)

CMOS E²PROM Product Selection Guide

AT28MC020

see page 2–173

Organization: 256K x 8 Number of Pins: DIP 32	Speed (ns)	Package M	Package Z	Temperature Range	Icc (mA) Active	Icc (mA) Standby
	150	•	•	C	80	0.5
	150	•	•	I	80	0.5
	150	•	•	M	80	0.5
	150	•	•	MB	80	0.5
	200	•	•	C	80	0.5
	200	•	•	I	80	0.5
	200	•	•	M	80	0.5
	200	•	•	MB	80	0.5
	250	•	•	C	80	0.5
	250	•	•	I	80	0.5
	250	•	•	M	80	0.5
	250	•	•	MB	80	0.5

Package Type	
M	32M2, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
Z	32Z, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB	MIL-STD-883C, Class B Components (-55°C to 125°C)

AT28MC040

see page 2–183

Organization: 512K x 8
Number of Pins: DIP 32

Speed (ns)	Package M	Package Z	Temperature Range	Icc (mA) Active	Icc (mA) Standby
150	•	•	C	80	0.5
150	•	•	I	80	0.5
150	•	•	M	80	0.5
150	•	•	MB	80	0.5
200	•	•	C	80	0.5
200	•	•	I	80	0.5
200	•	•	M	80	0.5
200	•	•	MB	80	0.5
250	•	•	C	80	0.5
250	•	•	I	80	0.5
250	•	•	M	80	0.5
250	•	•	MB	80	0.5

Package Type	
M	32M2, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
Z	32Z, 32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
MB	MIL-STD-883C, Class B Components (-55°C to 125°C)

CMOS PEROM Product Selection Guide

AT29C256

see page 3–3

Organization: 32K x 8
No. of Pins: DIP 28, LCC 32

Speed (ns)	Package D	Package J	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
120	•	•	•	•	C	10%	80	0.3
120	•	•	•	•	I	10%	80	0.3
120	•		•		M	10%	80	0.3
120	•		•		M/883	10%	80	0.3
150	•	•	•	•	C	10%	80	0.3
150	•	•	•	•	I	10%	80	0.3
150	•		•		M	10%	80	0.3
150	•		•		M/883	10%	80	0.3
200	•	•	•	•	C	10%	80	0.3
200	•	•	•	•	I	10%	80	0.3
200	•		•		M	10%	80	0.3
200	•		•		M/883	10%	80	0.3
250	•	•	•	•	C	10%	80	0.3
250	•	•	•	•	I	10%	80	0.3
250	•		•		M	10%	80	0.3
250	•		•		M/883	10%	80	0.3

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PEROM Product Selection Guide

AT29C257

see page 3–17

Organization: 32K x 8
No. of Pins: DIP 32, LCC 32

Speed (ns)	Package D	J	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
120	•	•	•	•	C	10%	80	0.3
120	•	•	•	•	I	10%	80	0.3
120	•		•		M	10%	80	0.3
120	•		•		M/883	10%	80	0.3
150	•	•	•	•	C	10%	80	0.3
150	•	•	•	•	I	10%	80	0.3
150	•		•		M	10%	80	0.3
150	•		•		M/883	10%	80	0.3
200	•	•	•	•	C	10%	80	0.3
200	•	•	•	•	I	10%	80	0.3
200	•		•		M	10%	80	0.3
200	•		•		M/883	10%	80	0.3
250	•	•	•	•	C	10%	80	0.3
250	•	•	•	•	I	10%	80	0.3
250	•		•		M	10%	80	0.3
250	•		•		M/883	10%	80	0.3

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PEROM Product Selection Guide

AT29C010

see page 3–31

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32

Speed (ns)	Package D	Package J	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
120	•	•	•	•	C	10%	50	0.1
120	•	•	•	•	C	10%	50	0.3
150	•	•	•	•	C	10%	50	0.1
150	•	•	•	•	I	10%	50	0.3
150	•		•		M	10%	50	0.3
150	•		•		M/883	10%	50	0.3
200	•	•	•	•	C	10%	50	0.1
200	•	•	•	•	I	10%	50	0.3
200	•		•		M	10%	50	0.3
200	•		•		M/883	10%	50	0.3
250	•	•	•	•	C	10%	50	0.1
250	•	•	•	•	I	10%	50	0.3
250	•		•		M	10%	50	0.3
250	•		•		M/883	10%	50	0.3

Package Type	
D	32D6, 32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C256 –Not recommended for new designs. Use AT27C256R.

AT27C256R

see page 4–3

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	K	L	P	R	Temp. Range	Power Supply	Icc (mA) Active	Standby
	90	•	•	•	•	•	•	C	10%	20	0.1
	90	•	•	•	•	•	•	I	10%	25	0.2
	120	•	•	•	•	•	•	C	10%	20	0.1
	120	•	•	•	•	•	•	I	10%	25	0.2
	120	•		•	•			M	10%	25	0.2
	120	•		•	•			M/883	10%	25	0.2
	150	•	•	•	•	•	•	C	10%	20	0.1
	150	•	•	•	•	•	•	I	10%	25	0.2
	150	•		•	•			M	10%	25	0.2
	150	•		•	•			M/883	10%	25	0.2
	170	•	•	•	•	•	•	C	10%	20	0.1
	170	•	•	•	•	•	•	I	10%	25	0.2
	170	•		•	•			M	10%	25	0.2
	170	•		•	•			M/883	10%	25	0.2
	200	•	•	•	•	•	•	C	10%	20	0.1
	200	•	•	•	•	•	•	I	10%	25	0.2
	200	•		•	•			M	10%	25	0.2
	200	•		•	•			M/883	10%	25	0.2
	250	•	•	•	•	•	•	C	10%	20	0.1
	250	•	•	•	•	•	•	I	10%	25	0.2
	250	•		•	•			M	10%	25	0.2
	250	•		•	•			M/883	10%	25	0.2
SMD Number for part AT27C256R											
5962-86063 05	150	•		•	•			M/883	10%	25	0.2
5962-86063 04	170	•		•	•			M/883	10%	25	0.2
5962-86063 01	200	•		•	•			M/883	10%	25	0.2
5962-86063 02	250	•		•	•			M/883	10%	25	0.2
5962-86063 03	300	•		•	•			M/883	10%	25	0.2

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC256/L –Not recommended for new designs. Use AT27HC256R/RL.

AT27HC256R

see page 4–11

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	55	•		•	•		C	10%	50	30
	55	•		•	•		I	10%	55	35
	70	•	•	•	•	•	C	10%	50	30
	70	•	•	•	•	•	I	10%	55	35
	70	•		•	•		M	10%	55	35
	70	•		•	•		M/883	10%	55	35
	90	•	•	•	•	•	C	10%	50	30
	90	•	•	•	•	•	I	10%	55	35
	90	•		•	•		M	10%	55	35
	90	•		•	•		M/883	10%	55	35
	120	•	•	•	•	•	C	10%	50	30
	120	•	•	•	•	•	I	10%	55	35
	120	•		•	•		M	10%	55	35
	120	•		•	•		M/883	10%	55	35
SMD Number for AT27HC256R										
5962-86063 08	70	•			•		M/883	10%	55	35

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC256RL

see page 4–11

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	70	•		•	•		C	10%	50	0.1
	70	•		•	•		I	10%	55	0.2
	90	•	•	•	•	•	C	10%	50	0.1
	90	•	•	•	•	•	I	10%	55	0.2
	90	•		•	•		M	10%	55	0.2
	90	•		•	•		M/883	10%	55	0.2
	120	•	•	•	•	•	C	10%	50	0.1
	120	•	•	•	•	•	I	10%	55	0.2
	120	•		•	•		M	10%	55	0.2
	120	•		•	•		M/883	10%	55	0.2
SMD Number for AT27HC256RL										
5962-86063 07	90	•			•		M/883	10%	55	0.2
5962-86063 06	120	•			•		M/883	10%	55	0.2

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27LV256R

see page 4–21

Organization: 32K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package					Temperature Range	I_{CC} (mA)	
		D	J	L	P	R		Active	Standby
	270	•	•	•	•	•	C	8	0.1
	270	•		•			I	10	0.1

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C512 –Not recommended for new designs. Use AT27C512R.

AT27C512R

see page 4–29

Organization: 64K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package D	J	K	L	P	R	Temp. Range	Power Supply	Icc (mA) Active	Standby
	100	•	•	•	•	•	•	C	5%	20	0.1
	120	•	•	•	•	•	•	C	10%	20	0.1
	120	•	•	•	•	•	•	I	10%	25	0.2
	120	•		•	•			M	10%	25	0.2
	120	•		•	•			M/883	10%	25	0.2
	150	•	•	•	•	•	•	C	10%	20	0.1
	150	•	•	•	•	•	•	I	10%	25	0.2
	150	•		•	•			M	10%	25	0.2
	150	•		•	•			M/883	10%	25	0.2
	200	•	•	•	•	•	•	C	10%	20	0.1
	200	•	•	•	•	•	•	I	10%	25	0.2
	200	•		•	•			M	10%	25	0.2
	200	•		•	•			M/883	10%	25	0.2
	250	•	•	•	•	•	•	C	10%	20	0.1
	250	•	•	•	•	•	•	I	10%	25	0.2
	250	•		•	•			M	10%	25	0.2
	250	•		•	•			M/883	10%	25	0.2
SMD Number for AT27C512R											
5962-87648 04	120	•		•	•			M/883	10%	25	0.2
5962-87648 01	150	•		•	•			M/883	10%	25	0.2
5962-87648 02	200	•		•	•			M/883	10%	25	0.2
5962-87648 03	250	•		•	•			M/883	10%	25	0.2

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27LV512R

see page 4–37

Organization: 64K x 8 No. of Pins: DIP 28, LCC 32	Speed (ns)	Package					Temperature Range	I_{CC} (mA)	
		D	J	L	P	R		Active	Standby
	270	•	•	•	•	•	C	8	0.1
	270	•		•			I	10	0.1

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C010

see page 4–45

Organization: 128K x 8 No. of Pins: DIP 32, LCC 32	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	120	•	•	•	•	•	C	10%	40	0.1
	120	•	•	•	•	•	I	10%	50	0.1
	120	•		•	•		M	10%	50	0.1
	120	•		•	•		M/883	10%	50	0.1
	150	•	•	•	•	•	C	10%	40	0.1
	150	•	•	•	•	•	I	10%	50	0.1
	150	•		•	•		M	10%	50	0.1
	150	•		•	•		M/883	10%	50	0.1
	170	•	•	•	•	•	C	10%	40	0.1
	170	•	•	•	•	•	I	10%	50	0.1
	170	•		•	•		M	10%	50	0.1
	170	•		•	•		M/883	10%	50	0.1
	200	•	•	•	•	•	C	10%	40	0.1
	200	•	•	•	•	•	I	10%	50	0.1
	200	•		•	•		M	10%	50	0.1
	200	•		•	•		M/883	10%	50	0.1
	250	•	•	•	•	•	C	10%	40	0.1
	250	•	•	•	•	•	I	10%	50	0.1
	250	•		•	•		M	10%	50	0.1
	250	•		•	•		M/883	10%	50	0.1
SMD Number for AT27C010										
5962-89614 05	150	•			•		M/883	10%	50	0.1
5962-89614 04	170	•			•		M/883	10%	50	0.1
5962-89614 03	200	•			•		M/883	10%	50	0.1
5962-89614 02	250	•			•		M/883	10%	50	0.1
5962-89614 01	300	•			•		M/883	10%	50	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C010L

see page 4–45

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32

Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
120	•	•	•	•	•	C	10%	25	0.1
120	•	•	•	•	•	I	10%	30	0.1
120	•		•	•		M	10%	30	0.1
120	•		•	•		M/883	10%	30	0.1
150	•	•	•	•	•	C	10%	25	0.1
150	•	•	•	•	•	I	10%	30	0.1
150	•		•	•		M	10%	30	0.1
150	•		•	•		M/883	10%	30	0.1
170	•	•	•	•	•	C	10%	25	0.1
170	•	•	•	•	•	I	10%	30	0.1
170	•		•	•		M	10%	30	0.1
170	•		•	•		M/883	10%	30	0.1
200	•	•	•	•	•	C	10%	25	0.1
200	•	•	•	•	•	I	10%	30	0.1
200	•		•	•		M	10%	30	0.1
200	•		•	•		M/883	10%	30	0.1
250	•	•	•	•	•	C	10%	25	0.1
250	•	•	•	•	•	I	10%	30	0.1
250	•		•	•		M	10%	30	0.1
250	•		•	•		M/883	10%	30	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27CL010

see page 4–55

Organization: 128K x 8
No. of Pins: DIP 32, LCC 32

Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
150	•	•	•	•	•	C	10%	20	0.1
170	•	•	•	•	•	C	10%	20	0.1
170	•	•	•	•	•	I	10%	20	0.1
170	•		•	•		M	10%	20	0.1
170	•		•	•		M/883	10%	20	0.1
200	•	•	•	•	•	C	10%	20	0.1
200	•	•	•	•	•	I	10%	20	0.1
200	•		•	•		M	10%	20	0.1
200	•		•	•		M/883	10%	20	0.1
250	•	•	•	•	•	C	10%	20	0.1
250	•	•	•	•	•	I	10%	20	0.1
250	•		•	•		M	10%	20	0.1
250	•		•	•		M/883	10%	20	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27LV010

see page 4–63

Organization: 128K x 8 No. of Pins: DIP 32, LCC 32	Speed (ns)	Package D	J	L	P	Temperature Range	Icc (mA) Active	Standby
	270	•	•	•	•	C	8	0.1
	270	•		•		I	10	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	32J, 32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPROM Product Selection Guide

AT27C1024

see page 4–71

Organization: 64K x 16 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	120	•		•	•		C	5%	50	0.1
	150	•	•	•	•	•	C	10%	50	0.1
	150	•	•	•	•	•	I	10%	60	0.1
	150	•		•	•		M	10%	60	0.1
	150	•		•	•		M/883	10%	60	0.1
	170	•	•	•	•	•	C	10%	50	0.1
	170	•	•	•	•	•	I	10%	60	0.1
	170	•		•	•		M	10%	60	0.1
	170	•		•	•		M/883	10%	60	0.1
	200	•	•	•	•	•	C	10%	50	0.1
	200	•	•	•	•	•	I	10%	60	0.1
	200	•		•	•		M	10%	60	0.1
	200	•		•	•		M/883	10%	60	0.1
	250	•	•	•	•	•	C	10%	50	0.1
	250	•	•	•	•	•	I	10%	60	0.1
	250	•		•	•		M	10%	60	0.1
	250	•		•	•		M/883	10%	60	0.1
SMD Number for AT27C1024										
5962-86805 04	170	•			•		M/883	10%	60	0.1
5962-86805 03	200	•			•		M/883	10%	60	0.1
5962-86805 02	250	•			•		M/883	10%	60	0.1
5962-86805 01	300	•			•		M/883	10%	60	0.1

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C1024L

see page 4–71

Organization: 64K x 16
No. of Pins: DIP 40, LCC 44

Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
120	•		•	•		C	5%	30	0.1
150	•	•	•	•	•	C	10%	30	0.1
150	•	•	•	•	•	I	10%	40	0.1
150	•		•	•		M	10%	40	0.1
150	•		•	•		M/883	10%	40	0.1
170	•	•	•	•	•	C	10%	30	0.1
170	•	•	•	•	•	I	10%	40	0.1
170	•		•	•		M	10%	40	0.1
170	•		•	•		M/883	10%	40	0.1
200	•	•	•	•	•	C	10%	30	0.1
200	•	•	•	•	•	I	10%	40	0.1
200	•		•	•		M	10%	40	0.1
200	•		•	•		M/883	10%	40	0.1
250	•	•	•	•	•	C	10%	30	0.1
250	•	•	•	•	•	I	10%	40	0.1
250	•		•	•		M	10%	40	0.1
250	•		•	•		M/883	10%	40	0.1

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27HC1024

see page 4–81

Organization: 64K x 16 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	55	•		•	•		C	5%	80	8
	70	•	•	•	•	•	C	10%	80	8
	70	•	•	•	•	•	I	10%	90	10
	70	•		•	•		M	10%	90	10
	70	•		•	•		M/883	10%	90	10
	90	•	•	•	•	•	C	10%	80	8
	90	•	•	•	•	•	I	10%	90	10
	90	•		•	•		M	10%	90	10
	90	•		•	•		M/883	10%	90	10
	120	•	•	•	•	•	C	10%	80	8
	120	•	•	•	•	•	I	10%	90	10
	120	•		•	•		M	10%	90	10
	120	•		•	•		M/883	10%	90	10
SMD Number for AT27HC1024										
5962-86805 08	70	•			•		M/883	10%	90	10
5962-86805 07	90	•			•		M/883	10%	90	10

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPROM Product Selection Guide

AT27C040

see page 4–89

Organization: 512K x 8 No. of Pins: DIP 32, LCC 44	Speed (ns)	Package D	J	L	P	Temperature Range	Power Supply	Icc (mA) Active	Standby
	120	•				C	5%	25	0.1
	150	•	•	•	•	C	10%	25	0.1
	150	•	•	•	•	I	10%	30	0.1
	150	•		•		M	10%	30	0.1
	150	•		•		M/883	10%	30	0.1
	200	•	•	•	•	C	10%	25	0.1
	200	•	•	•	•	I	10%	30	0.1
	200	•		•		M	10%	30	0.1
	200	•		•		M/883	10%	30	0.1

Package Type	
D	32DW6, 32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	32P6, 32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PROM Product Selection Guide

AT28HC191

see page 5–3

Organization: 2K x 8
Number of Pins: DIP 24

Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
35	•	•	C	10%	80	60
45	•	•	C	10%	80	60
45	•	•	I	10%	80	60
45	•		M	10%	80	60
45	•		M/883	10%	80	60
55	•	•	C	10%	80	60
55	•	•	I	10%	80	60
55	•		M	10%	80	60
55	•		M/883	10%	80	60

AT28HC191L

see page 5–3

Organization: 2K x 8
Number of Pins: DIP 24

Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
45	•	•	C	10%	80	3
45	•	•	I	10%	80	3
45	•		M	10%	80	3
45	•		M/883	10%	80	3
55	•	•	C	10%	80	3
55	•	•	I	10%	80	3
55	•		M	10%	80	3
55	•		M/883	10%	80	3

Package Type	
D	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PROM Product Selection Guide

AT28HC291

see page 5–11

Organization: 2K x 8 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
	35	•		•	C	10%	80	60
	45	•	•	•	C	10%	80	60
	45	•	•	•	I	10%	80	60
	45	•	•		M	10%	80	60
	45	•	•		M/883	10%	80	60
	55	•	•	•	C	10%	80	60
	55	•	•	•	I	10%	80	60
	55	•	•		M	10%	80	60
	55	•	•		M/883	10%	80	60

AT28HC291L

see page 5–11

Organization: 2K x 8 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	Package L	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
	45	•		•	C	10%	80	3
	45	•		•	I	10%	80	3
	45	•			M	10%	80	3
	45	•			M/883	10%	80	3
	55	•	•	•	C	10%	80	3
	55	•	•	•	I	10%	80	3
	55	•	•		M	10%	80	3
	55	•	•		M/883	10%	80	3

Package Type	
D	24D3, 24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	28L, 28 Pad, Non Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

AT27HC641 –Not recommended for new designs. Use AT27HC641R.

AT27HC641R

see page 5–19

Organization: 8K x 8 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	L	P	Y	Temperature Range	Power Supply	Icc (mA) Active	Standby
	35	•	•			C	5%	45	25
	45	•	•	•		C	10%	45	25
	45	•	•	•		I	10%	50	30
	45	•	•			M	10%	50	30
	45	•	•			M/883	10%	50	30
	55	•	•	•		C	10%	45	25
	55	•	•	•		I	10%	50	30
	55	•	•			M	10%	50	30
	55	•	•			M/883	10%	50	30
	70	•	•	•		C	10%	45	25
	70	•	•	•		I	10%	50	30
	70	•	•			M	10%	50	30
	70	•	•			M/883	10%	50	30
	90	•	•	•		C	10%	45	25
	90	•	•	•		I	10%	50	30
	90	•	•			M	10%	50	30
	90	•	•			M/883	10%	50	30
SMD Number for AT27HC641R									
5962-87515 01	45	•	•		•	M/883	10%	50	30
5962-87515 02	55	•	•		•	M/883	10%	50	30
5962-87515 03	70	•	•		•	M/883	10%	50	30
5962-87515 04	90	•	•		•	M/883	10%	50	30

Package Type	
D	24DW6, 24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PROM Product Selection Guide

AT27HC642 –Not recommended for new designs. Use AT27HC642R.

AT27HC642R

see page 5–19

Organization: 8K x 8 Number of Pins: DIP 24	Speed (ns)	Package D	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
	35	•		C	5%	45	25
	45	•	•	C	10%	45	25
	45	•	•	I	10%	50	30
	45	•		M	10%	50	30
	45	•		M/883	10%	50	30
	55	•	•	C	10%	45	25
	55	•	•	I	10%	50	30
	55	•		M	10%	50	30
	55	•		M/883	10%	50	30
	70	•	•	C	10%	45	25
	70	•	•	I	10%	50	30
	70	•		M	10%	50	30
	70	•		M/883	10%	50	30
	90	•	•	C	10%	45	25
	90	•	•	I	10%	50	30
	90	•		M	10%	50	30
	90	•		M/883	10%	50	30
SMD Number for AT27HC642R							
5962-87515 01	45	•		M/883	10%	50	30
5962-87515 02	55	•		M/883	10%	50	30
5962-87515 03	70	•		M/883	10%	50	30
5962-87515 04	90	•		M/883	10%	50	30

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS PROM Product Selection Guide

AT32C16							see page 5–27
Organization: 32K x 16 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package J	Package P	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
	150	•	•	C	10%	30	0.1
	170	•	•	C	10%	30	0.1
	170	•	•	I	10%	40	0.2
	200	•	•	C	10%	30	0.1
	200	•	•	I	10%	40	0.2
	250	•	•	C	10%	30	0.1
	250	•	•	I	10%	40	0.2

Package Type	
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS SRAM Product Selection Guide

AT3864L

see page 6-3

Organization: 8K x 8 No. of Pins: DIP 28, SOIC 28	Speed (ns)	Package P	Package R	Temperature Range	Icc (mA) Active	Icc (mA) Standby
	100	•	•	C	35	0.1
	100	•	•	I	35	0.1
	120	•	•	C	35	0.1
	120	•	•	I	35	0.1
	150	•	•	C	35	0.1
	150	•	•	I	35	0.1

Package Type	
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS SRAM Product Selection Guide

AT3864L-15DMB					see page 6–11
Organization: 8K x 8 Number of Pins: DIP 28	**Speed (ns)**	**Package D**	**Temperature Range**	**Icc (mA) Active**	**Standby**
	150	•	M	40	1.0

	Package Type
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
	Temperature Range
M	Military (-55°C to 125°C)

CMOS SRAM Product Selection Guide

AT38LV64						see page 6–19
Organization: 8K x 8 No. of Pins: DIP 28, SOIC 28	Speed (ns)	Package P	Package R	Temperature Range	I_{CC} (mA) Active	I_{CC} (mA) Standby
	200	•	•	C	35	0.1

Package Type	
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
R	28R, 28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Logic Product Selection Guide

AT40391

see page 7–3

No. of Pins: Flatpack 160	Speed (ns)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	40	•	C	5%

AT40392

see page 7–3

No. of Pins: Flatpack 160	Speed (ns)	Package Q	Temperature Range	Power Supply
	25	•	C	5%
	33	•	C	5%
	40	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Logic Product Selection Guide

AT40491				see page 7–7
No. of Pins: Flatpack 160	**Speed (MHz)**	**Package Q**	**Temperature Range**	**Power Supply**
	25	•	C	5%
	33	•	C	5%

AT40492				see page 7–7
No. of Pins: Flatpack 160	**Speed (MHz)**	**Package Q**	**Temperature Range**	**Power Supply**
	25	•	C	5%
	33	•	C	5%

Package Type	
Q	160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS EPLD Product Selection Guide

AT18V8Z								see page 8–3
No. of Pins: DIP 20, LCC 20	Speed (ns)	Package D	Package J	Package P	Temperature Range	Power Supply	Icc Active mA (1MHz)	ICC Standby (μA)
	35	•	•	•	C	5%	2	100
	40	•	•	•	I	10%	2	100

Package Type	
D	20DW3, 20 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	20J, 20 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	20P3, 20 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)

CMOS EPLD Product Selection Guide

AT22V10

see page 8–19

Approx. Gates: 500 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package									Temp. Range	Power Supply	I_{CC} (mA)
		D	F	G	J	K	L	N	P	Y			
	15	•	•	•	•	•	•	•	•	•	C	10%	90
	15	•	•	•	•	•	•	•	•	•	I	10%	100
	15	•	•	•		•	•	•		•	M	10%	100
	15	•	•	•		•	•	•		•	M/883	10%	100
	20	•	•	•	•	•	•	•	•	•	C	10%	90
	20	•	•	•	•	•	•	•	•	•	I	10%	100
	20	•	•	•		•	•	•		•	M	10%	100
	20	•	•	•		•	•	•		•	M/883	10%	100
	25	•	•	•	•	•	•	•	•	•	C	10%	55
	25	•	•	•	•	•	•	•	•	•	I	10%	55
	25	•	•	•		•	•	•		•	M	10%	55
	25	•	•	•		•	•	•		•	M/883	10%	55
	30	•	•	•		•	•	•		•	M	10%	55
	30	•	•	•		•	•	•		•	M/883	10%	55
	35	•	•	•	•	•	•	•	•	•	C	10%	55
	35	•	•	•	•	•	•	•	•	•	I	10%	55
SMD Number for AT22V10													
5962-87539 04	20	•					•			•	M/883	10%	100
5962-87539 01	25	•					•			•	M/883	10%	55
5962-87539 02	30	•					•			•	M/883	10%	55
5962-87539 03	40	•					•			•	M/883	10%	55
5962-88670 04	20		•	•				•			M/883	10%	100
5962-88670 01	25		•	•				•			M/883	10%	55
5962-88670 02	30		•	•				•			M/883	10%	55
5962-88670 03	40		•	•				•			M/883	10%	55

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

AT22V10L

see page 8–19

Approx. Gates: 500 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)
	20	•	•	•	•	•	•	•	•	•	C	10%	12
	20	•	•	•	•	•	•	•	•	•	I	10%	15
	20	•	•	•		•	•	•		•	M	10%	15
	20	•	•	•		•	•	•		•	M/883	10%	15
	25	•	•	•	•	•	•	•	•	•	C	10%	12
	25	•	•	•	•	•	•	•	•	•	I	10%	15
	25	•	•	•		•	•	•		•	M	10%	15
	25	•	•	•		•	•	•		•	M/883	10%	15
	30	•	•	•		•	•	•		•	M	10%	15
	30	•	•	•		•	•	•		•	M/883	10%	15
	35	•	•	•	•	•	•	•	•	•	C	10%	12
	35	•	•	•	•	•	•	•	•	•	I	10%	15
SMD Number for AT22V10L													
5962-88724 01	25		•	•				•			M/883	10%	15
5962-88724 02	30		•	•				•			M/883	10%	15
5962-88724 03	40		•	•				•			M/883	10%	15
5962-89755 04	20		•	•				•			M/883	10%	15
5962-89755 01	25		•	•				•			M/883	10%	15
5962-89755 02	30		•	•				•			M/883	10%	15
5962-89755 03	40		•	•				•			M/883	10%	15

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV750

see page 8–35

Approx. Gates: 750 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)
	20	•	•	•	•	•	•	•	•	•	C	10%	120
	20	•	•	•	•	•	•	•	•	•	I	10%	140
	20	•	•	•		•	•	•		•	M	10%	140
	20	•	•	•		•	•	•		•	M/883	10%	140
	25	•	•	•	•	•	•	•	•	•	C	10%	120
	25	•	•	•	•	•	•	•	•	•	I	10%	140
	25	•	•	•		•	•	•		•	M	10%	140
	25	•	•	•		•	•	•		•	M/883	10%	140
	30	•	•	•	•	•	•	•	•	•	C	10%	120
	30	•	•	•	•	•	•	•	•	•	I	10%	140
	30	•	•	•		•	•	•		•	M	10%	140
	30	•	•	•		•	•	•		•	M/883	10%	140
	35	•	•	•	•	•	•	•	•	•	C	10%	120
	35	•	•	•	•	•	•	•	•	•	I	10%	140
	35	•	•	•		•	•	•		•	M	10%	140
	35	•	•	•		•	•	•		•	M/883	10%	140
	40	•	•	•	•	•	•	•	•	•	I	10%	140
	40	•	•	•		•	•	•		•	M	10%	140
	40	•	•	•		•	•	•		•	M/883	10%	140
SMD Number for ATV750													
5962-88726 02	35	•					•				M/883	10%	140
5962-88726 01	40	•					•				M/883	10%	140

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV750L

see page 8–35

Approx. Gates: 750 No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	F	G	J	K	L	N	P	Y	Temp. Range	Power Supply	Icc (mA)
	25	•	•	•	•	•	•	•	•	•	C	10%	12
	25	•	•	•	•	•	•	•	•	•	I	10%	15
	25	•	•	•		•	•	•		•	M	10%	15
	25	•	•	•		•	•	•		•	M/883	10%	15
	30	•	•	•	•	•	•	•	•	•	C	10%	12
	30	•	•	•	•	•	•	•	•	•	I	10%	15
	30	•	•	•		•	•	•		•	M	10%	15
	30	•	•	•		•	•	•		•	M/883	10%	15

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
F	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
G	24D3, 24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	28KW, 28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
N	28L, 28 Pad, Non-Windowed Ceramic Leadless Chip Carrier OTP (LCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Y	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV2500H

see page 8–55

Approx. Gates: 2500 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	I_{CC} (mA)
	25	•	•	•	•	•	C	10%	160
	25	•	•	•	•	•	I	10%	180
	25	•		•	•		M	10%	180
	25	•		•	•		M/883	10%	180
	30	•	•	•	•	•	C	10%	160
	30	•	•	•	•	•	I	10%	180
	30	•		•	•		M	10%	180
	30	•		•	•		M/883	10%	180
	35	•	•	•	•	•	C	10%	160
	35	•	•	•	•	•	I	10%	180
	35	•		•	•		M	10%	180
	35	•		•	•		M/883	10%	180

ATV2500L

see page 8–55

Approx. Gates: 2500 No. of Pins: DIP 40, LCC 44	Speed (ns)	Package D	J	K	L	P	Temperature Range	Power Supply	I_{CC} (mA)
	30	•	•	•	•	•	C	10%	5
	35	•	•	•	•	•	C	10%	5
	35	•	•	•	•	•	I	10%	10
	35	•		•	•		M	10%	10
	35	•		•	•		M/883	10%	10
	40	•	•	•	•	•	C	10%	5
	40	•	•	•	•	•	I	10%	10
	40	•		•	•		M	10%	10
	40	•		•	•		M/883	10%	10
	45	•	•	•	•	•	I	10%	10
	45	•		•	•		M	10%	10
	45	•		•	•		M/883	10%	10

Package Type	
D	40DW6, 40 Lead, 0.600" Wide, Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
J	44J, 44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
L	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
P	40P6, 40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATV5000

see page 8–73

Approx. Gates: 5000 No. of Pins: LCC 68, PGA 68	Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)
	25	•	•	•	C	10%	350
	30	•	•	•	C	10%	350
	30		•	•	I	10%	400
	30		•	•	M	10%	400
	30		•	•	M/883	10%	400
	35	•	•	•	C	10%	350
	35		•	•	I	10%	400
	35		•	•	M	10%	400
	35		•	•	M/883	10%	400

ATV5000L

see page 8–73

Approx. Gates: 5000 No. of Pins: LCC 68, PGA 68	Speed (ns)	Package J	Package K	Package U	Temperature Range	Power Supply	Icc (mA)
	30	•	•	•	C	10%	40
	35	•	•	•	C	10%	40
	35		•	•	I	10%	50
	35		•	•	M	10%	50
	35		•	•	M/883	10%	50

Package Type	
J	68J, 68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	68KW, 68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
U	68UW, 68 Pin, Windowed, Ceramic Pin Grid Array (PGA)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)
M/883	MIL-STD-883C, Class B, Fully Compliant (-55°C to 125°C)

CMOS EPLD Product Selection Guide

ATS42VA12							see page 8–101
No. of Pins: DIP 24, LCC 28	Speed (ns)	Package D	J	P	Temperature Range	Power Supply	I_{CC} (mA)
	35	•	•	•	C	5%	120

Package Type	
D	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	24P3, 24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS EPLD Product Selection Guide

ATS415							see page 8–123
No. of Pins: DIP 28, LCC 28	Speed (MHz)	Package D	Package J	Package P	Temperature Range	Power Supply	Icc (mA)
	16	•	•	•	C	5%	80

Package Type	
D	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
J	28J, 28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS EPLD Product Selection Guide

ATS2552							see page 8–143
No. of Pins: LCC 68	Speed (ns)	Package J	Package K	Temperature Range	Power Supply	Icc (mA) Active	Icc (mA) Standby
	35	•	•	C	5%	120	10
	50	•	•	C	5%	120	10

Package Type	
J	68J, 68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
K	68KW, 68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Temperature Range	
C	Commercial (0°C to 70°C)

CMOS Analog Product Selection Guide

AT76C10

see page 10–3

Delay (ms): 1.8
Gain (dB): 31.5
No. of Pins: DIP 16, SOIC 16

Bandwidth (kHz)	Package D	Package P	Package S	Temperature Range	Power Supply
4		•	•	C	10%
4		•	•	I	10%
4	•			M	5%

AT76C10E

see page 10–11

Delay (ms): 1.8
Gain (dB): 31.5
No. of Pins: DIP 16, SOIC 16

Bandwidth (kHz)	Package D	Package P	Package S	Temperature Range	Power Supply
4		•	•	C	10%
4		•	•	I	10%
4	•			M	5%

Package Type	
D	16D3, 16 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	16P3, 16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
S	16S, 16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Analog Product Selection Guide

AT76C120

see page 10–19

Organization: Dual 16/18-bit A/D No. of Pins: DIP 24, SOIC 24	Speed (kHz)	Signal-to-Noise (dB)	Accuracy (%FRS)	Package D	Package P	Package R	Temperature Range	Power Supply
	96	90	±0.006		•		C	10%
	96	90	±0.006		•		I	10%
	96	90	±0.006	•			M	5%
	96	84	±0.01		•	•	C	10%
	96	84	±0.01		•	•	I	10%
	96	84	±0.01	•			M	5%

Package Type	
D	24D6, 24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
P	24P6, 24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
R	24R, 24 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

AT76C171

–Not recommended for new designs. Use AT76C176A.

AT76C176

see page 10–27

Organization:
D/A: Triple 6-bit
RAM: 256 x 18
No. of Pins: DIP 28, LCC 32

Speed (MHz)	Package D	Package L	Package P	Temperature Range	Power Supply
40			•	C	10%
40			•	I	10%
40	•	•		M	5%
50			•	C	10%
50			•	I	10%
66			•	C	5%

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

CMOS Analog Product Selection Guide

AT76C176A

see page 10–39

Organization:
D/A: Triple 6-bit
RAM: 256 x 18
No. of Pins: DIP 28,
LCC 32, 44

Speed (MHz)	Package D	Package J1	Package J2	Package L	Package P	Temperature Range	Power Supply
50		•	•		•	C	10%
50		•	•		•	I	10%
50	•			•		M	5%
66		•	•		•	C	10%
66		•	•		•	I	10%
66	•			•		M	5%
80		•	•		•	C	10%
80		•	•		•	I	10%
110		•	•		•	C	5%

Package Type	
D	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
J1	32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
J2	44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
L	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
P	28P6, 28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Temperature Range	
C	Commercial (0°C to 70°C)
I	Industrial (-40°C to 85°C)
M	Military (-55°C to 125°C)

Explanation of Atmel's Part Number Code

All Atmel part numbers begin with the prefix "AT." The next four to nine digits are the part number. In addition, Atmel parts can be ordered in particular speeds, in specific packages, for particular temperature ranges and with the option of 883C level B military compliance. The available options for each part are listed at the back of its data sheet in its "Ordering Information" table. These options are designated by the following suffixes placed at the end of the Atmel part number, in the order given:

Prefix	Device -	Suffix
AT	XXXXX	X X X X

Processing

Blank	=	Standard
/883	=	MIL-STD-883, Class B Fully Compliant
B	=	MIL-STD-883, Clas B Non-Compliant

Temperature Range

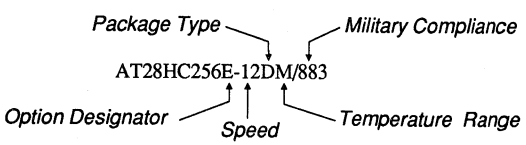
C	=	Com Temp (0°C to 70°C)
I	=	Ind Temp (-40°C to 85°C)
M	=	Mil Temp (-55°C to 125°C)

Package

B	=	Ceramic Side Braze Dual Inline
C	=	Cerpack
D	=	Cerdip
F	=	Flatpack
G	=	Cerdip, One Time Programmable
J	=	Plastic J-Lead Chip Carrier
K	=	Ceramic J-Lead Chip Carrier
L	=	Leadless Chip Carrier
M	=	Ceramic Module
N	=	Leadless Chip Carrier, One Time Programmable
P	=	Plastic DIP
R	=	SOIC
S	=	SOIC
T	=	TSOP
U	=	PGA
V	=	TAB
W	=	Die
X	=	Plastic J-leaded SOIC
Y	=	Cerpack
Z	=	Ceramic Multi-Chip Module

Speed

Here is an example of how to designate a part number:



Section 2

CMOS E^2PROMS

2-Wire Serial CMOS E^2PROM

1K (128 x 8)

Preliminary

Features

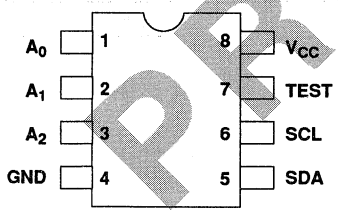
- **Low Voltage And Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 6.0 V)**
  - **2.5 V (V_{CC} = 2.5 V to 6.0 V)**
- **Internally Organized 128 x 8**
- **Two-wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **4-byte Page Write Mode**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight-pin PDIP And JEDEC SOIC Packages**

Description

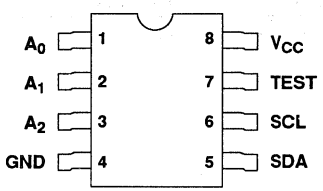
The AT24C01 provides 1024 bits of serial EEPROM (Electrically Erasable and Programmable Read Only Memory) organized as 128 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01 is available in space saving 8-pin PDIP and 8-pin SOIC packages and is accessed via a 2-wire serial interface. Atmel's EEPROMs are designed and tested for applications requiring extended endurance. The AT24C01 is guaranteed for 100,000 erase/write cycles and 100 year data retention. In addition, the AT24C01 is available in 5.0 V (4.5 V to 5.5 V), 3.0 V (2.7 V to 6.0 V) and 2.5 V (2.5 V to 6.0 V) versions.

Pin Configurations

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock
Test	**Test Input → to GND**



8 pin PDIP



8 pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5 V to +6.0 V, T_{AC} = 0°C to +70°C, V_{CC} = +2.5 V to +6.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.5	5.0	6.0	V
V_{CC2}	Supply Voltage		3.0	5.0	6.0	V
V_{CC3}	Supply Voltage		4.5	5.0	5.5	V
I_{CC1}	Supply Current V_{CC} = 2.5 V	100 KHz		1.0		mA
I_{CC2}	Supply Current V_{CC} = 3.0 V	100 KHz	0.5	2.0	3.0	mA
I_{CC3}	Supply Current V_{CC} = 5.0 V	100 KHz		2.0		mA
I_{SB4}	Standby Current V_{CC} = 6.0 V	V_{IN} = V_{CC} or V_{SS}			150	µA
I_{SB3}	Standby Current V_{CC} = 5.0 V	V_{IN} = V_{CC} or V_{SS}			110	µA
I_{SB2}	Standby Current V_{CC} = 3.0 V	V_{IN} = V_{CC} or V_{SS}			50	µA
I_{SB1}	Standby Current V_{CC} = 2.5 V	V_{IN} = V_{CC} or V_{SS}			30	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.1	10	µA
I_{IO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.1	10	µA
V_{IL}	Input Low Level(1)		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level(1)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0 V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 2.5 V	I_{OL} = 2.1 mA			0.45	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)			100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	250			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100			ns
t_{WR}	1 Byte Write Time		5	10	ms

Pin Capacitance(2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E²PROM in eight-bit words. Any device on the system bus receiving data (when communicating with the E²PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the nineth clock cycle after each word received and after all other system devices have freed the SDA bus. The E²PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver Timing diagram).

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +3.0 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)			100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	250			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100			ns
t_{WR}	1 Byte Write Time		5	10	ms

Pin Capacitance(2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

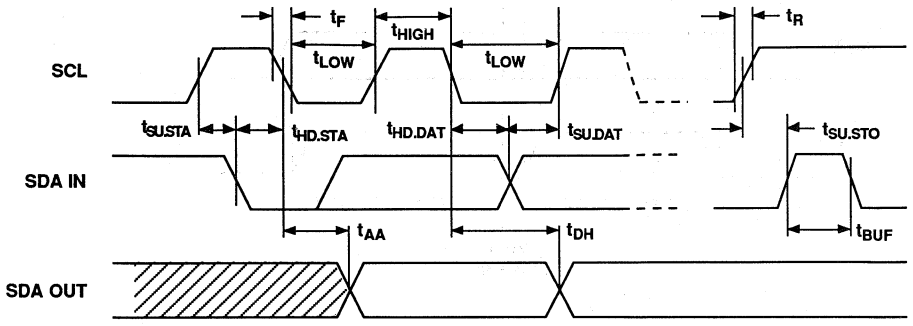
CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

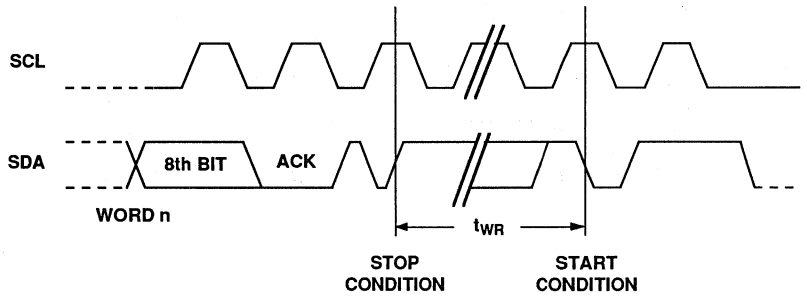
STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E²PROM in eight-bit words. Any device on the system bus receiving data (when communicating with the E²PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the nineth clock cycle after each word received and after all other system devices have freed the SDA bus. The E²PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver Timing diagram).

Bus Timing SCL: Serial Clock SDA: Serial Data I/O

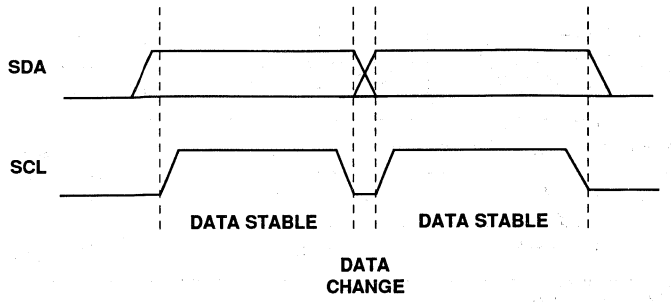


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

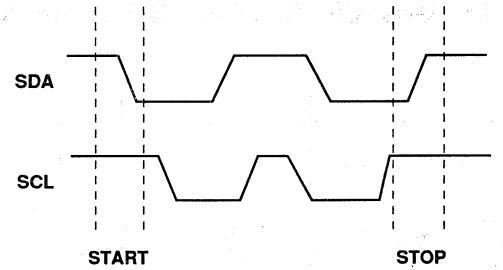


Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

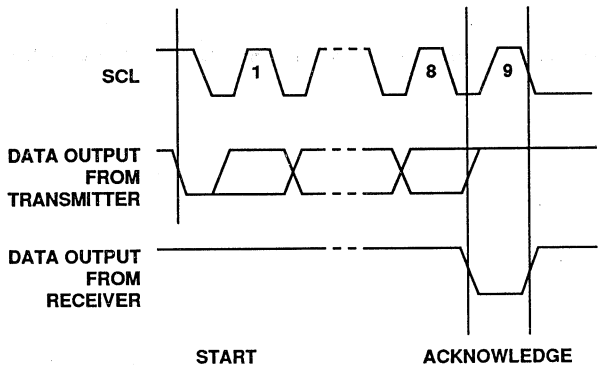
Data Validity



Start and Stop Definition



Acknowledge Response from Receiver



Write Operations

BYTE WRITE: Following a start condition, a write operation requires a seven-bit data word address and a low write bit. Upon receipt of this address, the E²PROM will again respond with an acknowledge on SDA and then clock in the first eight-bit data word. Following receipt of the eight-bit data word, the E²PROM will acknowledge SDA and the data transmitting device must terminate the write sequence with a stop condition. At this time the E²PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E²PROM will not respond for communication until the write is complete (refer to Figure 1).

PAGE WRITE: The AT24C01 is capable of a four- byte page write.

A page write is initiated the same as a byte write but the data transmitting device does not send a stop condition after the first data word is clocked in. Instead, after the E²PROM acknowledges receipt of the first data word, the data transmitting device can transmit up to three more data words. The E²PROM will respond with an acknowledge on SDA after each data word received. The transmitting device must terminate the page write sequence with a stop condition (refer to Figure 2).

The data word address lower two bits are internally incremented following the receipt of each data word. The higher five data word address bits are not incremented retaining the memory page row location. If more than four data words are transmitted to the E²PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E²PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E²PROM respond with an acknowledge on the SDA bus allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are two read operations: byte read and sequential read.

BYTE READ: A byte read is initiated with a start condition followed by a seven bit data word address and a high read bit. The AT24C01 will respond with an acknowledge and then serially transmit eight data bits to the SDA bus. The device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 3).

SEQUENTIAL READ: Sequential reads are initiated the same as a byte read. After the device reading the data receives an eight bit data word, it responds with an acknowledge. As long as the E²PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 4).

Figure 1. Byte Write

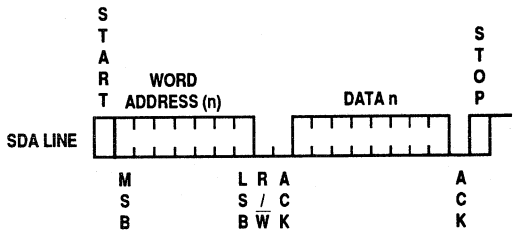


Figure 2. Page Write

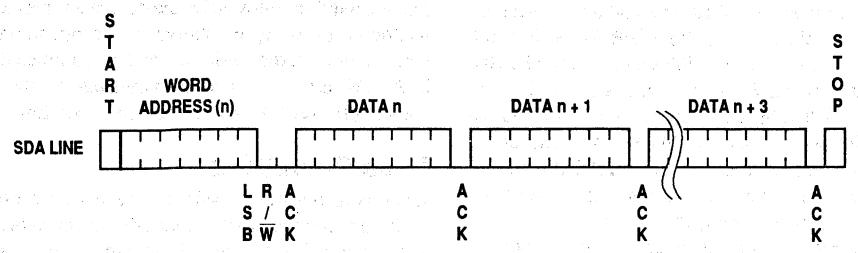


Figure 3. Byte Read

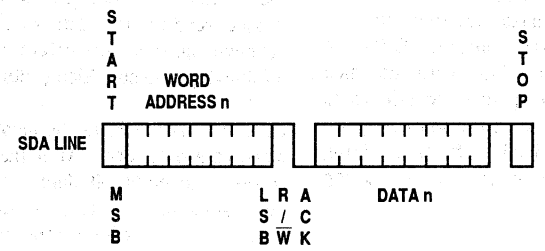
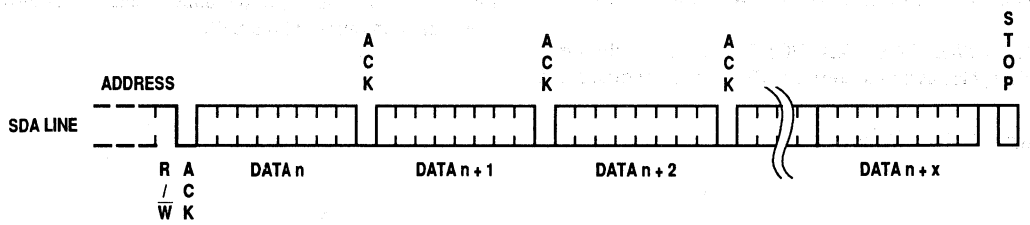


Figure 4. Sequential Read



Ordering Information

t_{WR} (ms)	I_{CC} (mA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2.0	100	AT24C01-10PC (-2.7/-2.5) AT24C01-10SC (-2.7/-2.5)	8P3 8S1	Commercial (0°C to 70°C)
			AT24C01-10PI (-2.7/-2.5) AT24C01-10SI (-2.7/-2.5)	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)

2-Wire Serial CMOS E²PROMs

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

Preliminary

Features

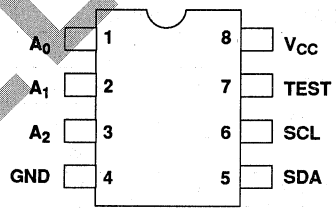
- **Low Voltage And Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 6.0 V)**
  - **2.5 V (V_{CC} = 2.5 V to 6.0 V)**
- **Internally Organized 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **8-byte Page (2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Self-timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight And Fourteen-pin JEDEC SOIC And Eight-pin PDIP Packages**

Description

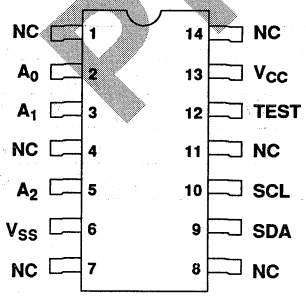
The AT24C02/04/08/16 provides 2048/4096/8192/16384 bits of serial EEPROM (Electrically Erasable and Programmable Read Only Memory) organized as 256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C02/04/08/16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. Atmel's EEPROMs are designed and tested for applications requiring extended endurance. The AT24C02/04/08/16 is guaranteed for 100,000 erase/write cycles and 100 year data retention. In addition, the entire family is available in 5.0 V (4.5 V to 5.5 V), 3.0 V (2.7 V to 6.0 V) and 2.5 V (2.5 V to 6.0 V) versions.

Pin Configurations

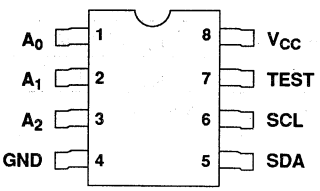
Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
Test	**Test Input → to GND**
NC	No Connect



8 pin PDIP



14 pin SOIC



8 pin SOIC

Memory Page Organization

AT24C02, 2K SERIAL E²PROM: Internally organized with 256 eight-bit words, the 2K requires an eight-bit data word address for random word addressing.

AT24C04, 4K SERIAL E²PROM: The 4K is internally organized with two pages of 256 eight-bit words. Random word addressing requires a nine-bit data word address.

AT24C08, 8K SERIAL E²PROM: The 8K is internally organized with four pages of 256, eight-bit words. Random word addressing requires a ten-bit data word address.

AT24C16, 16K SERIAL E²PROM: The 16K is internally organized with eight pages of 256, eight-bit words. Random word addressing requires an eleven-bit data word address.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.6 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5 V to +6.0 V, T_{AC} = 0°C to +70°C, V_{CC} = +2.5 V to +6.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.5	5.0	6.0	V
V_{CC2}	Supply Voltage		3.0	5.0	6.0	V
V_{CC3}	Supply Voltage		4.5	5.0	5.5	V
I_{CC1}	Supply Current V_{CC} = 2.5 V	100 KHz		1.0		mA
I_{CC2}	Supply Current V_{CC} = 3.0 V	100 KHz	0.5	2.0	3.0	mA
I_{CC3}	Supply Current V_{CC} = 5.0 V	100 KHz		2.0		mA
I_{SB1}	Standby Current V_{CC} = 6.0 V	V_{IN} = V_{CC} or V_{SS}			150	µA
I_{SB2}	Standby Current V_{CC} = 5.0 V	V_{IN} = V_{CC} or V_{SS}			110	µA
I_{SB3}	Standby Current V_{CC} = 3.0 V	V_{IN} = V_{CC} or V_{SS}			50	µA
I_{SB4}	Standby Current V_{CC} = 2.5 V	V_{IN} = V_{CC} or V_{SS}			30	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.1	10	µA
I_{IO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.1	10	µA
V_{IL}	Input Low Level(1)		-1.0		V_{CC} x 0.3	V
V_{IH}	Input High Level(1)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0 V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 2.5 V	I_{OL} = 2.1 mA			0.45	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)			100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	250			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100			ns
t_{WR}	1 Byte Write Time		5	10	ms

Pin Capacitance(2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor as shown in Figure 7. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition Timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition Timing Diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the E²PROM in eight-bit words. Any device on the system bus receiving data (when communicating with the E²PROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the nineth clock cycle after each word received and after all other system devices have freed the SDA bus. The E²PROM will likewise acknowledge by pulling SDA low after receiving each address or data word (refer to Acknowledge Response from Receiver Timing diagram).

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +3.0 V to +6.0 V CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency, SCL	0		100	kHz
t_{LOW}	Clock Pulse Width Low	4.7			µs
t_{HIGH}	Clock Pulse Width High	4.0			µs
t_I	Noise Suppression Time(2)			100	ns
t_{AA}	Clock Low to Data Out Valid	0.1		3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7			µs
$t_{HD.STA}$	Start Hold Time	4.0			µs
$t_{SU.STA}$	Start Set-up Time	4.7			µs
$t_{HD.DAT}$	Data In Hold Time	0.0			µs
$t_{SU.DAT}$	Data In Set-up Time	250			ns
t_R	Inputs Rise Time(2)			1.0	µs
t_F	Inputs Fall Time(2)			300	ns
$t_{SU.STO}$	Stop Set-up Time	4.7			µs
t_{DH}	Data Out Hold Time	100			ns
t_{WR}	1 Byte Write Time		5	10	ms

Pin Capacitance(2)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0 V

Note: 2. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SCL and SDA bus lines are normally pulled high with a resistor as shown in Figure 7. Data on the SDA bus may change only during SCL low time periods (refer to Data Validity Timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

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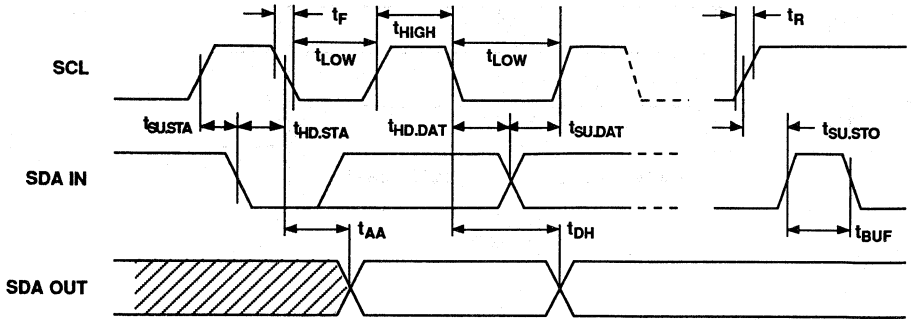
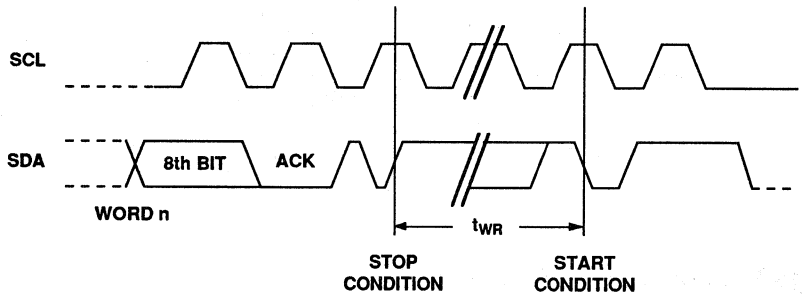
Bus Timing SCL: Serial Clock SDA: Serial Data I/O

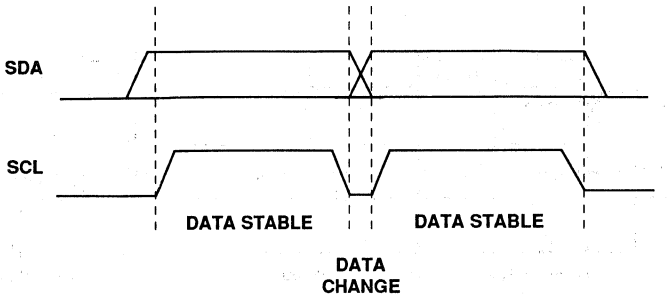


Write Cycle Timing SCL: Serial Clock SDA: Serial Data I/O

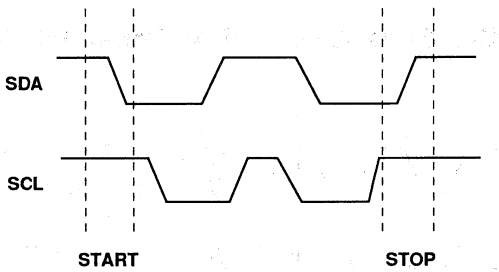


Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

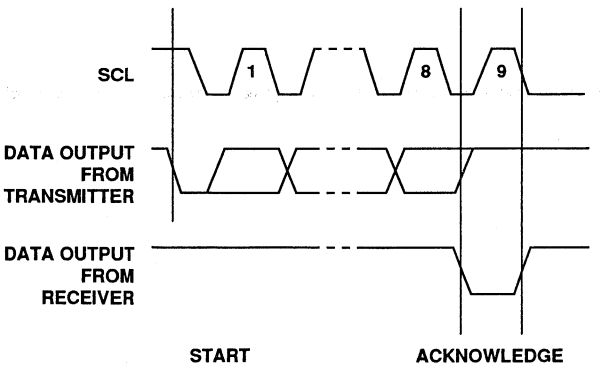
Data Validity



Start and Stop Definition



Acknowledge Response from Receiver



DEVICE ADDRESSING: The 2K, 4K, 8K and 16K E²PROM devices all require an eight-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the E²PROM devices.

The next three bits are the A2, A1 and A0 device address bits for the 2K E²PROM. These three bits must compare to their corresponding hard-wired input pins.

The 4K E²PROM only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hard-wired input pins. The A0 pin is no connect.

The 8K E²PROM only uses the A2 device address bit with the next two bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The 16K does not use any device address bits but instead the three bits are used for memory page addressing. These page addressing bits on the 4K and 16K devices should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the E²PROM will output an acknowledge on the SDA bus. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an eight-bit data word address following the device address word and acknowledgement. Upon receipt of this address, the E²PROM will again respond with an acknowledge on SDA and then clock in the first eight-bit data word. Following receipt of the eight-bit data word, the E²PROM will acknowledge SDA and the data transmitting device must terminate the write sequence with a stop condition. At this time the E²PROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the E²PROM will not respond for communication until the write is complete (refer to Figure 2).

PAGE WRITE: The 2K E²PROM is capable of an eight-byte page write, and the 4K, 8K and 16K devices are capable of sixteen-byte page writes.

A page write is initiated the same as a byte write, but the data transmitting device does not send a stop condition after the first data word is clocked in. Instead, after the E²PROM acknowledges receipt of the first data word, the data transmitting device can transmit up to seven (2K) or fifteen (4K, 8K, 16K) more data words. The E²PROM will respond with an acknowledge on SDA after each data word received. The transmitting device must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower three (2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented retaining the memory page row location. If more than eight (2K) or sixteen (4K, 8K, 16K) data words are transmitted to the E²PROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the E²PROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the E²PROM respond with an acknowledge on the SDA bus allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. If the last operation was a read at address n, then the current address would be n+1. If the final operation was a write at address n, the current address would again be n+1 with one exception. If address n was the eighth (2K) or sixteenth (4K, 8K, 16K) byte address in the memory row, the incremented address n+1 would "roll over" to the 1st byte address of the same row.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the E²PROM, the current address data word is serially clocked out. The device that is reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 4)

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the E²PROM, the transmitting device must generate another start condition. The transmitting device now initiates a current address read by sending a device address with the read/write select bit high. The E²PROM acknowledges the device address and serially clocks out the data word. The device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the device reading the data receives a data word, it responds with an acknowledge. As long as the E²PROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the device reading the data does not respond with an acknowledge (leaving the SDA bus high) but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

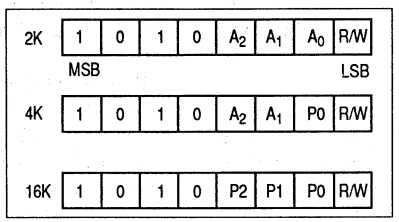


Figure 2. Byte Write

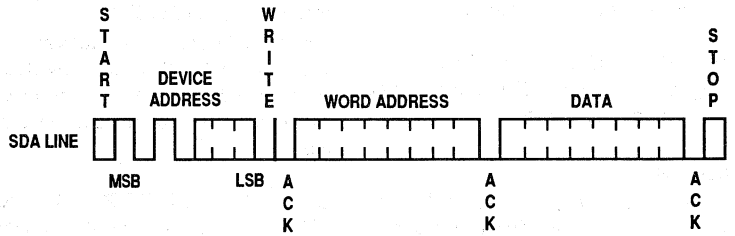


Figure 3. Page Write

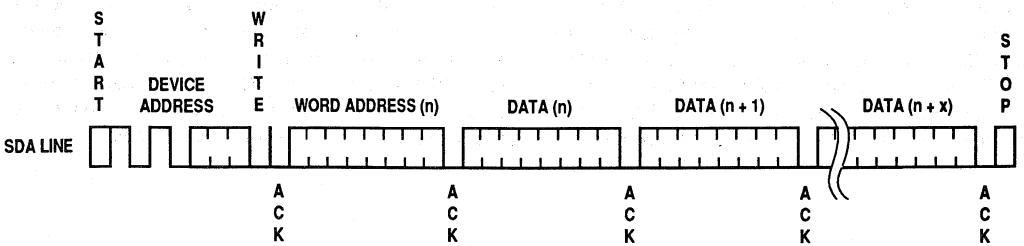


Figure 4. Current Address Read

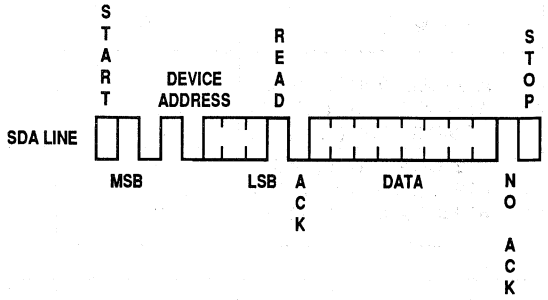


Figure 5. Random Read

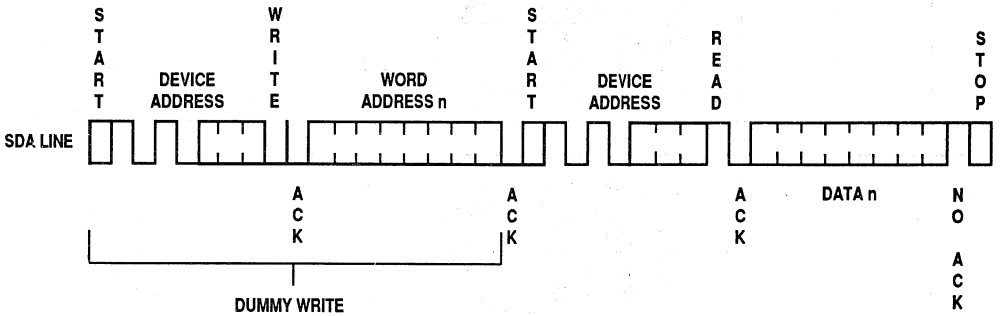


Figure 6. Sequential Read

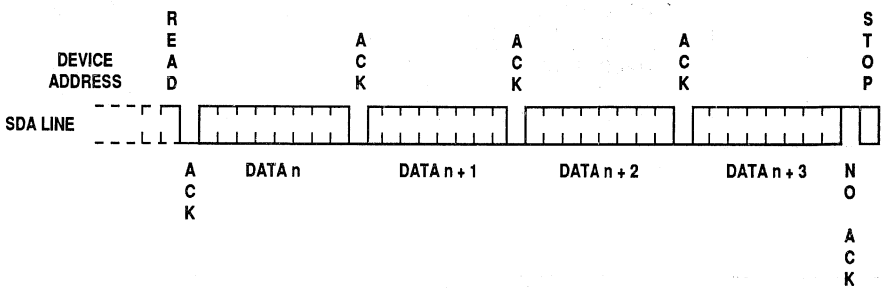
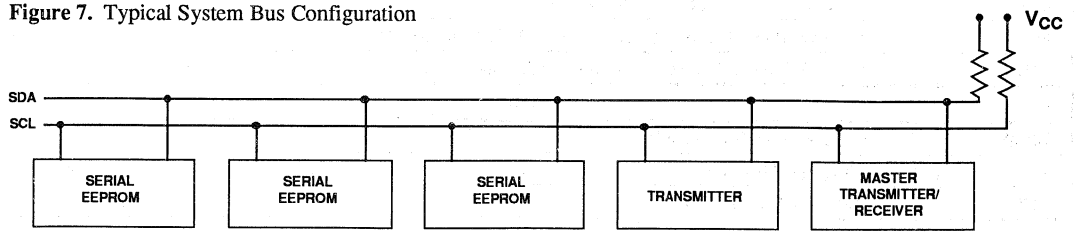


Figure 7. Typical System Bus Configuration



Ordering Information

t_{WR} (ms)	I_{CC} (mA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2.0	100	AT24C02-10PC (-2.7/-2.5) AT24C02N-10SC (-2.7/-2.5) AT24C02-10SC (-2.7/-2.5)	8P3 8S1 14S	Commercial (0°C to 70°C)
			AT24C02-10PI (-2.7/-2.5) AT24C02N-10SI (-2.7/-2.5) AT24C02-10SI (-2.7/-2.5)	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	2.0	100	AT24C04-10PC (-2.7/-2.5) AT24C04N-10SC (-2.7/-2.5) AT24C04-10SC (-2.7/-2.5)	8P3 8S1 14S	Commercial (0°C to 70°C)
			AT24C04-10PI (-2.7/-2.5) AT24C04N-10SI (-2.7/-2.5) AT24C04-10SI (-2.7/-2.5)	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	2.0	100	AT24C08-10PC (-2.7/-2.5) AT24C08N-10SC (-2.7/-2.5) AT24C08-10SC (-2.7/-2.5)	8P3 8S1 14S	Commercial (0°C to 70°C)
			AT24C08-10PI (-2.7/-2.5) AT24C08N-10SI (-2.7/-2.5) AT24C08-10SI (-2.7/-2.5)	8P3 8S1 14S	Industrial (-40°C to 85°C)
10	2.0	100	AT24C16-10PC (-2.7/-2.5) AT24C16N-10SC (-2.7/-2.5) AT24C16-10SC (-2.7/-2.5)	8P3 8S1 14S	Commercial (0°C to 70°C)
			AT24C16-10PI (-2.7/-2.5) AT24C16N-10SI (-2.7/-2.5) AT24C16-10SI (-2.7/-2.5)	8P3 8S1 14S	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S 1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
14S	14 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 6.0 V)
-2.5	Low Voltage (2.5 V to 6.0 V)

3-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Preliminary

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (Vcc = 4.5 V to 5.5 V)**
  - **3.0 V (Vcc = 2.7 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Three-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **8-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages**

Description

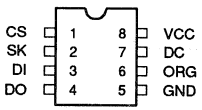
The AT93C46/56/66 provides 1024/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to Vcc and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/66 is available in space saving 8-pin PDIP and 8-pin JEDEC and EIAJ SOIC packages.

The AT93C46/56/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

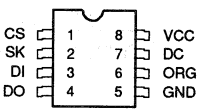
Atmel's E²PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT93C46/56/66 is available in 5.0 V ± 10% and 2.7 Vto 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
DC	Don't Connect

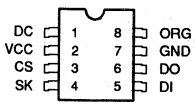


8-Pin PDIP



8-Pin SOIC

Rotated (R)
(1K JEDEC Only)



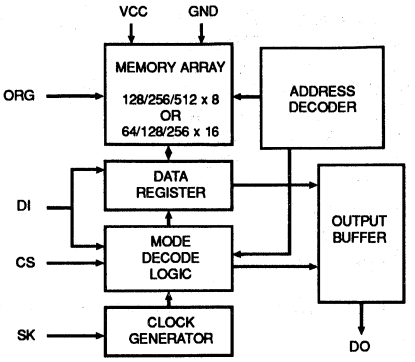
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

D.C. Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.7 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +2.7 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{IH},	SK = 1.0 MHz(1) SK = 0.5 MHz(1)		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH},	SK = 1.0 MHz(1) SK = 0.5 MHz(1)		3 3	mA
I_{CC3}	Standby Current	CS = 0 V	SK = 1.0 MHz(1) SK = 0.5 MHz(1)		100 100	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}		-2.5 -10	2.5 10	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}		-2.5 -10	2.5 10	µA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V		-0.1 2	0.6 VCC + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 2.1 mA I_{OH} = -400 µA		 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 10 µA I_{OH} = -10 µA		 V_{CC} - 0.2	0.2	V V

Note: 1. Devices operate at 1.0 MHz at VCC = 5.0 V ± 10% at commercial temperature. All low voltage and industrial parts operate at 0.5 MHz.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.7 V to +5.5 V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
f_{SK}	SK Clock Frequency		0 0	1 0.5	MHz
t_{SKH}	SK High Time	Note 1 Note 2	500 500		ns
t_{SKL}	SK Low Time	Note 1 Note 2	250 500		ns
t_{CS}	Minimum CS Low Time	Note 3 Note 4	250 500		ns
t_{CSS}	CS Setup Time	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time	Relative to SK	0		ns
t_{DIH}	DI Hold Time	Relative to SK	100 200		ns
t_{PD1}	Output Delay to '1'	AC Test		500 1000	ns
t_{PD0}	Output Delay to '0'	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	AC Test		500 1000	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time			10	ms
	Endurance	Number of Data Changes per Bit	Typical 100,000		Cycles

Notes:
1. The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 µs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 µs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.
2. The SK frequency specification for extended Temperature parts specifies a minimum SK clock period of 2 µs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 µs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 µs in order to meet the SK frequency specification.
3. For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.
4. For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT93C46/56/66 is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by 7 instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Instruction Set for the AT93C46

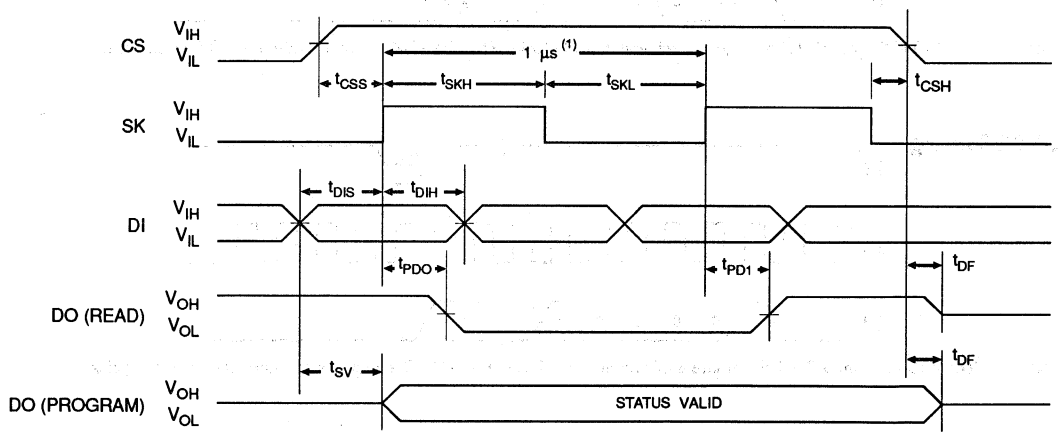
Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6-A_0	A_5-A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXX	01XXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8-A_0	A_7-A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



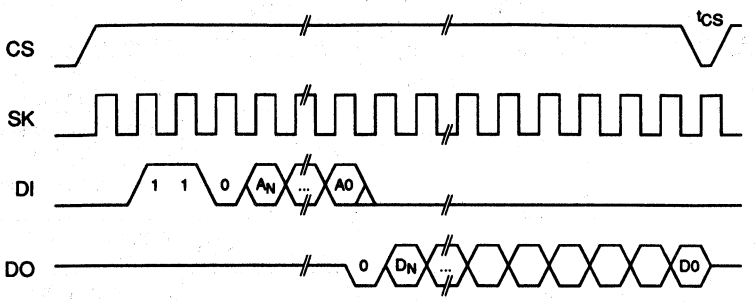
Note: 1. This is the minimum SK period.

Organization Key for Timing Diagrams

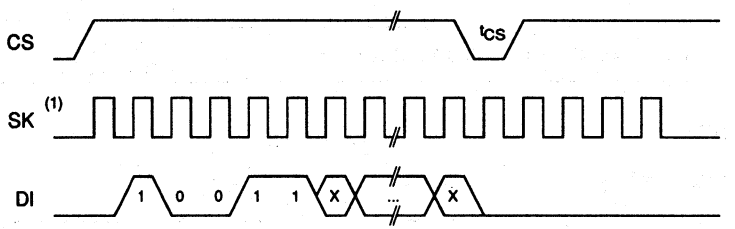
I/O	Density 1K x 8	Density 1K x 16	Density 2K x 8	Density 2K x 16	Density 4K x 8	Density 4K x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

Timing Diagrams (Continued)

READ Timing

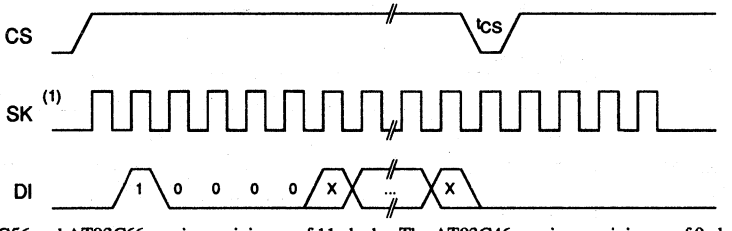


EWEN Timing



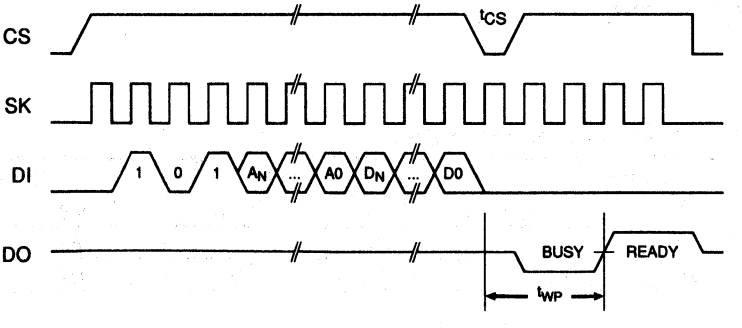
Note: 1. The AT93C56 and AT93C66 require a minimum of 11 clocks. The AT93C46 requires a minimum of 9 clock cycles.

EWDS Timing



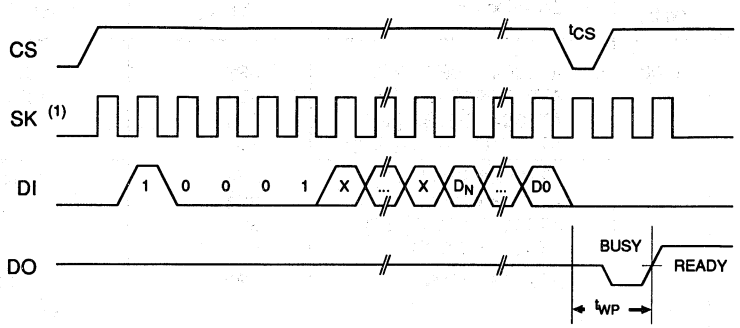
Note: 1. The AT93C56 and AT93C66 require a minimum of 11 clocks. The AT93C46 requires a minimum of 9 clock cycles.

WRITE Timing



Timing Diagrams (Continued)

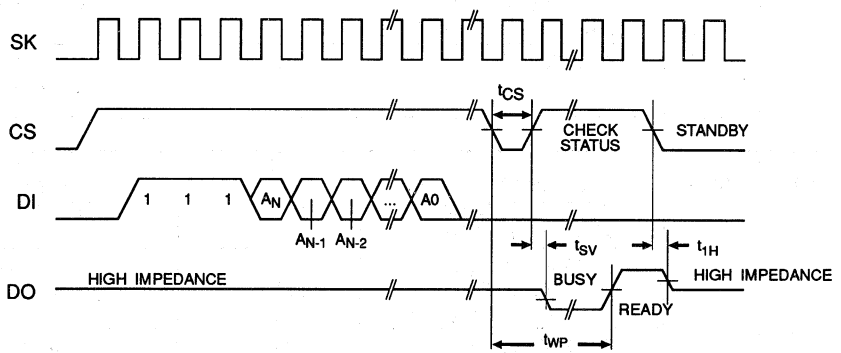
WRAL Timing [2]



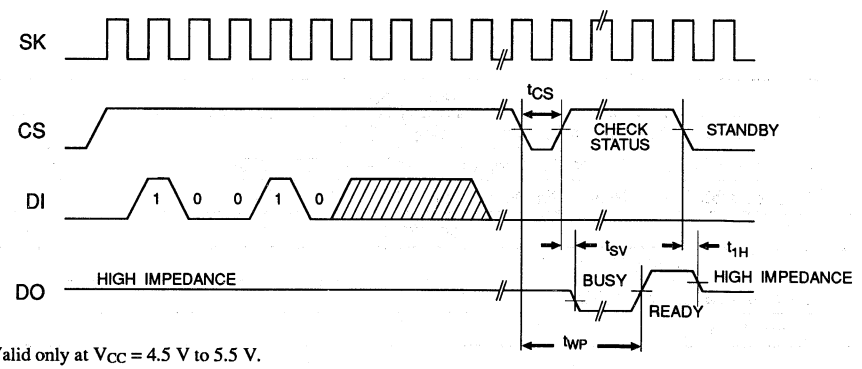
Notes: 1. The AT93C56 and AT93C66 require a minimum of 11 clocks. The AT93C46 requires a minimum of 9 clock cycles.

2. Valid only at V_{CC} = 4.5 V to 5.5 V.

ERASE Timing



ERAL Timing [1]



Note: 1. Valid only at V_{CC} = 4.5 V to 5.5 V.

Ordering Information

t_{WP} (ms)	I_{CC} (mA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3.0	1000	AT93C46-10PC (-2.7) AT93C46-10SC (-2.7) AT93C46R-10SC (-2.7) AT93C46W-10SC (-2.7)	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
			AT93C46-10PI (-2.7) AT93C46-10SI (-2.7) AT93C46R-10SI (-2.7) AT93C46W-10SI (-2.7)	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
			AT93C46-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT93C56-10PC (-2.7) AT93C56-10SC (-2.7) AT93C56W-10SC (-2.7)	8P3 8S1 8S2	Commercial (0°C to 70°C)
			AT93C56-10PI (-2.7) AT93C56-10SI (-2.7) AT93C56W-10SI (-2.7)	8P3 8S1 8S2	Industrial (-40°C to 85°C)
			AT93C56-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT93C66-10PC (-2.7) AT93C66-10SC (-2.7) AT93C66W-10SC (-2.7)	8P3 8S1 8S2	Commercial (0°C to 70°C)
			AT93C66-10PI (-2.7) AT93C66-10SI (-2.7) AT93C66W-10SI (-2.7)	8P3 8S1 8S2	Industrial (-40°C to 85°C)
			AT93C66-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
R	Rotated Pinout

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Four-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **8-Pin PDIP and JEDEC SOIC Packages**

4-Wire Serial CMOS E^2PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Preliminary

Description

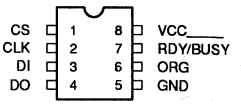
The AT59C11/12/13 provides 1024/2048/4096 bits of serial E^2PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/12/13 is available in space saving 8-pin PDIP and 8-pin JEDEC and SOIC packages.

The AT59C11/12/13 is enabled through the Chip Select pin (CS), and accessed via a 4-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/$\overline{\text{Busy}}$ status can be monitered upon completion of a programming operation by polling the Ready/$\overline{\text{Busy}}$ pin.

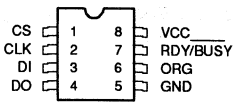
Atmel's E^2PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT59C11/12/13 is available in 5.0 V ± 10% and 2.7 V to 5.5 V versions. Data retention is specified to be greater than 100 years.

Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
RDY/$\overline{\text{BUSY}}$	Status Output



8-Pin PDIP



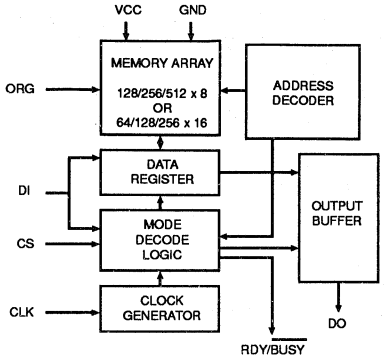
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

D.C. Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.7 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +2.7 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{IH}, CLK = 1.0 MHz(1) CLK = 0.5 MHz(1)		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, CLK = 1.0 MHz(1) CLK = 0.5 MHz(1)		3 3	mA
I_{CC3}	Standby Current	CS = 0 V CLK = 1.0 MHz(1) CLK = 0.5 MHz(1)		100 100	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}	-2.5 -10	2.5 10	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}	-2.5 -10	2.5 10	µA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V	2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V	-0.1 2	0.6 VCC + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 2.1 mA I_{OH} = -400 µA	2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 10 µA I_{OH} = -10 µA	V_{CC} - 0.2	0.2	V V

Note: 1. Devices operate at 1.0 MHz at VCC = 5.0 V ± 10% at commercial temperature. All low voltage and industrial parts operate at 0.5 MHz.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.7 V to +5.5 V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
f_{CLK}	CLK Clock Frequency		0 0	1 0.5	MHz
t_{CKH}	CLK High Time	Note 1 Note 2	500 500		ns
t_{CKL}	CLK Low Time	Note 1 Note 2	250 500		ns
t_{CS}	Minimum CS Low Time	Note 3 Note 4	250 500		ns
t_{CSS}	CS Setup Time	Relative to CLK	50 100		ns
t_{DIS}	DI Setup Time	Relative to CLK	100 200		ns
t_{CSH}	CS Hold Time	Relative to CLK	0		ns
t_{DIH}	DI Hold Time	Relative to CLK	100 200		ns
t_{PD}	Output Delay	AC Test		500 1000	ns
t_{RBD}	CS to Status Valid	AC Test		500 1000	ns
t_{CZ}	CS to DO in High Impedance	AC Test CS = V_{IL}		100 200	ns
t_{WC}	Write Cycle Time			10	ms
	Endurance	Number of Data Changes per Bit	Typical 100,000		Cycles

Notes:
1. The CLK frequency specification for Commercial parts specifies a minimum CLK clock period of 1 µs, therefore in an CLK clock cycle t_{CKH} + t_{CKL} must be greater than or equal to 2 µs. For example if t_{CKL} = 250 ns then the minimum t_{CKH} = 750 ns in order to meet the CLK frequency specification.
2. The CLK frequency specification for extended Temperature parts specifies a minimum CLK clock period of 2 µs, therefore in an CLK clock cycle t_{CKH} + t_{CKL} must be greater than or equal to 2 µs. For example, if the t_{CKL} = 500 ns then the minimum t_{CKH} = 1.5 µs in order to meet the CLK frequency specification.
3. For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.
4. For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, CLK, DI, RDY/$\overline{BUSY}$)	5	pF	V_{IN} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT59C11/12/13 are accessed via a simple and versatile 4-wire serial communication interface. Device operation is controlled by 6 instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/12/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/12/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The ERAL instruction is valid only at V_{CC} = 5.0 V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/12/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The WRAL instruction is valid only at V_{CC} = 5.0 V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Instruction Set for the AT59C11

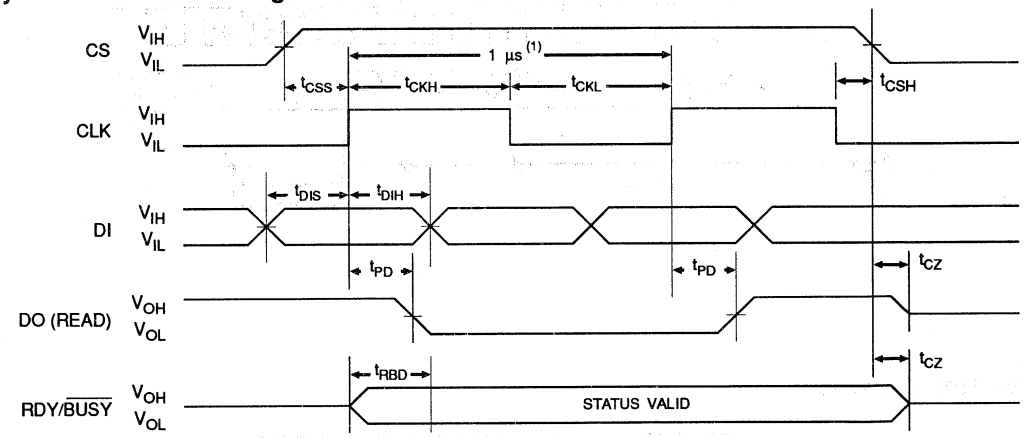
Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	0000000	000000			Write enable must precede all programming modes.
WRITE	1	X1XX	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	0000000	000000			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	0000000	000000	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	0000	0000000	000000			Disables all programming instructions.

Instruction Set for the AT59C12 and AT59C13

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	000000000	00000000			Write enable must precede all programming modes.
WRITE	1	X1XX	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	000000000	00000000			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	000000000	00000000	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	0000	000000000	00000000			Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



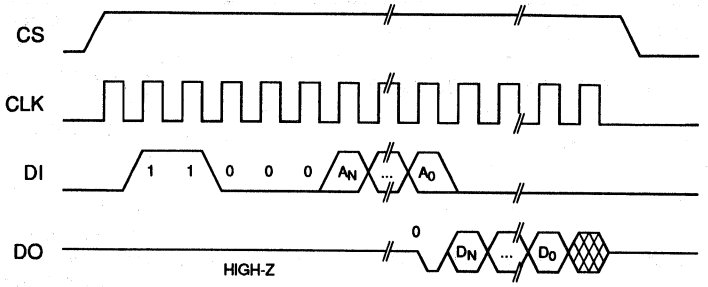
Note: 1. This is the minimum CLK period.

Organization Key for Timing Diagrams

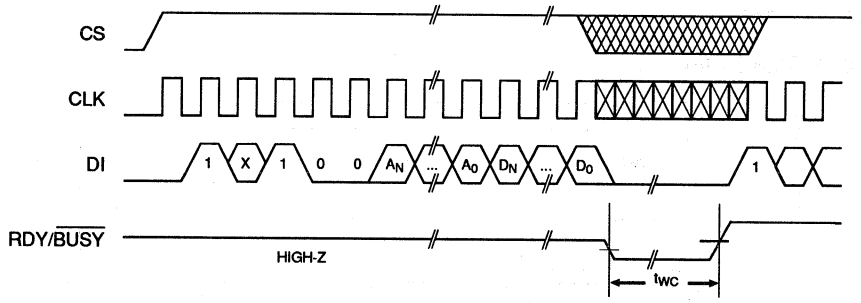
I/O	Density 1K x 8	Density 1K x 16	Density 2K x 8	Density 2K x 16	Density 4K x 8	Density 4K x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

Timing Diagrams (Continued)

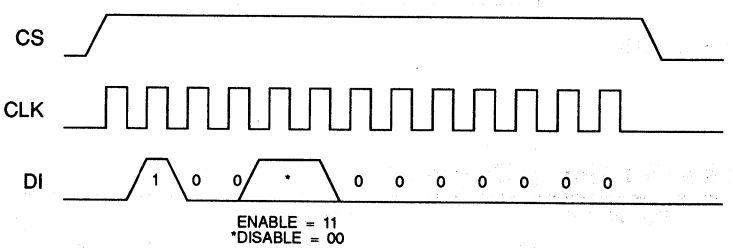
READ Timing



WRITE Timing

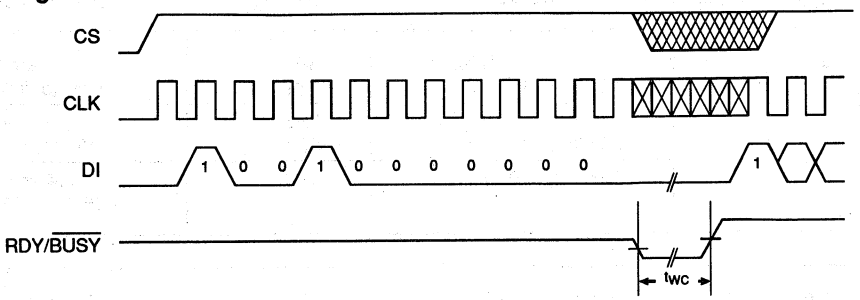


EWEN/EWDS Timing

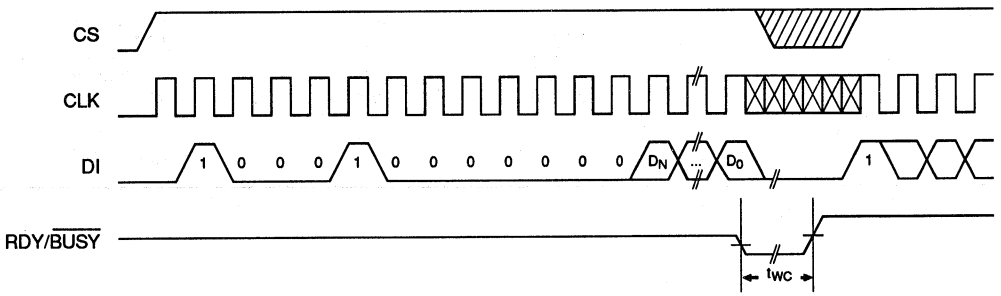


Timing Diagrams (Continued)

ERAL Timing



WRAL Timing



Ordering Information

t_{WC} (ms)	I_{CC} (mA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	3.0	1000	AT59C11-10PC (-2.7) AT59C11-10SC (-2.7)	8P3 8S1	Commercial (0°C to 70°C)
			AT59C11-10PI (-2.7) AT59C11-10SI (-2.7)	8P3 8S1	Industrial (-40°C to 85°C)
			AT59C11-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT59C12-10PC (-2.7) AT59C12-10SC (-2.7)	8P3 8S1	Commercial (0°C to 70°C)
			AT59C12-10PI (-2.7) AT59C12-10SI (-2.7)	8P3 8S1	Industrial (-40°C to 85°C)
			AT59C12-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT59C13-10PC (-2.7) AT59C13-10SC (-2.7)	8P3 8S1	Commercial (0°C to 70°C)
			AT59C13-10PI (-2.7) AT59C13-10SI (-2.7)	8P3 8S1	Industrial (-40°C to 85°C)
			AT59C13-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)

4K (512K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150ns
- Fast Byte Write - 200µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
- Low Power
  - 30mA Active Current
  - 100µa CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 cycles
  - Data Retention: 10 years
- 5V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

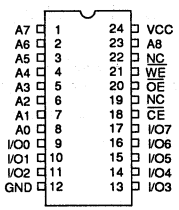
Description

The AT28C04 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C04 is a 4k memory organized as 512 words x 8 bits. The device is manufactured with Atmel's reliable non-volatile CMOS technology.

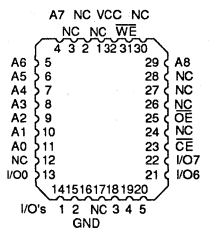
The AT28C04 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by DATA polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100µA. Atmel's 28C04 has additional features to ensure high quality and manufacturability, including internal error correction for extended endurance and for improved data retention characteristics.

Pin Configurations

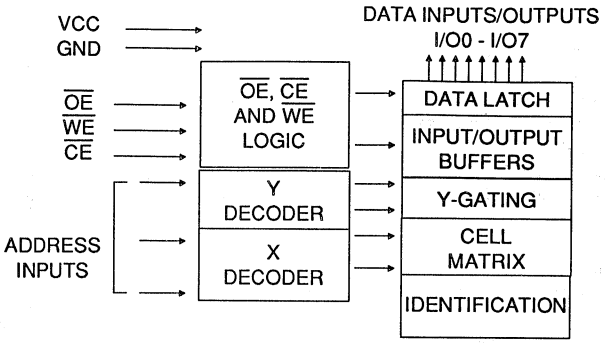


Pin Name	Function
A0 - A8	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28C04 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C04 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C04F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 0.1 seconds.

$\overline{DATA}$ POLLING: The AT28C04 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C04 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to VCC +0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C04-15	AT28C04-20	AT28C04-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to VCC + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to VCC			10	µA
I_{SB1}	VCC Standby Current CMOS	$\overline{CE}$=VCC-0.3V to VCC + 1.0V			100	µA
I_{SB2}	VCC Standby Current TTL	$\overline{CE}$=2.0V to VCC + 1.0V	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	VCC Active Current A.C.	f=5MHz; I_{OUT}=0mA $\overline{CE}$=V_{IL}	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-400µA		2.4		V

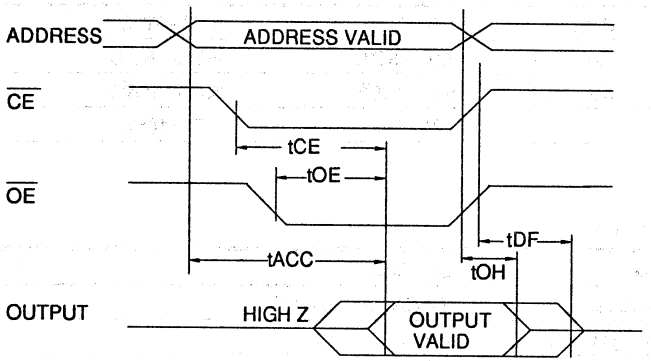
Pin Capacitance (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

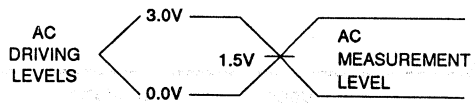
Symbol	Parameter	AT28C04-15		AT28C04-20		AT28C04-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



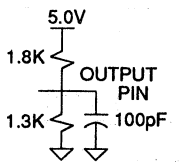
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

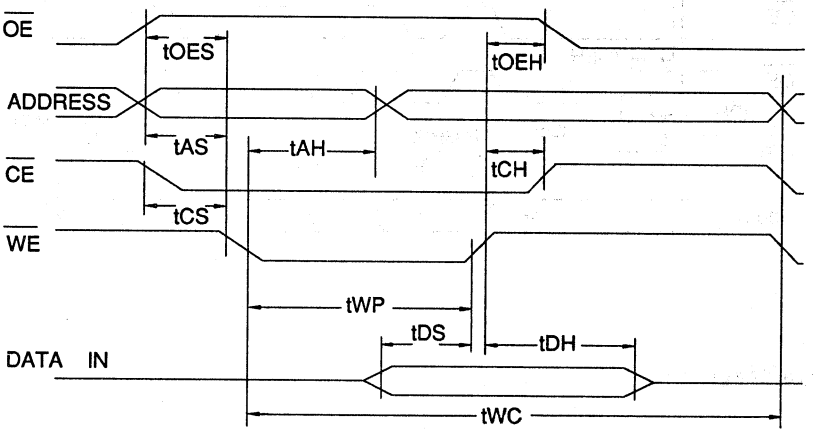
Output Test Load



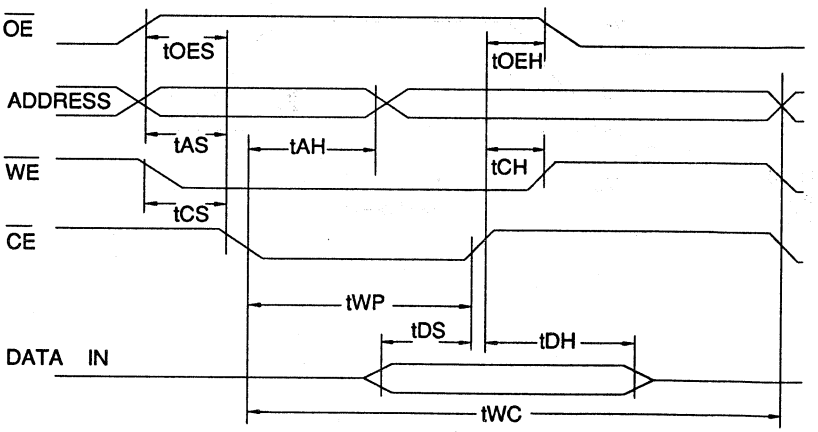
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{WC}	Write Cycle Time	AT28C04		0.5	1.0	ms
		AT28C04E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

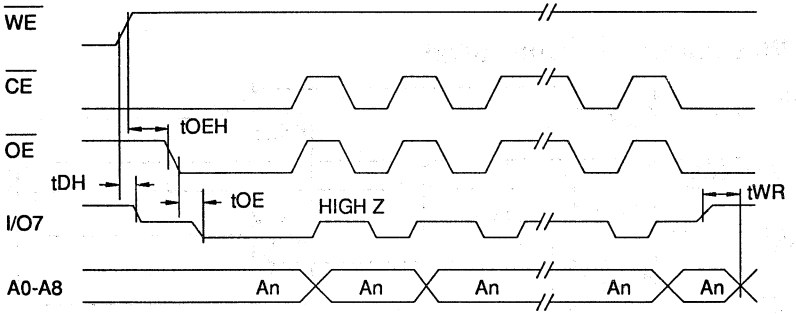


$\overline{\text{Data}}$ Polling Characteristics[1]

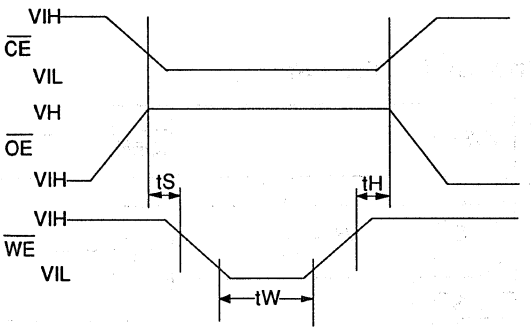
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

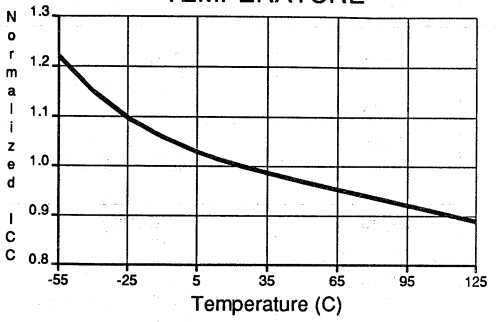


Chip Erase Waveforms

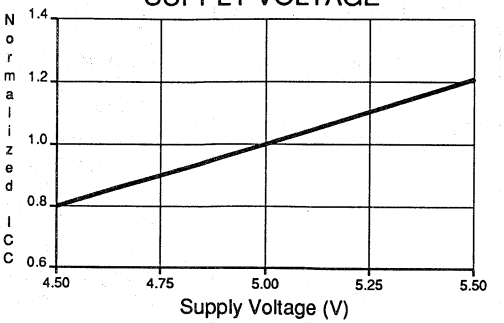


$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

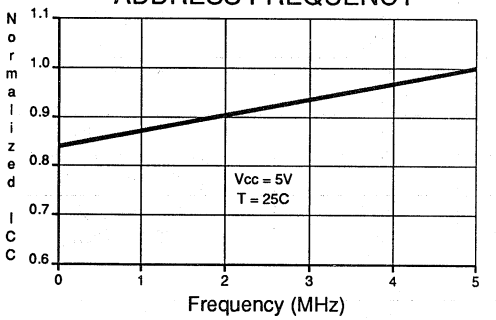
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



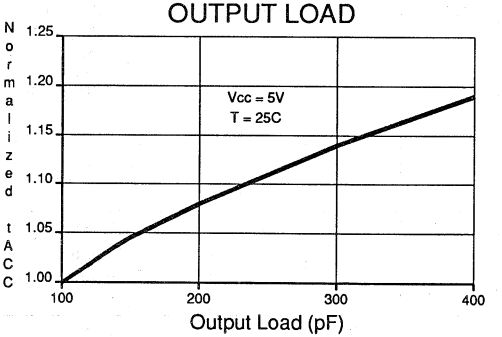
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



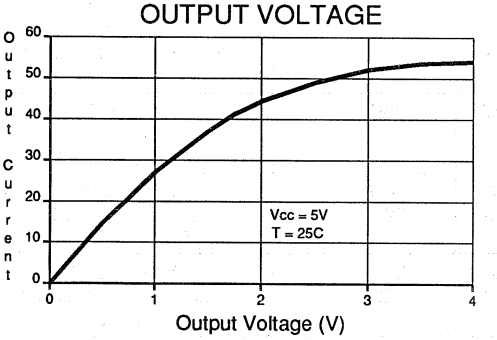
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



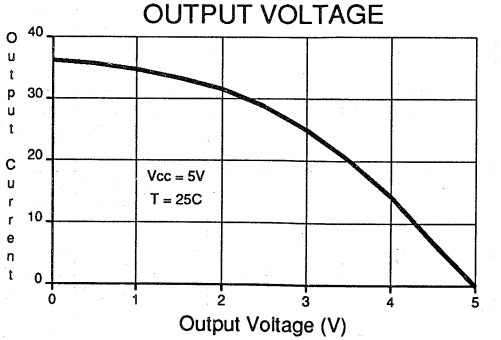
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C04(E,F)-15DC AT28C04(E,F)-15LC AT28C04(E,F)-15PC	24D6 32L 24P6	Commercial (0°C to 70°C)
150	45	0.1	AT28C04(E,F)-15DI AT28C04(E,F)-15LI AT28C04(E,F)-15PI	24D6 32L 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-15DM AT28C04(E,F)-15LM	24D6 32L	Military (-55°C to 125°C)
			AT28C04(E,F)-15DM/883 AT28C04(E,F)-15LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C04(E,F)-20DC AT28C04(E,F)-20LC AT28C04(E,F)-20PC	24D6 32L 24P6	Commercial (0°C to 70°C)
200	45	0.1	AT28C04(E,F)-20DI AT28C04(E,F)-20LI AT28C04(E,F)-20PI	24D6 32L 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-20DM AT28C04(E,F)-20LM	24D6 32L	Military (-55°C to 125°C)
			AT28C04(E,F)-20DM/883 AT28C04(E,F)-20LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C04(E,F)-25DC AT28C04(E,F)-25LC AT28C04(E,F)-25PC AT28C04-W	24D6 32L 24P6 DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C04(E,F)-25DI AT28C04(E,F)-25LI AT28C04(E,F)-25PI	24D6 32L 24P6	Industrial (-40°C to 85°C)
			AT28C04(E,F)-25DM AT28C04(E,F)-25LM	24D6 32L	Military (-55°C to 125°C)
			AT28C04(E,F)-25DM/883 AT28C04(E,F)-25LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C04(E,F)-30DM/883 AT28C04(E,F)-30LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C04(E,F)-35DM/883 AT28C04(E,F)-35LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C04(E,F)-45DM/883 AT28C04(E,F)-45LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

16K (2K x 8) CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Fast Byte Write - 200µs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **DATA POLLING**
- **Low Power**
  - **30mA Active Current**
  - **100µA CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 cycles**
  - **Data Retention: 10 years**
- **5V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

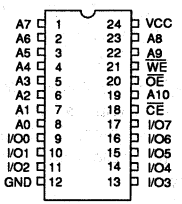
The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16k memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable non-volatile CMOS technology.

The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by DATA polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

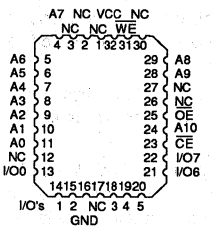
The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations

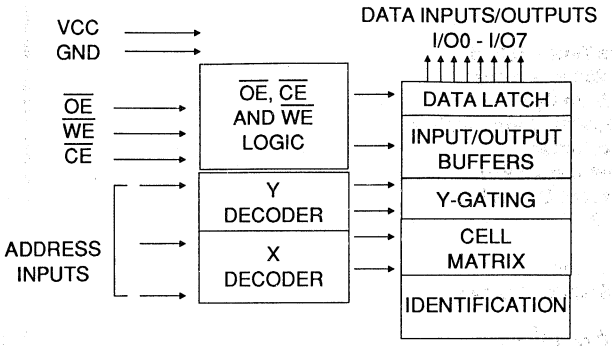


Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C16F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{DATA}$ POLLING: The AT28C16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C16-15	AT28C16-20	AT28C16-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f=5MHz; I_{OUT}=0mA $\overline{CE}$=V_{IL}	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-400µA		2.4		V

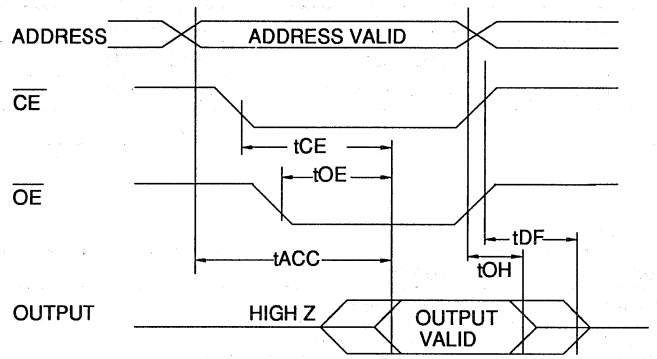
Pin Capacitance (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

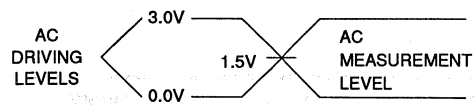
Symbol	Parameter	AT28C16-15		AT28C16-20		AT28C16-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



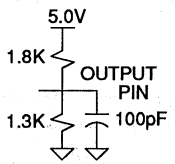
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

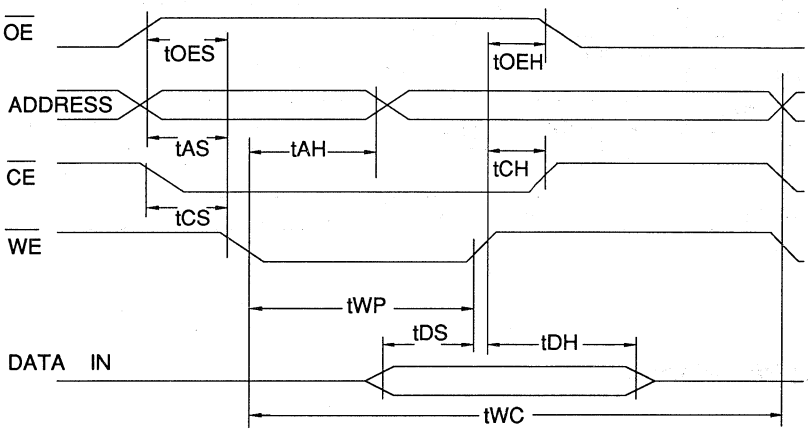
Output Test Load



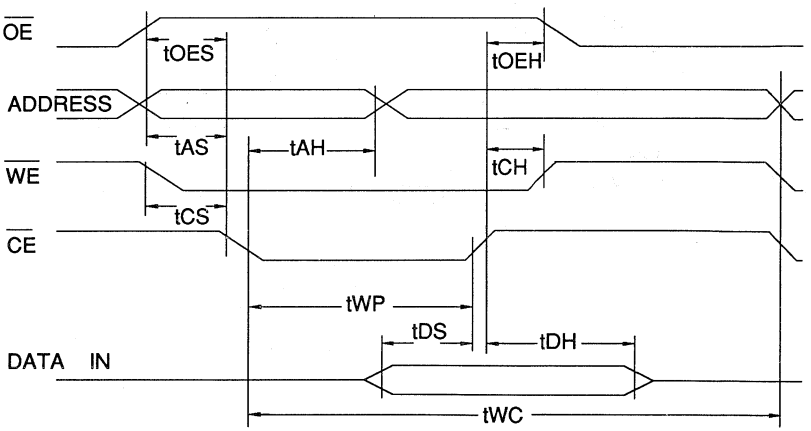
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{WC}	Write Cycle Time	AT28C16		0.5	1.0	ms
		AT28C16E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

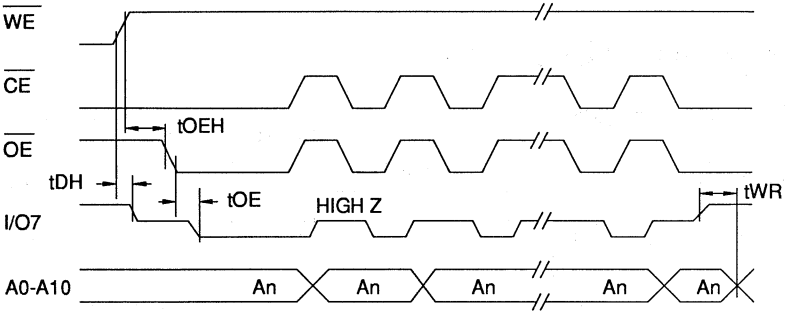


$\overline{\text{Data}}$ Polling Characteristics[1]

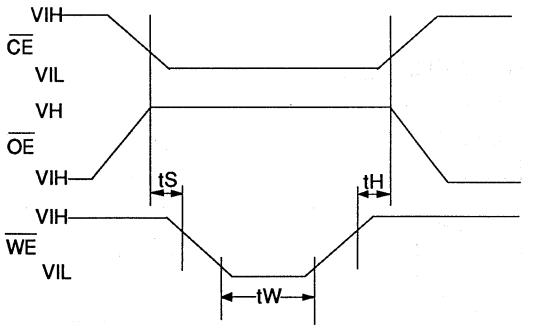
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

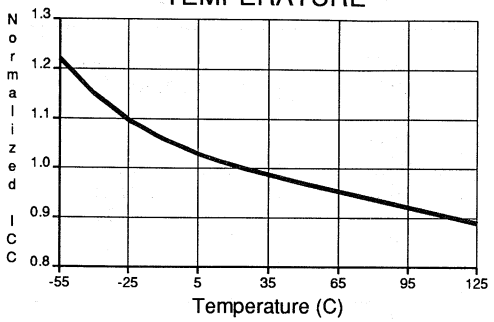


Chip Erase Waveforms

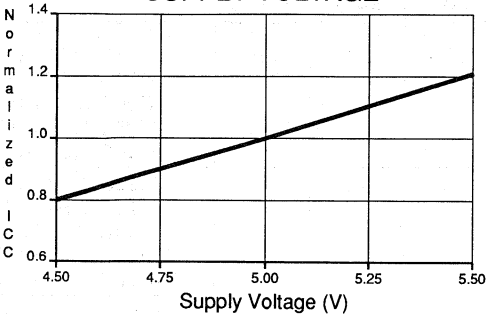


$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

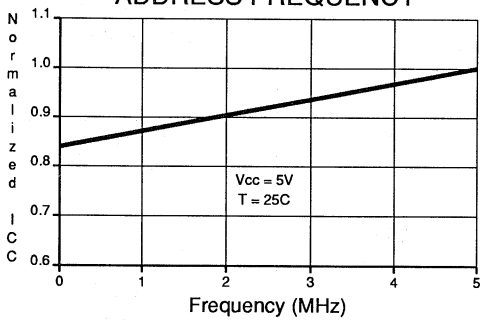
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



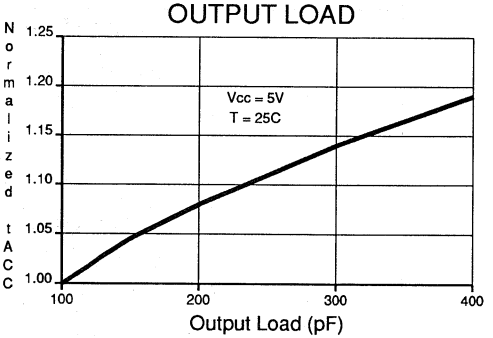
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



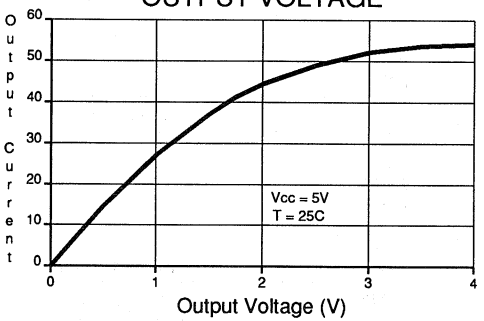
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



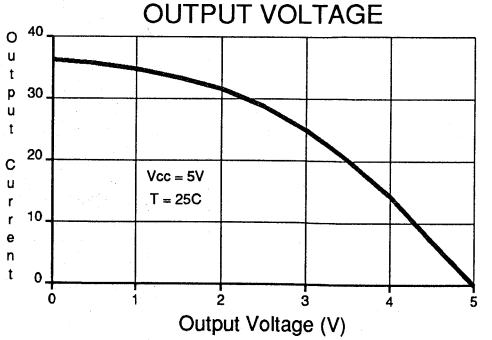
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16(E,F)-15DC AT28C16(E,F)-15JC AT28C16(E,F)-15LC AT28C16(E,F)-15PC AT28C16(E,F)-15SC	24D6 32J 32L 24P6 24S	Commercial (0°C to 70°C)
150	45	0.1	AT28C16(E,F)-15DI AT28C16(E,F)-15JI AT28C16(E,F)-15LI AT28C16(E,F)-15PI AT28C16(E,F)-15SI	24D6 32J 32L 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-15DM AT28C16(E,F)-15LM	24D6 32L	Military (-55°C to 125°C)
			AT28C16(E,F)-15DM/883 AT28C16(E,F)-15LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C16(E,F)-20DC AT28C16(E,F)-20JC AT28C16(E,F)-20LC AT28C16(E,F)-20PC AT28C16(E,F)-20SC	24D6 32J 32L 24P6 24S	Commercial (0°C to 70°C)
200	45	0.1	AT28C16(E,F)-20DI AT28C16(E,F)-20JI AT28C16(E,F)-20LI AT28C16(E,F)-20PI AT28C16(E,F)-20SI	24D6 32J 32L 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-20DM AT28C16(E,F)-20LM	24D6 32L	Military (-55°C to 125°C)
			AT28C16(E,F)-20DM/883 AT28C16(E,F)-20LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C16(E,F)-25DC AT28C16(E,F)-25JC AT28C16(E,F)-25LC AT28C16(E,F)-25PC AT28C16(E,F)-25SC AT28C16-W	24D6 32J 32L 24P6 24S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C16(E,F)-25DI AT28C16(E,F)-25JI AT28C16(E,F)-25LI AT28C16(E,F)-25PI AT28C16(E,F)-25SI	24D6 32J 32L 24P6 24S	Industrial (-40°C to 85°C)
			AT28C16(E,F)-25DM AT28C16(E,F)-25LM	24D6 32L	Military (-55°C to 125°C)
			AT28C16(E,F)-25DM/883 AT28C16(E,F)-25LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
300	45	0.1	AT28C16(E,F)-30DM/883 AT28C16(E,F)-30LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C16(E,F)-35DM/883 AT28C16(E,F)-35LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C16(E,F)-45DM/883 AT28C16(E,F)-45LM/883	24D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

16K (2K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 45ns
- Fast Byte Write - 1ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
- Low Power
  - 80mA Active Current
  - 500µA CMOS Standby Current (28HC16L)
- High Reliability CMOS Technology
  - Endurance: 10^4 cycles
  - Data Retention: 10 years
- 5 V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

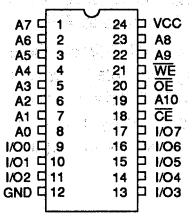
The AT28HC16/16L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. The device is optimized for high speed applications, featuring access times to 45ns. Its 16k of memory is organized as 2,048 words by 8 bits. The AT28HC16/16L comes in a space saving 24 pin DIP.

The AT28HC16/16L is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device being written will go to a busy state and automatically clear and write the latched data using an internal control timer. Data polling of I/O7 may be used to detect the end of the write cycle. Once a write cycle has been completed, a new access for a read or a write may begin immediately.

Atmel's high-speed CMOS technology is used to achieve access times of 45ns for the AT28HC16 with under 440mW of power dissipation. The AT28HC16L offers ultra low standby power consumption of under 2.75mW at access time to 55ns.

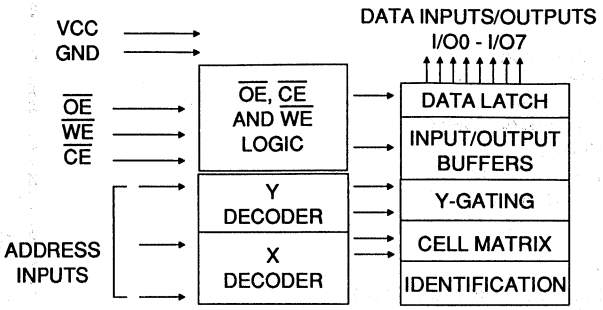
The AT28HC16/16L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and for improved data retention characteristics. An extra 16 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations



Pin Name	Function
A0 - A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28HC16/16L is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28HC16/16L is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

$\overline{DATA}$ POLLING: The AT28HC16/16L provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles. (d) Noise Protection— a $\overline{WE}$ or $\overline{CE}$ pulse of less than 10ns (typical) will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC16/16L may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: In the AT28HC16/16L there are an extra 16 bytes of E^2PROM memory available to the user for device identification. By raising A9 to $12 \pm 0.5V$ and using address locations 7F0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28HC16-45	AT28HC16L-55	AT28HC16-55	AT28HC16-70 AT28HC16L-70	AT28HC16-90 AT28HC16L-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-0.3V to V_{CC} + 1.0V	(AT28HC16L)		500	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1.0V	AT28HC16L		3	mA
			AT28HC16		60	mA
I_{CC}	V_{CC} Active Current A.C.	f=10MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=12mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4		V

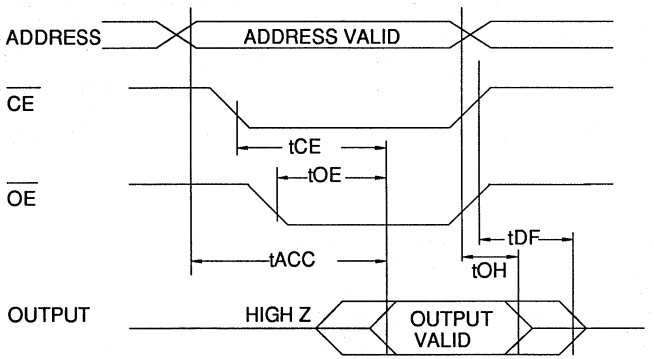
Pin Capacitance (f=1MHz T=25°C) [5]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics [1]

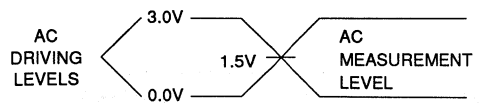
Symbol	Parameter	AT28HC16 -45		AT28HC16 -55		AT28HC16L -55		AT28HC16 -70		AT28HC16L -70		AT28HC16L -90		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		45		55		55		70		70		90	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay		30		40		55		50		70		90	ns
t_{OE} [3]	$\overline{OE}$ to Output Delay	0	30	0	40	0	40	0	50	0	50	0	50	ns
t_{DF} [4,5]	$\overline{OE}$ to Output Float	0	30	0	40	0	40	0	50	0	50	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$ or Address, whichever occurred first	0		0		0		0		0		0		ns

A.C. Read Waveforms



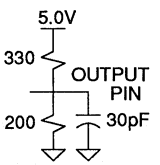
Notes:
1. C_L = 30pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

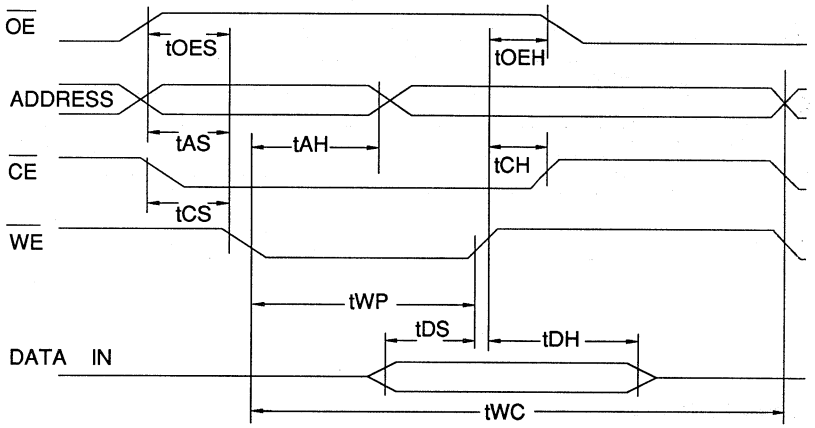
Output Test Load



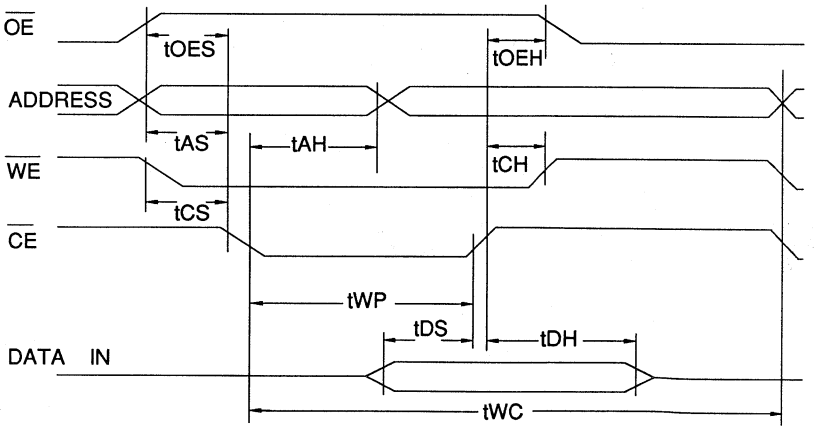
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{WC}	Write Cycle Time		0.5	1.0	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

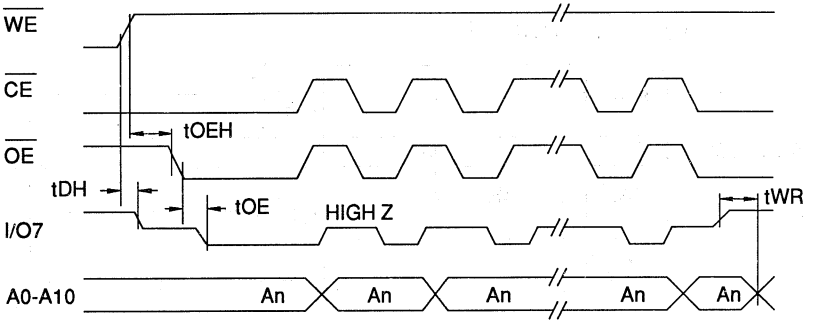


$\overline{\text{Data}}$ Polling Characteristics[1]

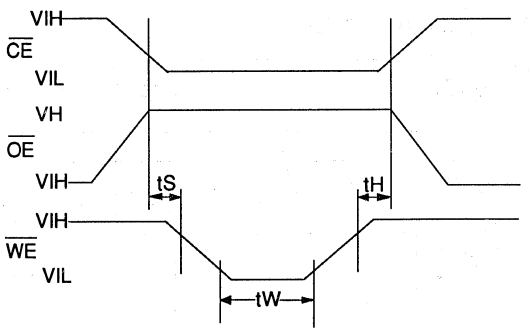
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

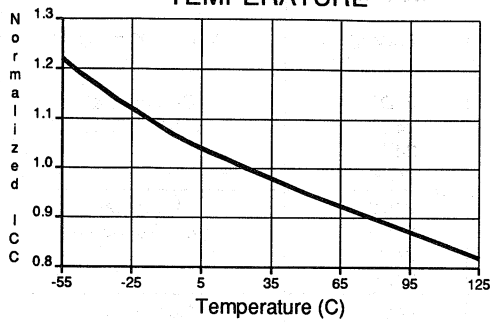


Chip Erase Waveforms

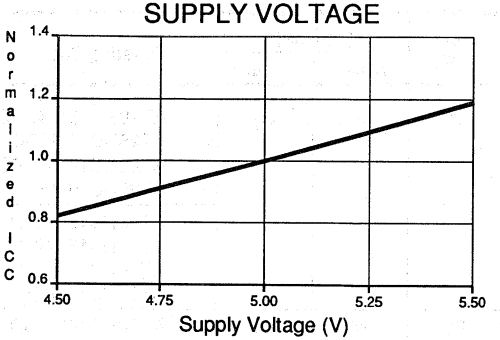


$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

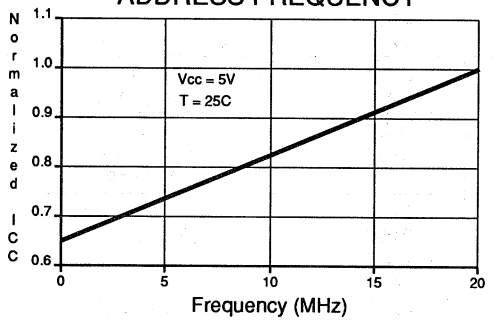
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

(Contact Factory: Not recommended for new designs.)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	60	AT28HC16N-45DC AT28HC16-45DC AT28HC16N-45PC AT28HC16-45PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-45DI AT28HC16-45DI AT28HC16N-45PI AT28HC16-45PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
55	80	60	AT28HC16N-55DC AT28HC16-55DC AT28HC16N-55PC AT28HC16-55PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-55DI AT28HC16-55DI AT28HC16N-55PI AT28HC16-55PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16N-55DM AT28HC16-55DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-55DM/883 AT28HC16-55DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
70	80	60	AT28HC16N-70DC AT28HC16-70DC AT28HC16N-70PC AT28HC16-70PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-70DI AT28HC16-70DI AT28HC16N-70PI AT28HC16-70PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16N-70DM AT28HC16-70DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-70DM/883 AT28HC16-70DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
90	80	60	AT28HC16N-90DC AT28HC16-90DC AT28HC16N-90PC AT28HC16-90PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16N-90DI AT28HC16-90DI AT28HC16N-90PI AT28HC16-90PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)

Ordering Information

(Contact Factory: Not recommended for new designs.)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	60	AT28HC16N-90DM AT28HC16-90DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16N-90DM/883 AT28HC16-90DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)

Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

(Contact Factory: Not recommended for new designs.)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	0.5	AT28HC16LN-55DC AT28HC16L-55DC AT28HC16LN-55PC AT28HC16L-55PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16LN-55DI AT28HC16L-55DI AT28HC16LN-55PI AT28HC16L-55PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-55DM AT28HC16L-55DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-55DM/883 AT28HC16L-55DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
70	80	0.5	AT28HC16LN-70DC AT28HC16L-70DC AT28HC16LN-70PC AT28HC16L-70PC	24D3 24D6 24P3 24P6	Commercial (0°C to 70°C)
			AT28HC16LN-70DI AT28HC16L-70DI AT28HC16LN-70PI AT28HC16L-70PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-70DM AT28HC16L-70DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-70DM/883 AT28HC16L-70DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)
90	80	0.5	AT28HC16LN-90DC AT28HC16L-90DC AT28HC16LN-90PC AT28HC16L-90PC AT28HC16L-W	24D3 24D6 24P3 24P6 DIE	Commercial (0°C to 70°C)
			AT28HC16LN-90DI AT28HC16L-90DI AT28HC16LN-90PI AT28HC16L-90PI	24D3 24D6 24P3 24P6	Industrial (-40°C to 85°C)
			AT28HC16LN-90DM AT28HC16L-90DM	24D3 24D6	Military (-55°C to 125°C)
			AT28HC16LN-90DM/883 AT28HC16L-90DM/883	24D3 24D6	Military with Burn-In (-55°C to 125°C)

Ordering Information

(Contact Factory: Not recommended for new designs.)

Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die

16K (2K x 8) CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Fast Byte Write - 200µs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ POLLING**
  - **READY/$\overline{\text{BUSY}}$ Open Drain Output**
- **Low Power**
  - **30mA Active Current**
  - **100µa CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 cycles**
  - **Data Retention: 10 years**
- **5 V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

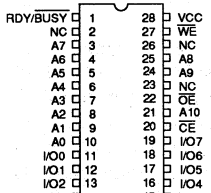
The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16k memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable non-volatile CMOS technology.

The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

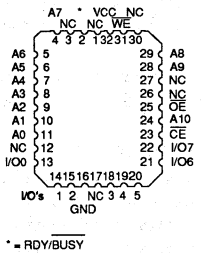
The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100µA.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations

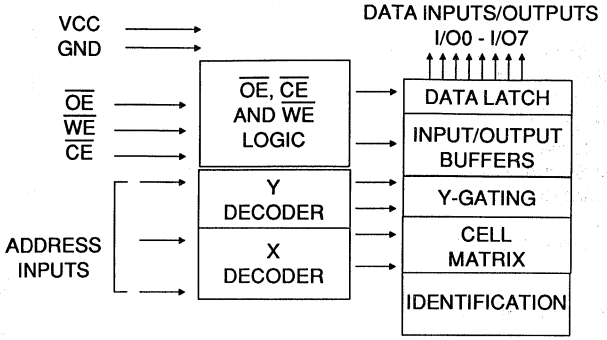


Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BUSY}}$	Ready/$\overline{\text{Busy}}$ Output
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28C17 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C17F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line.

$\overline{DATA}$ POLLING: The AT28C17 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to Vcc +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28C17-15	AT28C17-20	AT28C17-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to Vcc + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to Vcc			10	µA
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$=Vcc-0.3V to Vcc + 1.0V			100	µA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$=2.0V to Vcc + 1.0V	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	Vcc Active Current A.C.	f=5MHz; I_{OUT}=0mA $\overline{CE}$=V_{IL}	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA =4.0 for RDY/$\overline{BUSY}$			.4	V
V_{OH}	Output High Voltage	I_{OH}=-400µA		2.4		V

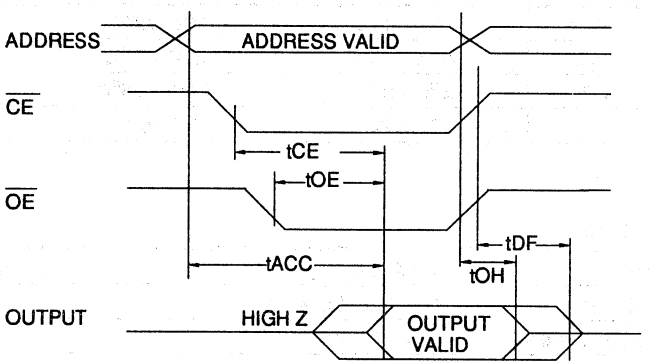
Pin Capacitance (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

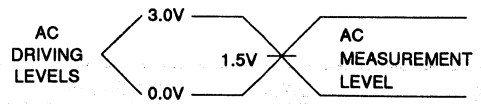
Symbol	Parameter	AT28C17-15		AT28C17-20		AT28C17-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



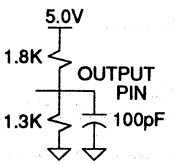
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

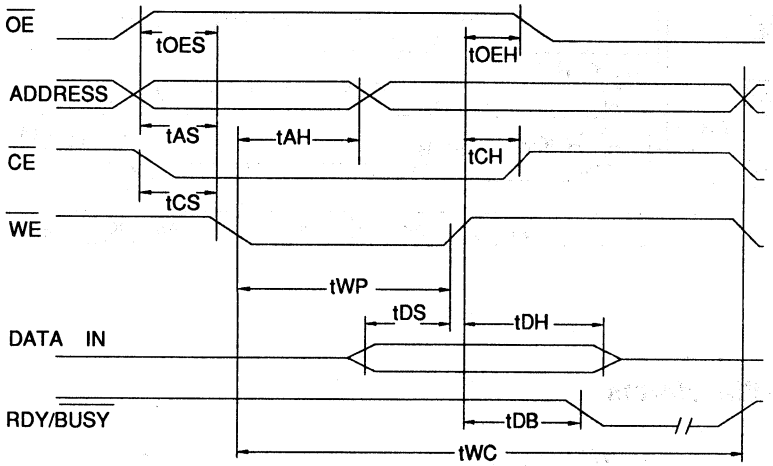
Output Test Load



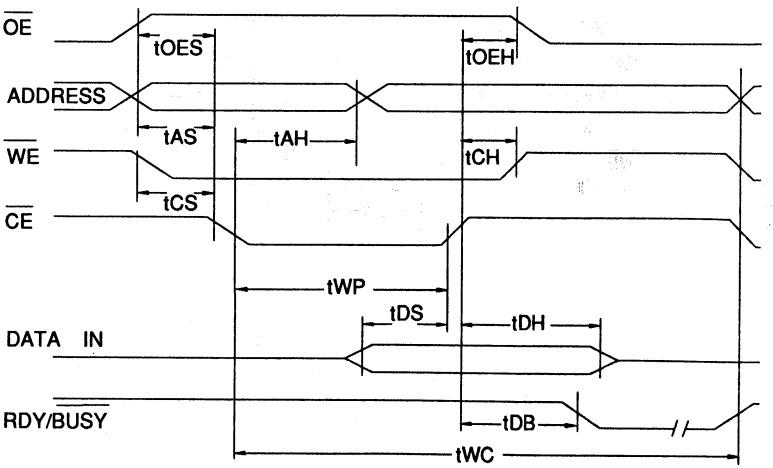
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{DB}	Time to Device Busy				50	ns
t_{WC}	Write Cycle Time	AT28C17		0.5	1.0	ms
		AT28C17E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

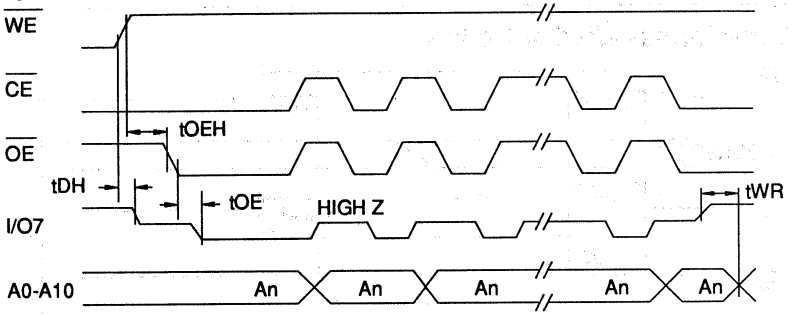


$\overline{\text{Data}}$ Polling Characteristics[1]

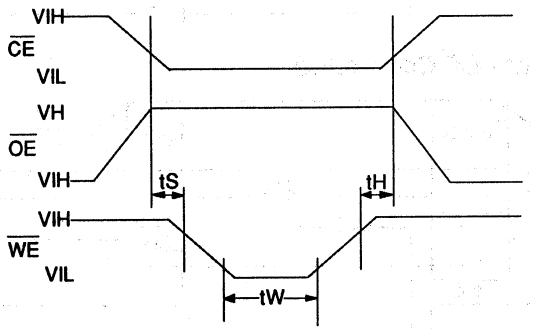
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

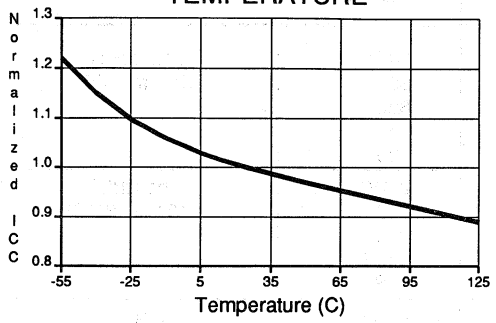


Chip Erase Waveforms

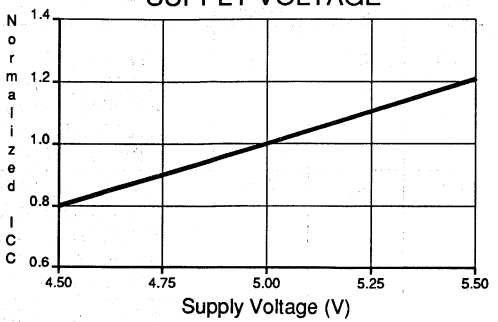


$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

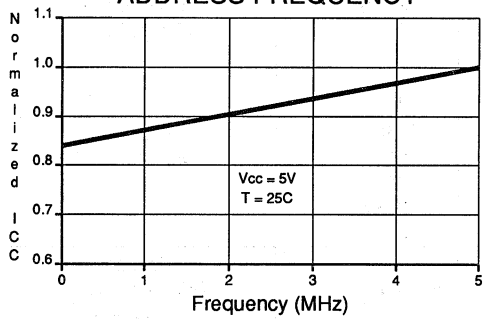
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



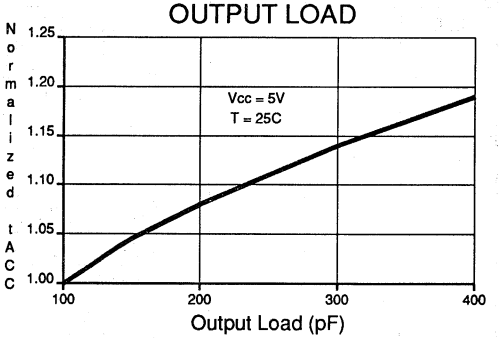
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



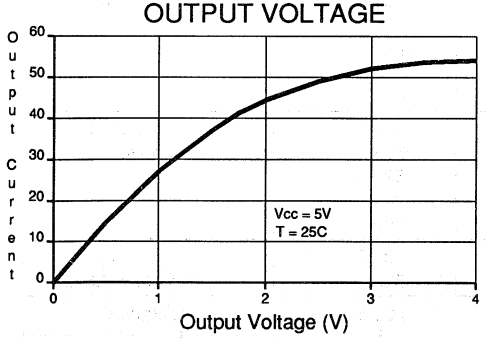
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



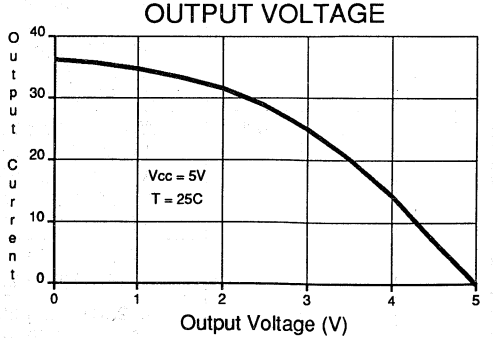
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E,F)-15DC AT28C17(E,F)-15JC AT28C17(E,F)-15LC AT28C17(E,F)-15PC AT28C17(E,F)-15SC	28D6 32J 32L 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C17(E,F)-15DI AT28C17(E,F)-15JI AT28C17(E,F)-15LI AT28C17(E,F)-15PI AT28C17(E,F)-15SI	28D6 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-15DM AT28C17(E,F)-15LM	28D6 32L	Military (-55°C to 125°C)
			AT28C17(E,F)-15DM/883 AT28C17(E,F)-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C17(E,F)-20DC AT28C17(E,F)-20JC AT28C17(E,F)-20LC AT28C17(E,F)-20PC AT28C17(E,F)-20SC	28D6 32J 32L 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C17(E,F)-20DI AT28C17(E,F)-20JI AT28C17(E,F)-20LI AT28C17(E,F)-20PI AT28C17(E,F)-20SI	28D6 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-20DM AT28C17(E,F)-20LM	28D6 32L	Military (-55°C to 125°C)
			AT28C17(E,F)-20DM/883 AT28C17(E,F)-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C17(E,F)-25DC AT28C17(E,F)-25JC AT28C17(E,F)-25LC AT28C17(E,F)-25PC AT28C17(E,F)-25SC AT28C17-W	28D6 32J 32L 28P6 28S DIE	Commercial (0°C to 70°C)
250	45	0.1	AT28C17(E,F)-25DI AT28C17(E,F)-25JI AT28C17(E,F)-25LI AT28C17(E,F)-25PI AT28C17(E,F)-25SI	28D6 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C17(E,F)-25DM AT28C17(E,F)-25LM	28D6 32L	Military (-55°C to 125°C)
			AT28C17(E,F)-25DM/883 AT28C17(E,F)-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
300	45	0.1	AT28C17(E,F)-30DM/883 AT28C17(E,F)-30LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C17(E,F)-35DM/883 AT28C17(E,F)-35LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C17(E,F)-45DM/883 AT28C17(E,F)-45LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

64K (8K x 8) CMOS E^2PROM

Features

- Fast Read Access Time - 150ns
- Fast Byte Write - 200µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - READY/BUSY Open Drain Output
  - DATA Polling
- Low Power
  - 30mA Active Current
  - 100µA CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

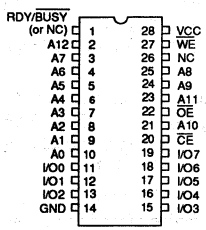
The AT28C64 is a low-power, high-performance 8,192 words x 8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with Atmel's reliable non-volatile technology.

The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/BUSY (unless pin 1 is N.C.) and DATA polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

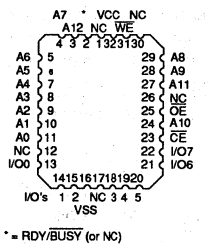
The CMOS technology offers fast access times of 150ns at low power dissipation. When the chip is deselected the standby current is less than 100µA.

Atmel's 28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E^2PROM are available for device identification or tracking.

Pin Configurations

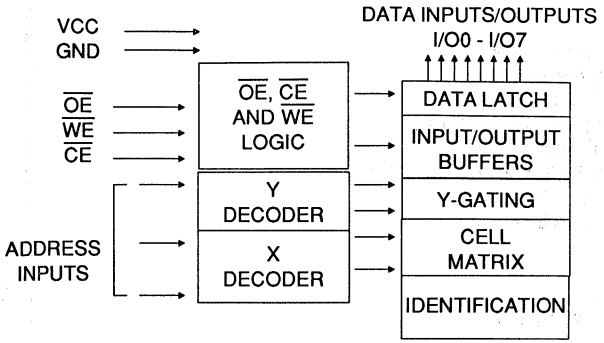


Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{Busy}$ Output
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28C64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

FAST BYTE WRITE: The AT28C64F offers a byte write time of 200µs maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

READY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line. Pin 1 is not connected for the AT28C64X.

$\overline{DATA}$ POLLING: The AT28C64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to $12 \pm 0.5V$ and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to VCC +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28C64-15	AT28C64-20	AT28C64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to VCC + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to VCC			10	µA
I_{SB1}	VCC Standby Current CMOS	$\overline{CE}$=VCC-0.3V to VCC + 1.0V			100	µA
I_{SB2}	VCC Standby Current TTL	$\overline{CE}$=2.0V to VCC + 1.0V	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	VCC Active Current A.C.	f=5MHz; I_{OUT}=0mA $\overline{CE}$=V_{IL}	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA =4.0mA for RDY/$\overline{BUSY}$			.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA		2.4		V

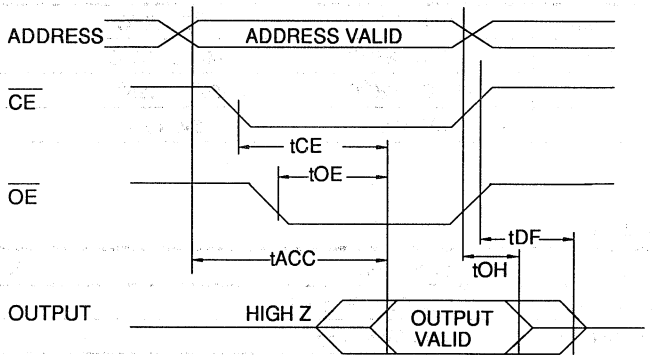
Pin Capacitance (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics

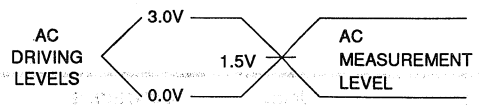
Symbol	Parameter	AT28C64-15		AT28C64-20		AT28C64-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



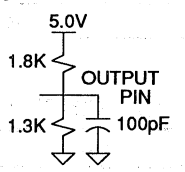
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20ns

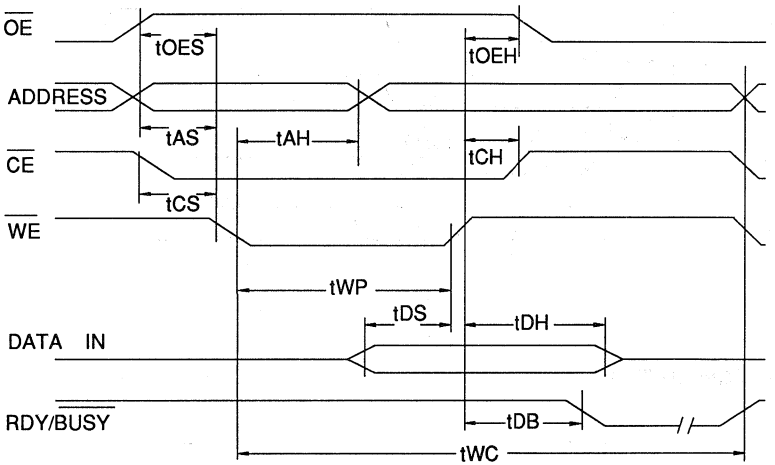
Output Test Load



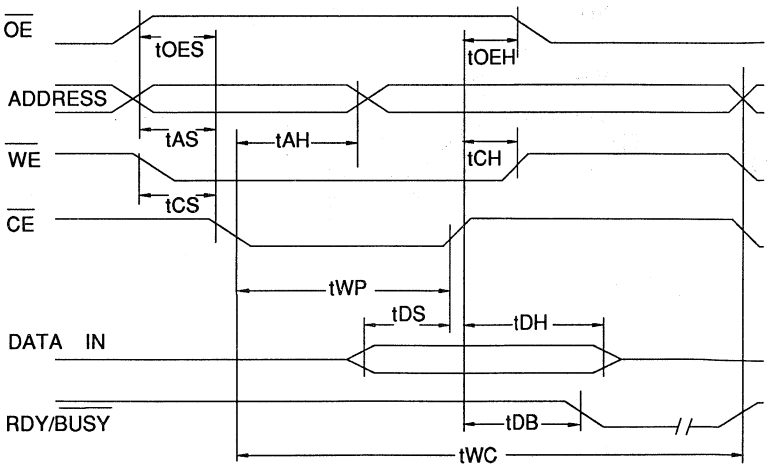
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{DB}	Time to Device Busy				50	ns
t_{WC}	Write Cycle Time	AT28C64		0.5	1.0	ms
		AT28C64E/F		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

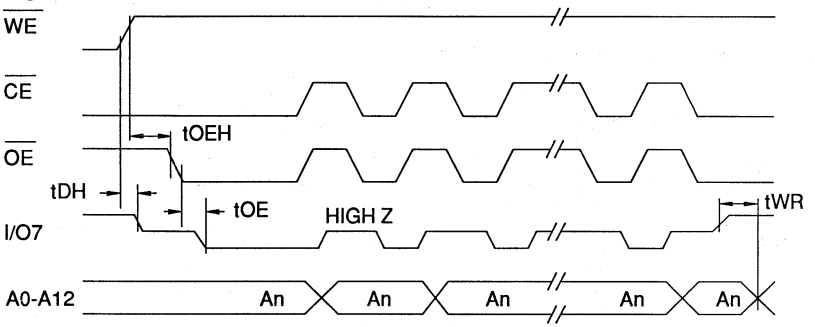


$\overline{\text{Data}}$ Polling Characteristics[1]

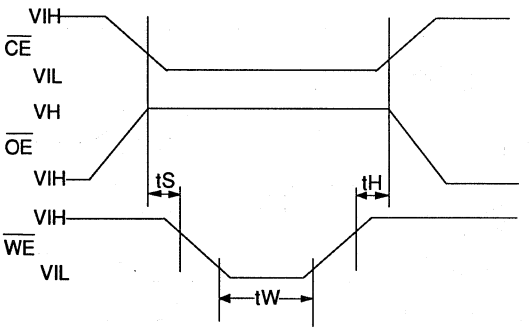
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

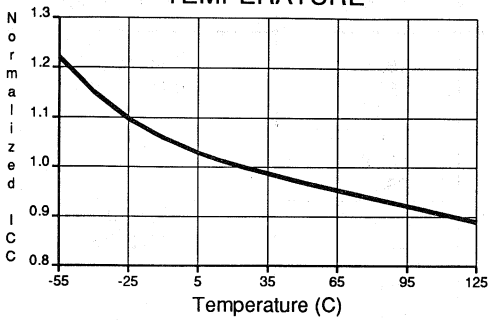


Chip Erase Waveforms

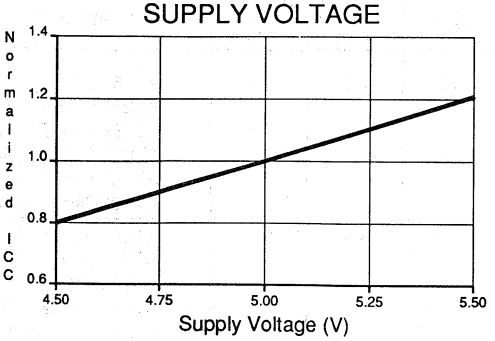


$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

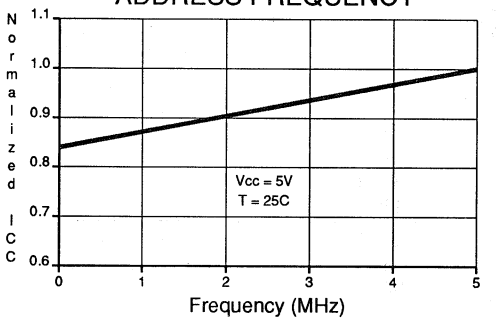
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



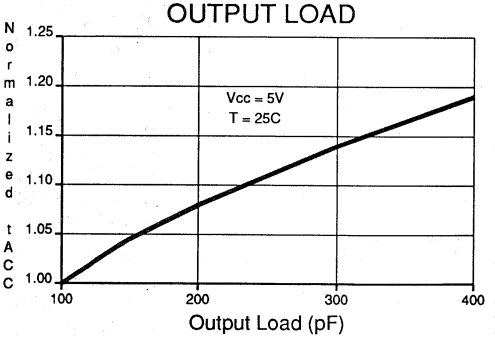
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



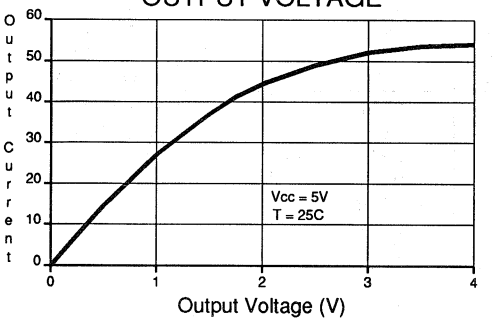
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



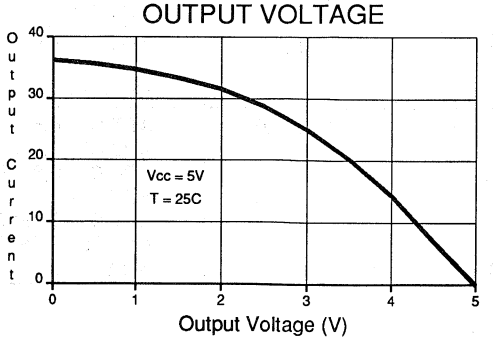
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64(E,F)-15DC AT28C64(E,F)-15FC AT28C64(E,F)-15JC AT28C64(E,F)-15LC AT28C64(E,F)-15PC AT28C64(E,F)-15SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C64(E,F)-15DI AT28C64(E,F)-15FI AT28C64(E,F)-15JI AT28C64(E,F)-15LI AT28C64(E,F)-15PI AT28C64(E,F)-15SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-15DM AT28C64(E,F)-15FM AT28C64(E,F)-15LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64(E,F)-15DM/883 AT28C64(E,F)-15FM/883 AT28C64(E,F)-15LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C64(E,F)-20DC AT28C64(E,F)-20FC AT28C64(E,F)-20JC AT28C64(E,F)-20LC AT28C64(E,F)-20PC AT28C64(E,F)-20SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C64(E,F)-20DI AT28C64(E,F)-20FI AT28C64(E,F)-20JI AT28C64(E,F)-20LI AT28C64(E,F)-20PI AT28C64(E,F)-20SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-20DM AT28C64(E,F)-20FM AT28C64(E,F)-20LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64(E,F)-20DM/883 AT28C64(E,F)-20FM/883 AT28C64(E,F)-20LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C64(E,F)-25DC AT28C64(E,F)-25FC AT28C64(E,F)-25JC AT28C64(E,F)-25LC AT28C64(E,F)-25PC AT28C64(E,F)-25SC AT28C64-W	28D6 28F 32J 32L 28P6 28S DIE	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	45	0.1	AT28C64(E,F)-25DI AT28C64(E,F)-25FI AT28C64(E,F)-25JI AT28C64(E,F)-25LI AT28C64(E,F)-25PI AT28C64(E,F)-25SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64(E,F)-25DM AT28C64(E,F)-25FM AT28C64(E,F)-25LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64(E,F)-25DM/883 AT28C64(E,F)-25FM/883 AT28C64(E,F)-25LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C64(E,F)-30DM/883 AT28C64(E,F)-30FM/883 AT28C64(E,F)-30LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C64(E,F)-35DM/883 AT28C64(E,F)-35FM/883 AT28C64(E,F)-35LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C64(E,F)-45DM/883 AT28C64(E,F)-45FM/883 AT28C64(E,F)-45LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	45	0.1	5962-87514 17 UX 5962-87514 17 XX 5962-87514 17 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	45	0.1	5962-87514 16 UX 5962-87514 16 XX 5962-87514 16 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	45	0.1	5962-87514 15 UX 5962-87514 15 XX 5962-87514 15 YX 5962-87514 15 ZX	32K 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	5962-87514 14 UX 5962-87514 14 XX 5962-87514 14 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	5962-87514 13 UX 5962-87514 13 XX 5962-87514 13 YX 5962-87514 13 ZX	32K 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs
F	Fast Write Option: Write Time = 200 µs

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C64X-15DC AT28C64X-15FC AT28C64X-15JC AT28C64X-15LC AT28C64X-15PC AT28C64X-15SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
150	45	0.1	AT28C64X-15DI AT28C64X-15FI AT28C64X-15JI AT28C64X-15LI AT28C64X-15PI AT28C64X-15SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-15DM AT28C64X-15FM AT28C64X-15LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64X-15DM/883 AT28C64X-15FM/883 AT28C64X-15LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C64X-20DC AT28C64X-20FC AT28C64X-20JC AT28C64X-20LC AT28C64X-20PC AT28C64X-20SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)
200	45	0.1	AT28C64X-20DI AT28C64X-20FI AT28C64X-20JI AT28C64X-20LI AT28C64X-20PI AT28C64X-20SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-20DM AT28C64X-20FM AT28C64X-20LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64X-20DM/883 AT28C64X-20FM/883 AT28C64X-20LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C64X-25DC AT28C64X-25FC AT28C64X-25JC AT28C64X-25LC AT28C64X-25PC AT28C64X-25SC	28D6 28F 32J 32L 28P6 28S	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	45	0.1	AT28C64X-25DI AT28C64X-25FI AT28C64X-25JI AT28C64X-25LI AT28C64X-25PI AT28C64X-25SI	28D6 28F 32J 32L 28P6 28S	Industrial (-40°C to 85°C)
			AT28C64X-25DM AT28C64X-25FM AT28C64X-25LM	28D6 28F 32L	Military (-55°C to 125°C)
			AT28C64X-25DM/883 AT28C64X-25FM/883 AT28C64X-25LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	AT28C64X-30DM/883 AT28C64X-30FM/883 AT28C64X-30LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	AT28C64X-35DM/883 AT28C64X-35FM/883 AT28C64X-35LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
450	45	0.1	AT28C64X-45DM/883 AT28C64X-45FM/883 AT28C64X-45LM/883	28D6 28F 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	45	0.1	5962-87514 22 UX 5962-87514 22 XX 5962-87514 22 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	45	0.1	5962-87514 21 UX 5962-87514 21 XX 5962-87514 21 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	45	0.1	5962-87514 20 UX 5962-87514 20 XX 5962-87514 20 YX 5962-87514 20 ZX	32K 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	45	0.1	5962-87514 19 UX 5962-87514 19 XX 5962-87514 19 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	45	0.1	5962-87514 18 UX 5962-87514 18 XX 5962-87514 18 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

64K (8K x 8) High Speed CMOS E^2PROM

Features

- Fast Read Access Time - 55ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 32 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Maximum Page Write Cycle Time: 2ms
  - 1 to 32 Byte Page Write Operation
- Low Power Dissipation
  - 80mA Active Current
  - 100µA CMOS Standby Current (28HC64L)
- Direct Microprocessor Control
  - DATA Polling
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

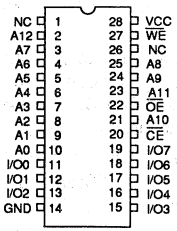
Description

The AT28HC64/L is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64k of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 55ns with power dissipation of just 440mW. When the device is deselected the standby current is less than 100µA.

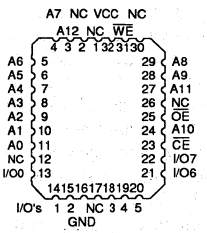
The AT28HC64/L is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC64/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28HC64/L also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Pin Configurations

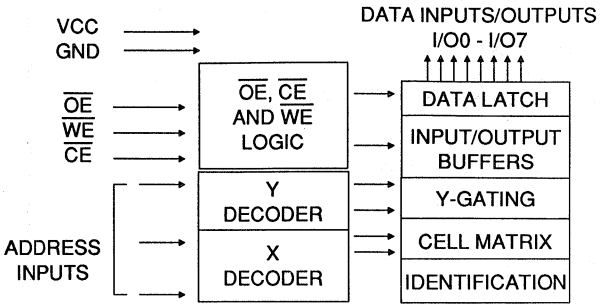


Pin Name	Function
A0 - A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Device Operation

READ: The AT28HC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28HC64 allows one to 32 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded, successive bytes may be loaded in the same manner. Each byte to be written must be loaded into the AT28HC64 within 150µs of the first byte. A5 to A12 determine the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A4 are used to specify which bytes within the page are to be written. All bytes to be written must share the same page address. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC64 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28HC64 may be set to the high state by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12+/-0.5V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28HC64-55	AT28HC64L-70	AT28HC64-70	AT28HC64-90 AT28HC64L-90	AT28HC64-12 AT28HC64L-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC} + 1V AT28HC64L	Com., Ind.		100	µA
			Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V	AT28HC64L		3	mA
			AT28HC64		60	mA
I_{CC}	V_{CC} Active Current	f=10MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=4mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4		V

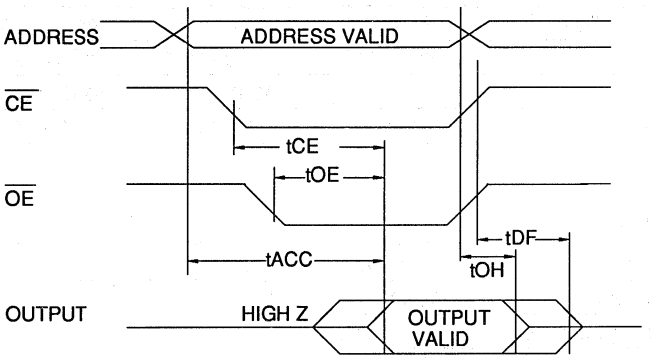
Pin Capacitance (f=1MHz T=25°C) [5]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Read Characteristics [1]

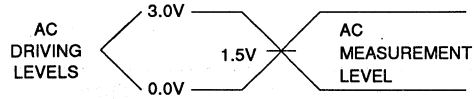
Symbol	Parameter	AT28HC64 -55		AT28HC64 -70		AT28HC64L -70		AT28HC64 -90		AT28HC64L -90		AT28HC64L -12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		55		70		70		90		90		120	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay		55		70		70		90		90		120	ns
t_{OE} [3]	$\overline{OE}$ to Output Delay	0	30	0	35	0	35	0	40	0	40	0	50	ns
t_{DF} [4,5]	$\overline{OE}$ to Output Float	0	30	0	35	0	35	0	40	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		0		0		ns

A.C. Read Waveforms



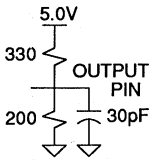
Notes:
1. C_L = 30pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

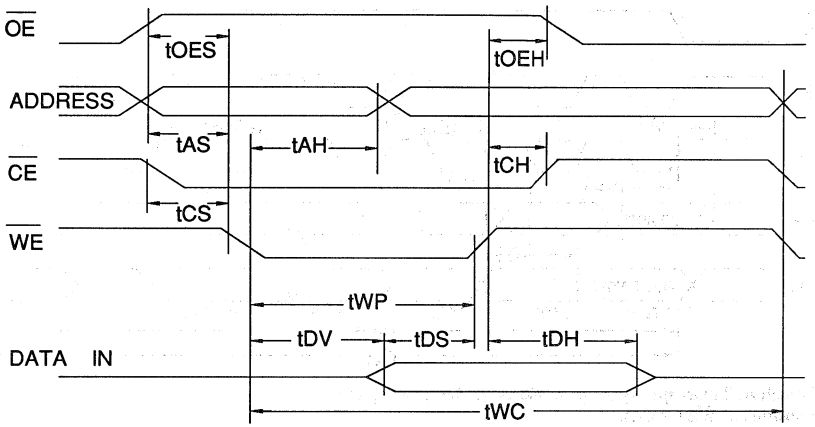
Output Test Load



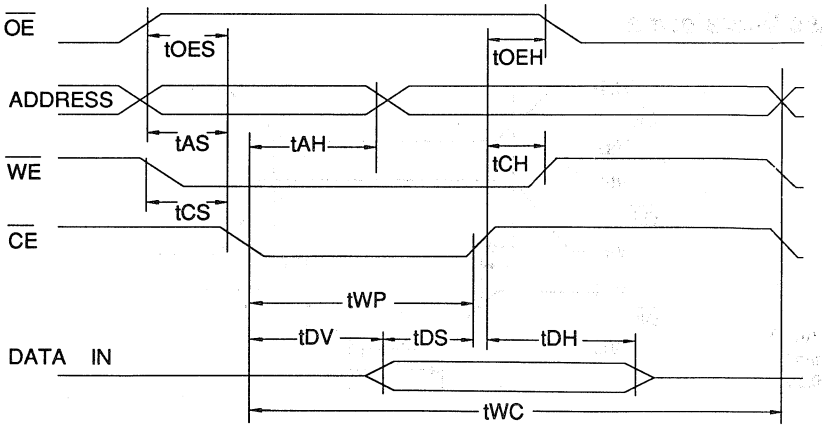
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{DV}	Time to Data Valid			1	µs
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



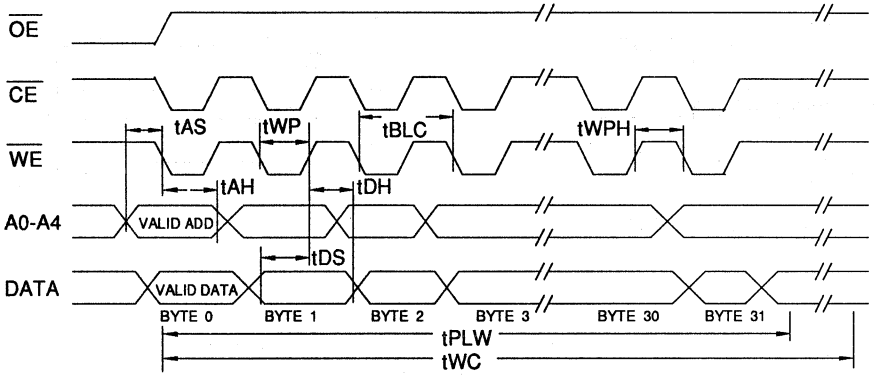
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Write Characteristics

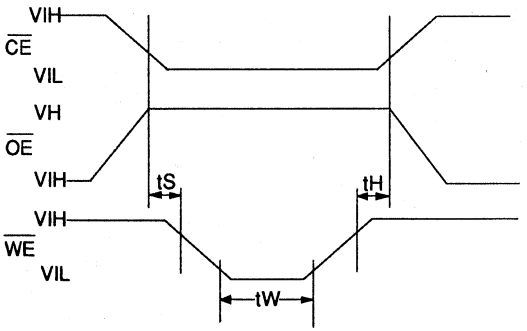
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Notes: A5 through A12 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



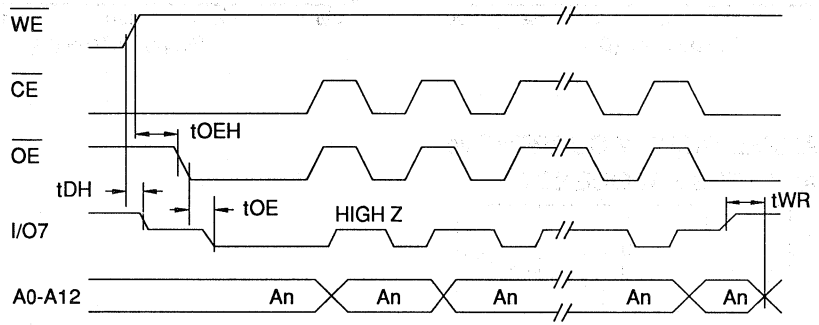
$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

$\overline{\text{Data}}$ Polling Characteristics[1]

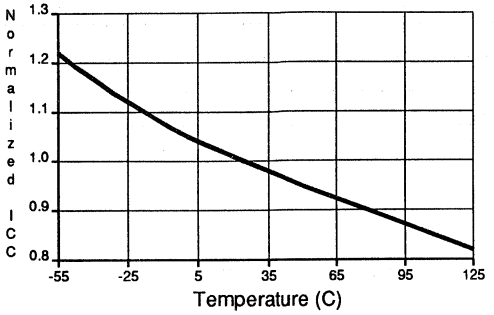
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

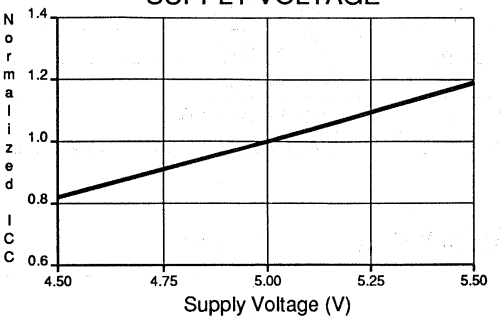
$\overline{\text{Data}}$ Polling Waveforms



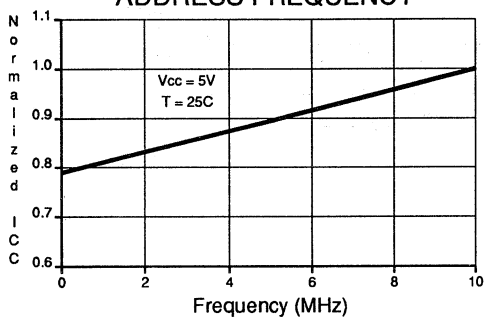
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	60	AT28HC64(E)-55DC AT28HC64(E)-55JC AT28HC64(E)-55LC AT28HC64(E)-55PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-55DI AT28HC64(E)-55JI AT28HC64(E)-55LI AT28HC64(E)-55PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
70	80	60	AT28HC64(E)-70DC AT28HC64(E)-70JC AT28HC64(E)-70LC AT28HC64(E)-70PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-70DI AT28HC64(E)-70JI AT28HC64(E)-70LI AT28HC64(E)-70PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-70DM AT28HC64(E)-70LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64(E)-70DM/883 AT28HC64(E)-70LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	60	AT28HC64(E)-90DC AT28HC64(E)-90JC AT28HC64(E)-90LC AT28HC64(E)-90PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-90DI AT28HC64(E)-90JI AT28HC64(E)-90LI AT28HC64(E)-90PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-90DM AT28HC64(E)-90LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64(E)-90DM/883 AT28HC64(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC64(E)-12DC AT28HC64(E)-12JC AT28HC64(E)-12LC AT28HC64(E)-12PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64(E)-12DI AT28HC64(E)-12JI AT28HC64(E)-12LI AT28HC64(E)-12PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
			AT28HC64(E)-12DM AT28HC64(E)-12LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64(E)-12DM/883 AT28HC64(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

Ordering Information

tACC (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	0.1	AT28HC64L(E)-70DC AT28HC64L(E)-70JC AT28HC64L(E)-70LC AT28HC64L(E)-70PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-70DI AT28HC64L(E)-70JI AT28HC64L(E)-70LI AT28HC64L(E)-70PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
90	80	0.1	AT28HC64L(E)-90DC AT28HC64L(E)-90JC AT28HC64L(E)-90LC AT28HC64L(E)-90PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC64L(E)-90DI AT28HC64L(E)-90JI AT28HC64L(E)-90LI AT28HC64L(E)-90PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
90	80	0.2	AT28HC64L(E)-90DM AT28HC64L(E)-90LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64L(E)-90DM/883 AT28HC64L(E)-90LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.1	AT28HC64L(E)-12DC AT28HC64L(E)-12JC AT28HC64L(E)-12LC AT28HC64L(E)-12PC AT28HC64L-W	28D6 32J 32L 28P6 DIE	Commercial (0°C to 70°C)
			AT28HC64L(E)-12DI AT28HC64L(E)-12JI AT28HC64L(E)-12LI AT28HC64L(E)-12PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
120	80	0.2	AT28HC64L(E)-12DM AT28HC64L(E)-12LM	28D6 32L	Military (-55°C to 125°C)
			AT28HC64L(E)-12DM/883 AT28HC64L(E)-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	80	0.2	5962-87514 12 UX 5962-87514 12 XX 5962-87514 12 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	0.2	5962-87514 11 UX 5962-87514 11 XX 5962-87514 11 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.2	5962-87514 10 UX 5962-87514 10 XX 5962-87514 10 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

64K (8K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 32 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Maximum Page Write Cycle Time: 2ms**
  - **1 to 32 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **100µA CMOS Standby Current**
- **Direct Microprocessor Control**
  - **DATA Polling**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

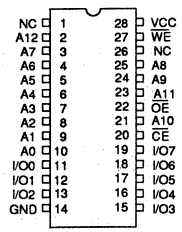
Description

The AT28PC64 is a high-speed, low-power Electrically Erasable and Programmable Read Only Memory. Its 64k of memory is organized as 8,192 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected the standby current is less than 100µA.

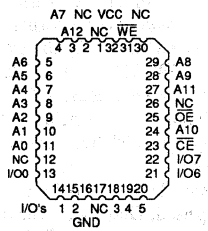
The AT28PC64 is accessed like a Static RAM for the read or write cycles without the need for external components. The device contains a 32-byte page register to allow writing of up to 32 bytes simultaneously. During a write cycle, the addresses and 1 to 32 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28PC64 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. The AT28PC64 also includes an extra 32 bytes of E^2PROM for device identification or tracking.

Pin Configurations

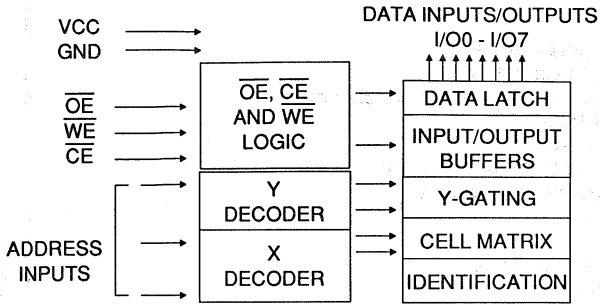


Pin Name	Function
A0 - A12	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

Description

READ: The AT28PC64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28PC64 allows one to 32 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded, successive bytes may be loaded in the same manner. Each byte to be written must be loaded into the AT28PC64 within 150µs of the first byte. A5 to A12 determine the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A4 are used to specify which bytes within the page are to be written. All bytes to be written must share the same page address. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28PC64 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28PC64 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

CHIP CLEAR: The contents of the entire memory of the AT28PC64 may be set to the high state by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10ms low pulse is applied to the $\overline{WE}$ pin.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to $12 \pm 0.5V$ and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28PC64-15	AT28PC64-20	AT28PC64-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC} + 1V	Com., Ind.		100	µA
			Mil.		200	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-400µA		2.4		V

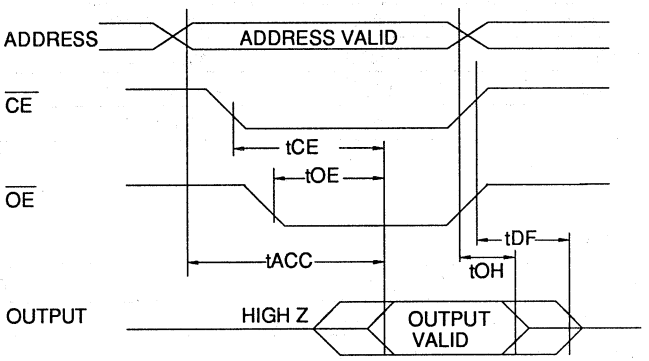
Pin Capacitance (f=1MHz T=25°C) [5]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Characteristics [1]

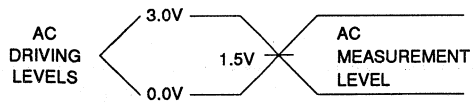
Symbol	Parameter	AT28PC64-15		AT28PC64-20		AT28PC64-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} [2]	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} [3]	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} [4,5]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



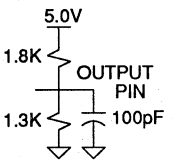
Notes:
1. C_L = 100pF.
2. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
5. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

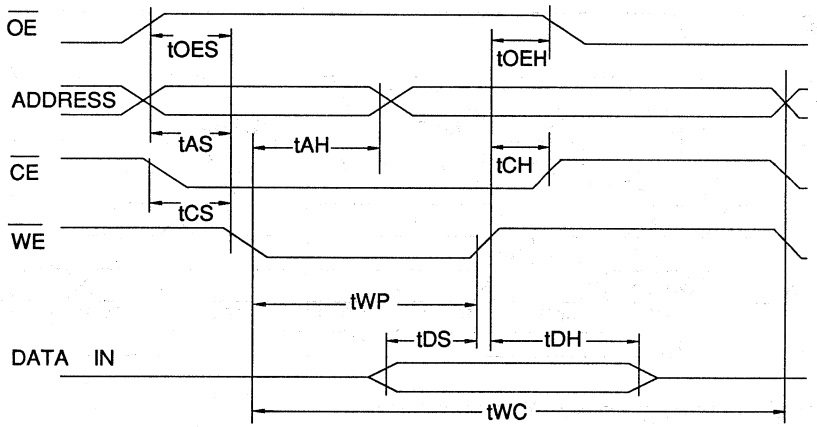
Output Test Load



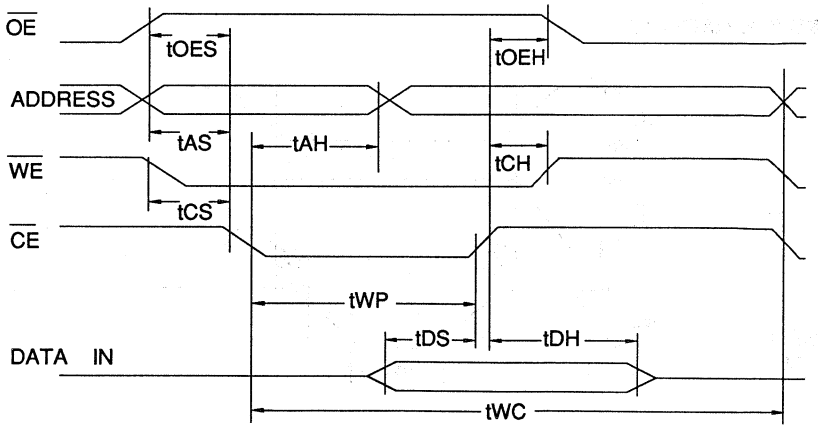
A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0			ns
t_{WC}	Write Cycle Time		1.0	2.0	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



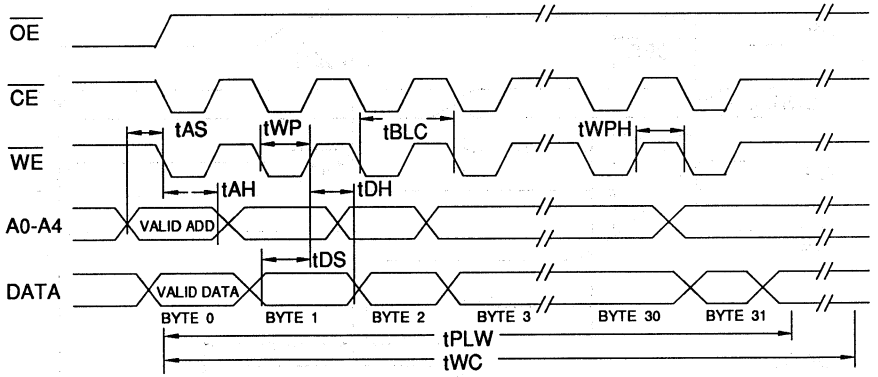
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Write Characteristics

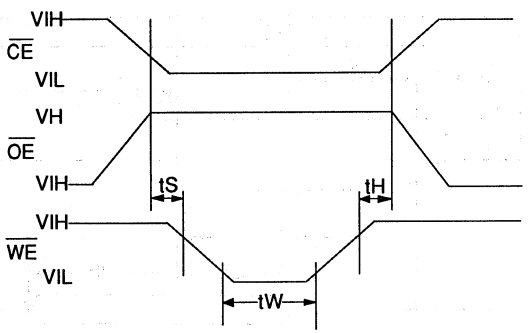
Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100		1000	ns
t_{BLC}	Byte Load Cycle Time	150			ns
t_{PLW}	Page Load Width			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms



Notes: A5 through A12 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



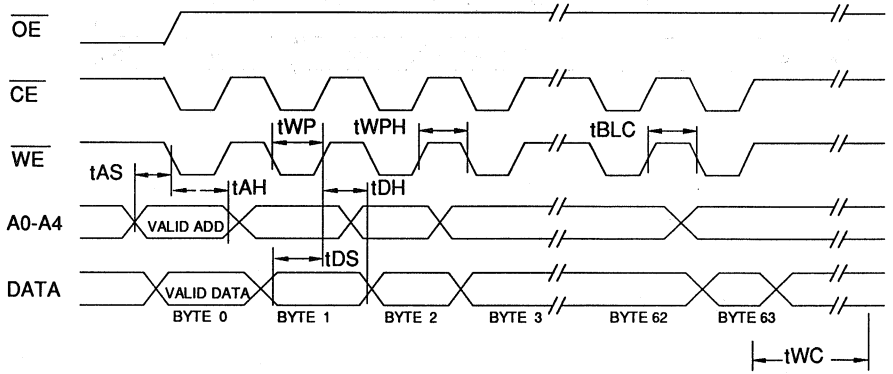
$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

Note: Some systems require increased load cycle time, beyond that permitted by the AT28PC64. The following Page Mode Write Characteristics and Waveforms address this situation. Please reference Atmel part number AT28PC64-SL376 to specify this device.

Page Mode Write Characteristics (AT28PC64-SL376)

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		1	2.0	ms
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	50			ns

Page Mode Write Waveforms (AT28PC64-SL376)



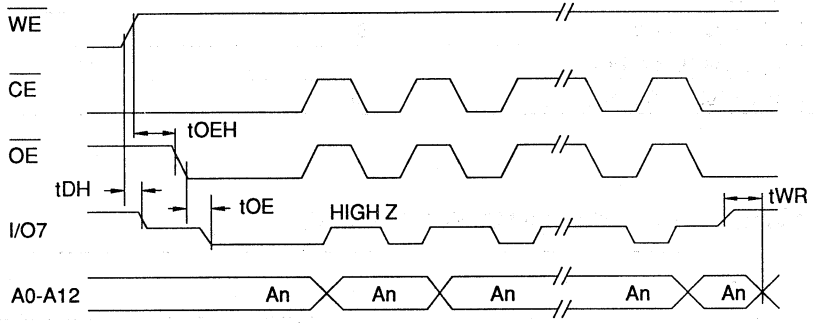
Notes: A5 through A12 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

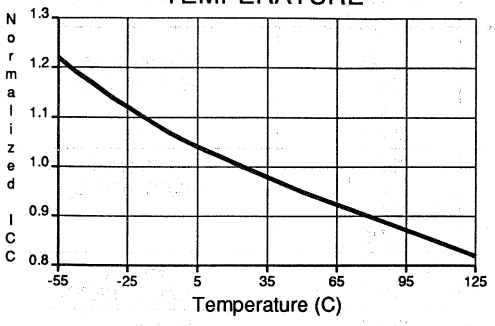
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			50	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

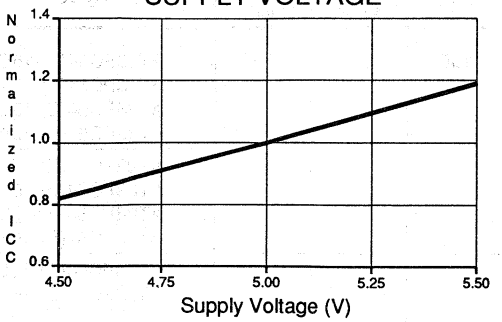
$\overline{\text{Data}}$ Polling Waveforms



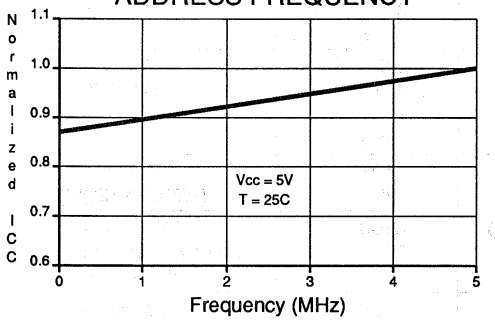
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.1	AT28PC64(E)-15DC AT28PC64(E)-15JC AT28PC64(E)-15LC AT28PC64(E)-15PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28PC64(E)-15DI AT28PC64(E)-15JI AT28PC64(E)-15LI AT28PC64(E)-15PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
150	80	0.2	AT28PC64(E)-15DM AT28PC64(E)-15LM	28D6 32L	Military (-55°C to 125°C)
			AT28PC64(E)-15DM/883 AT28PC64(E)-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.1	AT28PC64(E)-20DC AT28PC64(E)-20JC AT28PC64(E)-20LC AT28PC64(E)-20PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28PC64(E)-20DI AT28PC64(E)-20JI AT28PC64(E)-20LI AT28PC64(E)-20PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
200	80	0.2	AT28PC64(E)-20DM AT28PC64(E)-20LM	28D6 32L	Military (-55°C to 125°C)
			AT28PC64(E)-20DM/883 AT28PC64(E)-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.1	AT28PC64(E)-25DC AT28PC64(E)-25JC AT28PC64(E)-25LC AT28PC64(E)-25PC AT28PC64-W	28D6 32J 32L 28P6 DIE	Commercial (0°C to 70°C)
			AT28PC64(E)-25DI AT28PC64(E)-25JI AT28PC64(E)-25LI AT28PC64(E)-25PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
250	80	0.2	AT28PC64(E)-25DM AT28PC64(E)-25LM	28D6 32L	Military (-55°C to 125°C)
			AT28PC64(E)-25DM/883 AT28PC64(E)-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	80	0.2	AT28PC64(E)-30DM/883 AT28PC64(E)-30LM/883	28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)
350	80	0.2	AT28PC64(E)-35DM/883 AT28PC64(E)-35LM/883	28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.2	5962-87514 09 UX 5962-87514 09 XX 5962-87514 09 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.2	5962-87514 08 UX 5962-87514 08 XX 5962-87514 08 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	80	0.2	5962-87514 07 UX 5962-87514 07 XX 5962-87514 07 YX	32K 28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	80	0.2	5962-87514 06 UX 5962-87514 06 XX 5962-87514 06 YX	32K 28D6 32L	Military/883 Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32K	32 Lead, Non-Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 2 ms
E	High Endurance Option: Endurance = 100K Write Cycles

256K (32K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 3.0ms or 10ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **200µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

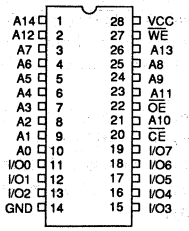
Description

The AT28C256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 200µA.

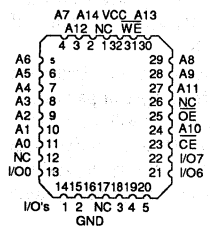
The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Pin Configurations

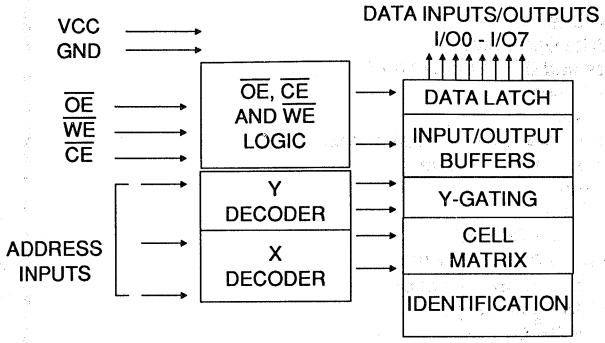


Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Device Operation

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28C256 allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28C256. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

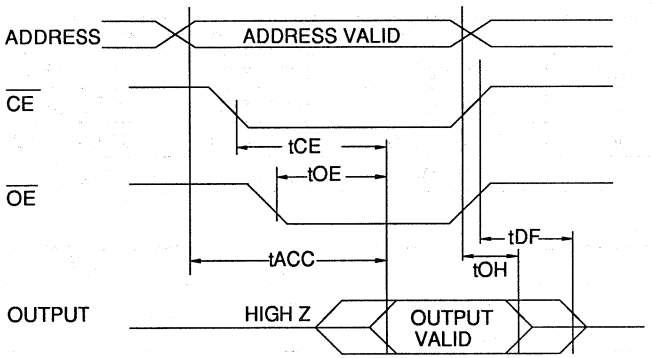
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC} + 1V	Com., Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA		2.4		V

A.C. Read Characteristics

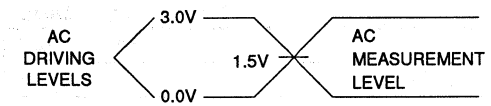
Symbol	Parameter	AT28C256-15		AT28C256-20		AT28C256-25		AT28C256-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250		350	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250		350	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



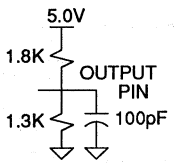
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

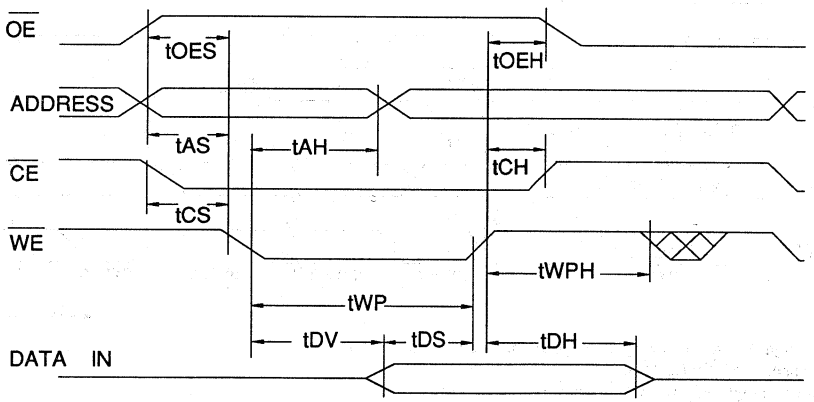
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Write Characteristics

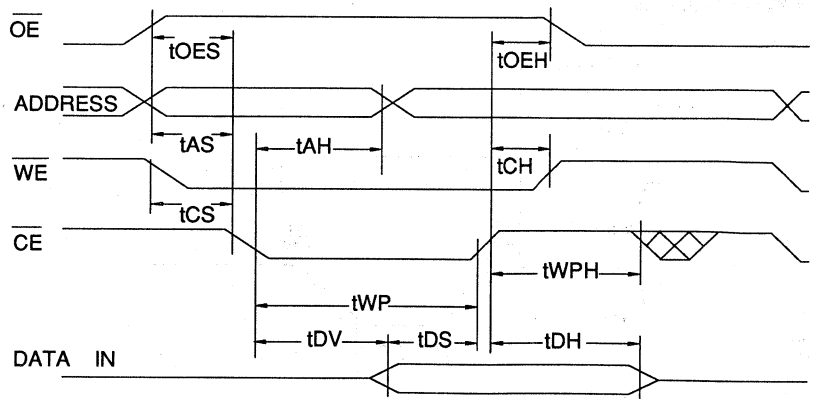
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{CS}	Chip Select Set-up Time		0		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		0		ns
t_{DV}	Time to Data Valid		NR(1)		
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms

Note: 1. NR = No Restiction

A.C. Write Waveforms- $\overline{WE}$ Controlled



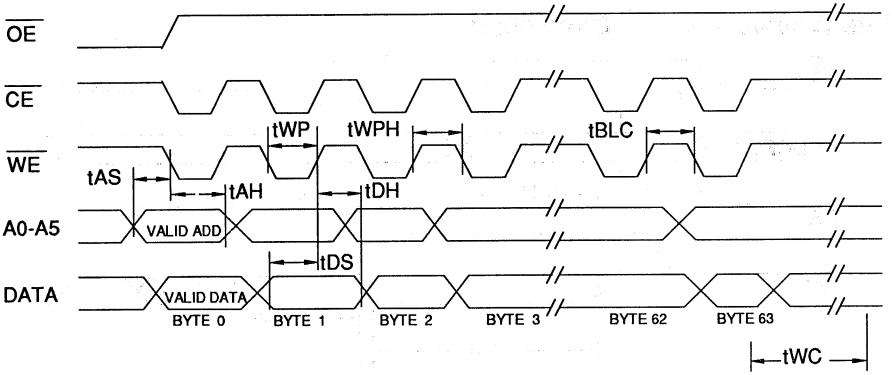
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Characteristics

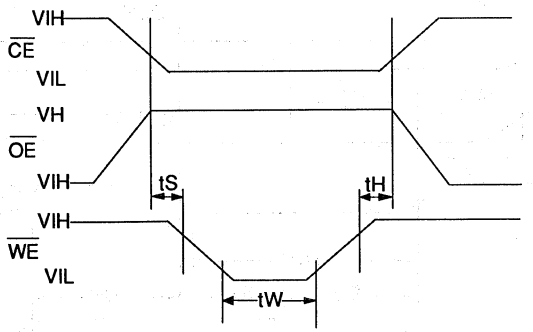
Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms
t_{AS}	Address Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

Page Mode Write Waveforms



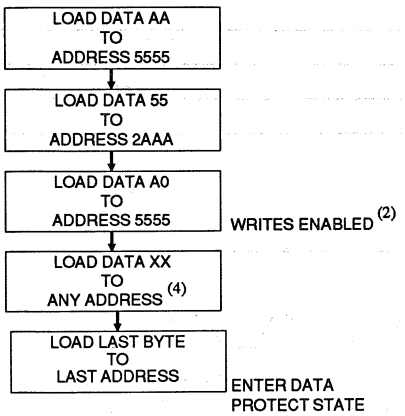
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

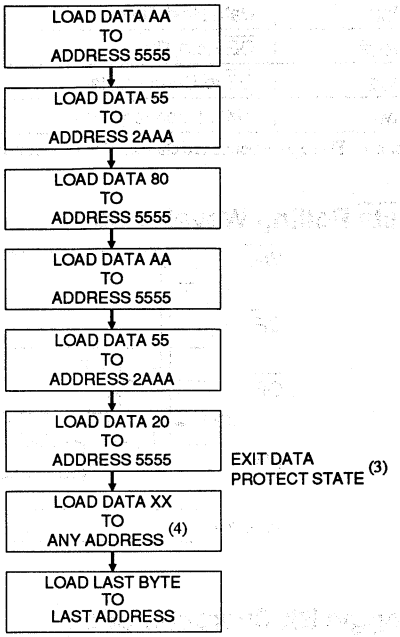


$t_S = t_H = 5\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

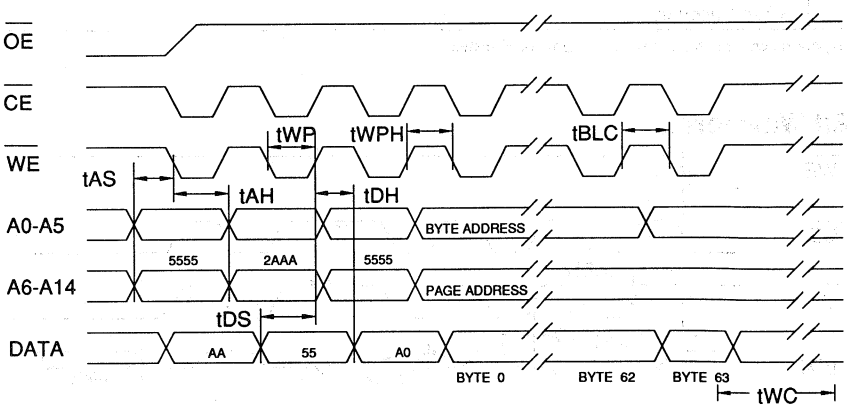


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms



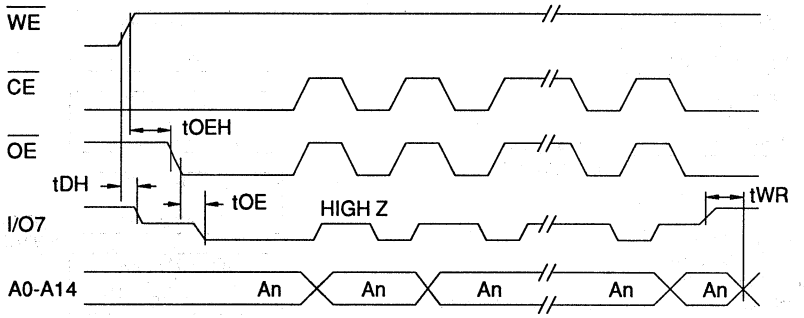
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

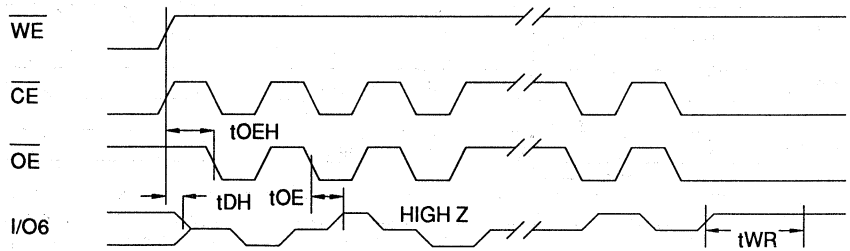


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

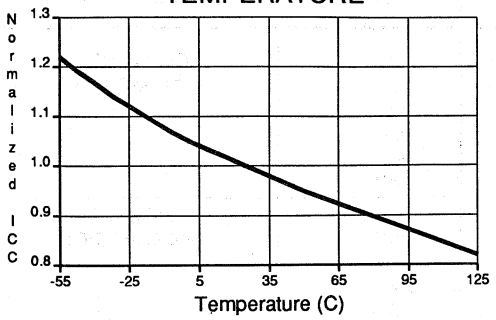
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

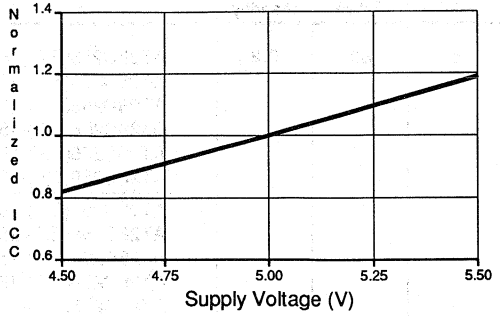


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

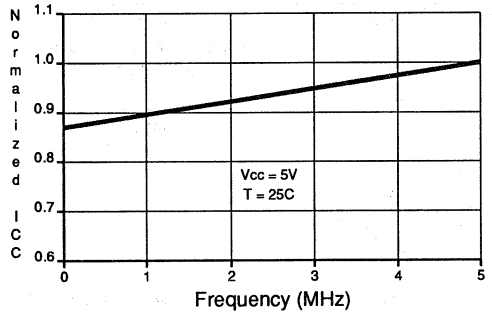
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.2	AT28C256(E,F)-15DC AT28C256(E,F)-15FC AT28C256(E,F)-15JC AT28C256(E,F)-15LC AT28C256(E,F)-15PC AT28C256(E,F)-15UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28C256(E,F)-15DI AT28C256(E,F)-15FI AT28C256(E,F)-15JI AT28C256(E,F)-15LI AT28C256(E,F)-15PI AT28C256(E,F)-15UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
150	80	0.3	AT28C256(E,F)-15DM AT28C256(E,F)-15FM AT28C256(E,F)-15LM AT28C256(E,F)-15UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28C256(E,F)-15DM/883 AT28C256(E,F)-15FM/883 AT28C256(E,F)-15LM/883 AT28C256(E,F)-15UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.2	AT28C256(E,F)-20DC AT28C256(E,F)-20FC AT28C256(E,F)-20JC AT28C256(E,F)-20LC AT28C256(E,F)-20PC AT28C256(E,F)-20UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28C256(E,F)-20DI AT28C256(E,F)-20FI AT28C256(E,F)-20JI AT28C256(E,F)-20LI AT28C256(E,F)-20PI AT28C256(E,F)-20UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
200	80	0.3	AT28C256(E,F)-20DM AT28C256(E,F)-20FM AT28C256(E,F)-20LM AT28C256(E,F)-20UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28C256(E,F)-20DM/883 AT28C256(E,F)-20FM/883 AT28C256(E,F)-20LM/883 AT28C256(E,F)-20UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.2	AT28C256(E,F)-25DC AT28C256(E,F)-25FC AT28C256(E,F)-25JC AT28C256(E,F)-25LC AT28C256(E,F)-25PC AT28C256(E,F)-25UC AT28C256-W	28D6 28F 32J 32L 28P6 28U DIE	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.2	AT28C256(E,F)-25DI AT28C256(E,F)-25FI AT28C256(E,F)-25JI AT28C256(E,F)-25LI AT28C256(E,F)-25PI AT28C256(E,F)-25UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
250	80	0.3	AT28C256(E,F)-25DM AT28C256(E,F)-25FM AT28C256(E,F)-25LM AT28C256(E,F)-25UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28C256(E,F)-25DM/883 AT28C256(E,F)-25FM/883 AT28C256(E,F)-25LM/883 AT28C256(E,F)-25UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	80	0.3	AT28C256(E,F)-30DM/883 AT28C256(E,F)-30FM/883 AT28C256(E,F)-30LM/883 AT28C256(E,F)-30UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	80	0.3	AT28C256(E,F)-35DM/883 AT28C256(E,F)-35FM/883 AT28C256(E,F)-35LM/883 AT28C256(E,F)-35UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.35	5962-88525 07 UX 5962-88525 07 XX 5962-88525 07 YX 5962-88525 07 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 06 UX 5962-88525 06 XX 5962-88525 06 YX 5962-88525 06 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.35	5962-88525 04 UX 5962-88525 04 XX 5962-88525 04 YX 5962-88525 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.35	5962-88525 03 UX 5962-88525 03 XX 5962-88525 03 YX 5962-88525 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 05 UX 5962-88525 05 XX 5962-88525 05 YX 5962-88525 05 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	80	0.35	5962-88525 02 UX 5962-88525 02 XX 5962-88525 02 YX 5962-88525 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
350	80	0.35	5962-88525 01 UX 5962-88525 01 XX 5962-88525 01 YX 5962-88525 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

256 (32K x 8) High Speed CMOS E^2PROM

Features

- **Fast Read Access Time - 70ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 10ms or 3ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **3mA Standby Current (AT28HC256L)**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

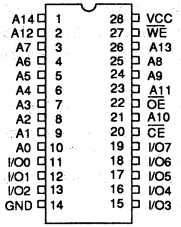
Description

The AT28HC256/L is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the AT28HC256 offers access times to 70ns with power dissipation of just 440mW. When the AT28HC256L is deselected, the standby current is less than 5mA.

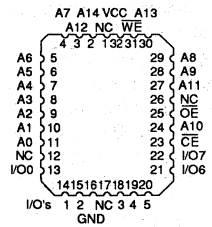
The AT28HC256/L is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28HC256/L has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of E^2PROM for device identification or tracking.

Pin Configurations

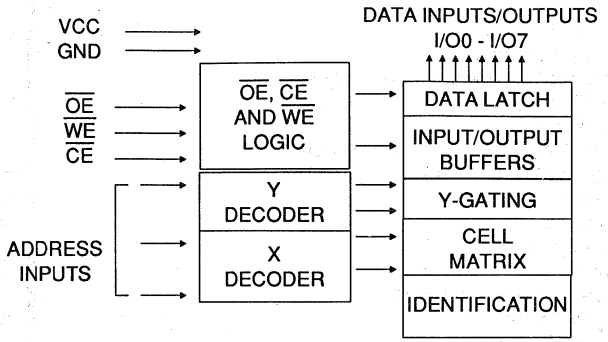


Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Device Operation

READ: The AT28HC256/L is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28HC256/L allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28HC256/L features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28HC256/L provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling, and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256/L in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28HC256/L. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12±0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28HC256-70	AT28HC256L-90	AT28HC256-90	AT28HC256L-12 AT28HC256-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.			-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.

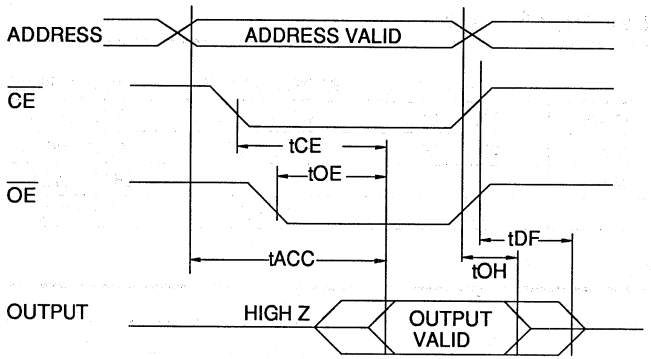
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V	AT28HC256L		3	mA
			AT28HC256		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE}$=-3.0V to V_{CC} + 1V	AT28HC256L		300	µA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=6.0mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-4mA		2.4		V

A.C. Read Characteristics

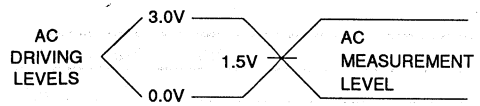
Symbol	Parameter	AT28HC256-70 Min	AT28HC256-70 Max	AT28C256-90 AT28HC256L-90 Min	AT28C256-90 AT28HC256L-90 Max	AT28HC256-12 AT28HC256L-12 Min	AT28HC256-12 AT28HC256L-12 Max	Units
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



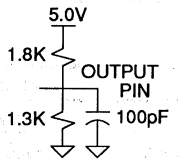
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

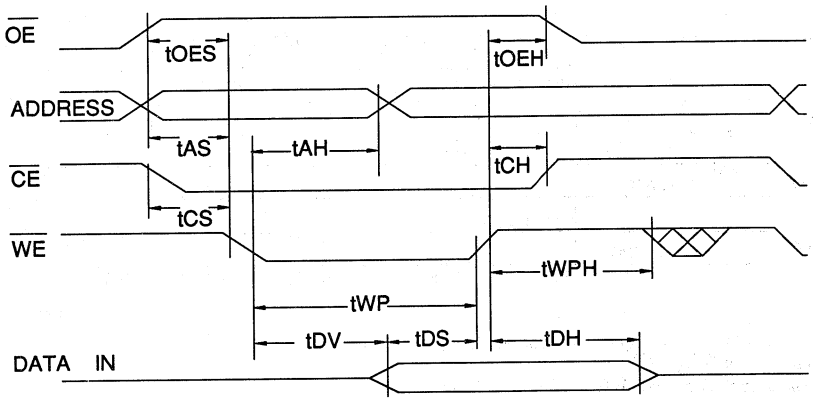
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Write Characteristics

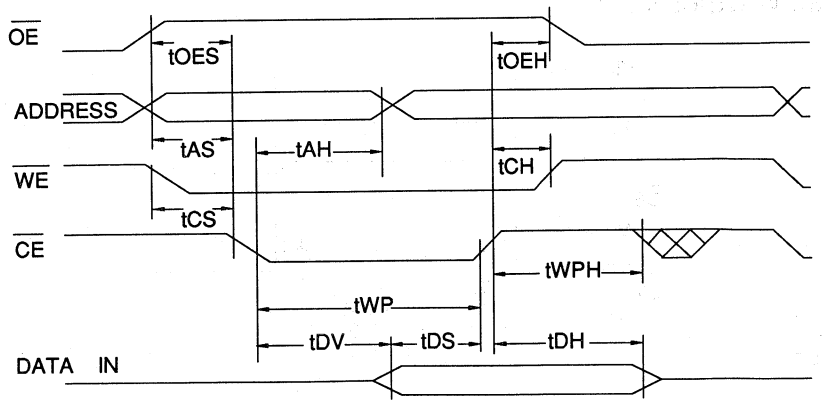
Symbol	Parameter		Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{CS}	Chip Select Set-up Time		0		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		0		ns
t_{DV}	Time to Data Valid		NR(1)		
t_{WC}	Write Cycle Time	AT28HC256		10	ms
		AT28HC256F		3.0	ms

Note: 1. NR = No Restiction

A.C. Write Waveforms- $\overline{WE}$ Controlled



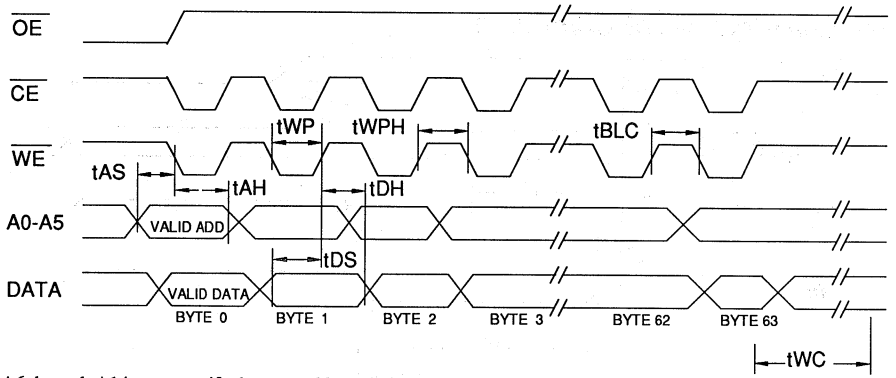
A.C. Write Load Waveforms- $\overline{CE}$ Controlled



Page Mode Write Characteristics

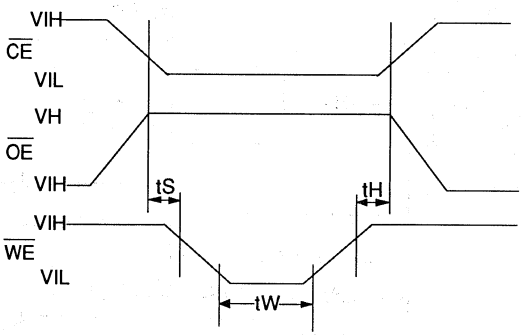
Symbol	Parameter		Min	Typ	Max	Units
t_{WC}	Write Cycle Time	AT28HC256		5	10	ms
		AT28HC256F		2	3.0	ms
t_{AS}	Address Set-up Time		0			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}	Data Hold Time		0			ns
t_{WP}	Write Pulse Width		100			ns
t_{BLC}	Byte Load Cycle Time				150	µs
t_{WPH}	Write Pulse Width High		50			ns

Page Mode Write Waveforms



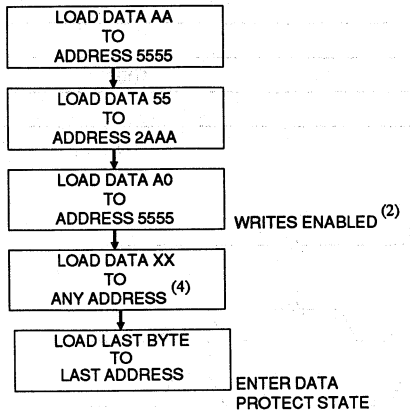
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms

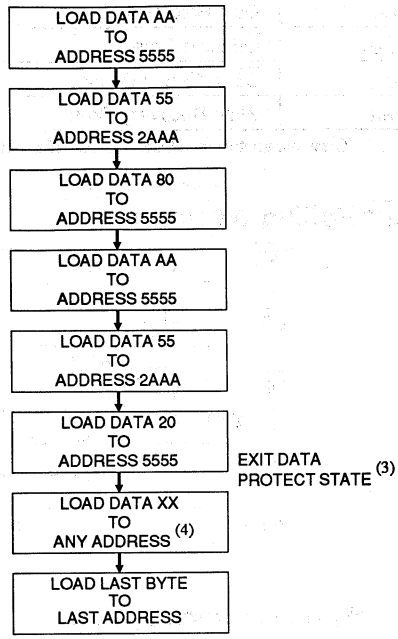


$t_S = t_H = 5\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

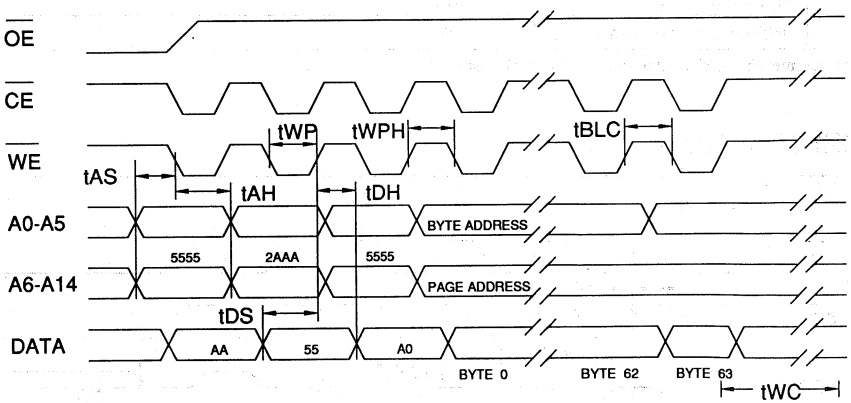


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms



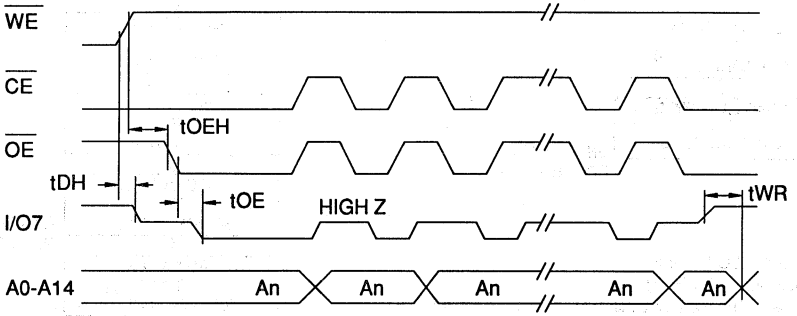
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

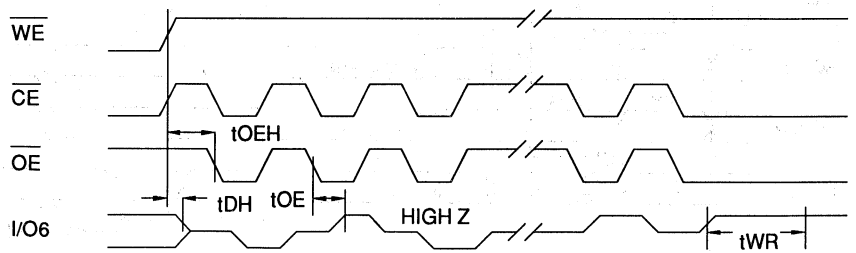


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

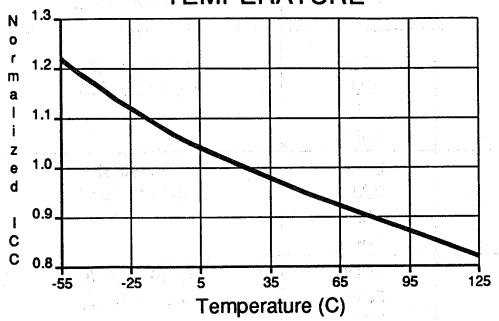
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

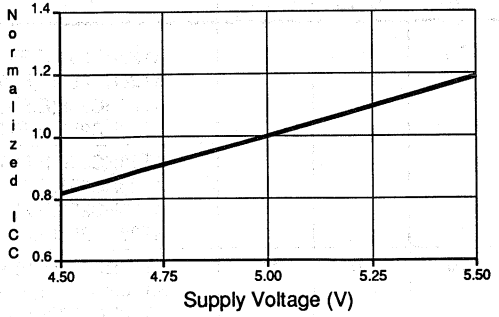


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

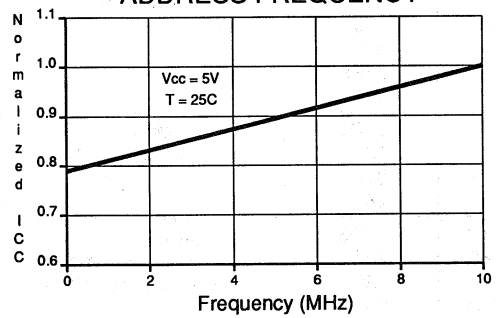
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	60	AT28HC256(E,F)-70DC AT28HC256(E,F)-70JC AT28HC256(E,F)-70LC AT28HC256(E,F)-70PC	28D6 32J 32L 28P6	Commercial (0°C to 70°C)
			AT28HC256(E,F)-70DI AT28HC256(E,F)-70JI AT28HC256(E,F)-70LI AT28HC256(E,F)-70PI	28D6 32J 32L 28P6	Industrial (-40°C to 85°C)
90	80	60	AT28HC256(E,F)-90DC AT28HC256(E,F)-90FC AT28HC256(E,F)-90JC AT28HC256(E,F)-90LC AT28HC256(E,F)-90PC AT28HC256(E,F)-90UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-90DI AT28HC256(E,F)-90FI AT28HC256(E,F)-90JI AT28HC256(E,F)-90LI AT28HC256(E,F)-90PI AT28HC256(E,F)-90UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-90DM AT28HC256(E,F)-90FM AT28HC256(E,F)-90LM AT28HC256(E,F)-90UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256(E,F)-90DM/883 AT28HC256(E,F)-90FM/883 AT28HC256(E,F)-90LM/883 AT28HC256(E,F)-90UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	60	AT28HC256(E,F)-12DC AT28HC256(E,F)-12FC AT28HC256(E,F)-12JC AT28HC256(E,F)-12LC AT28HC256(E,F)-12PC AT28HC256(E,F)-12UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256(E,F)-12DI AT28HC256(E,F)-12FI AT28HC256(E,F)-12JI AT28HC256(E,F)-12LI AT28HC256(E,F)-12PI AT28HC256(E,F)-12UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256(E,F)-12DM AT28HC256(E,F)-12FM AT28HC256(E,F)-12LM AT28HC256(E,F)-12UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256(E,F)-12DM/883 AT28HC256(E,F)-12FM/883 AT28HC256(E,F)-12LM/883 AT28HC256(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	60	5962-88634 03 UX 5962-88634 03 XX 5962-88634 03 YX 5962-88634 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 04 UX 5962-88634 04 XX 5962-88634 04 YX 5962-88634 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256L(E,F)-90DC AT28HC256L(E,F)-90FC AT28HC256L(E,F)-90JC AT28HC256L(E,F)-90LC AT28HC256L(E,F)-90PC AT28HC256L(E,F)-90UC	28D6 28F 32J 32L 28P6 28U	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-90DI AT28HC256L(E,F)-90FI AT28HC256L(E,F)-90JI AT28HC256L(E,F)-90LI AT28HC256L(E,F)-90PI AT28HC256L(E,F)-90UI AT28HC256L(E,F)-W	28D6 28F 32J 32L 28P6 28U DIE	Industrial (-40°C to 85°C)
120	80	0.3	AT28HC256L(E,F)-12DC AT28HC256L(E,F)-12FC AT28HC256L(E,F)-12JC AT28HC256L(E,F)-12LC AT28HC256L(E,F)-12PC AT28HC256L(E,F)-12UC AT28HC256L-W	28D6 28F 32J 32L 28P6 28U DIE	Commercial (0°C to 70°C)
			AT28HC256L(E,F)-12DI AT28HC256L(E,F)-12FI AT28HC256L(E,F)-12JI AT28HC256L(E,F)-12LI AT28HC256L(E,F)-12PI AT28HC256L(E,F)-12UI	28D6 28F 32J 32L 28P6 28U	Industrial (-40°C to 85°C)
			AT28HC256L(E,F)-12DM AT28HC256L(E,F)-12FM AT28HC256L(E,F)-12LM AT28HC256L(E,F)-12UM	28D6 28F 32L 28U	Military (-55°C to 125°C)
			AT28HC256L(E,F)-12DM/883 AT28HC256L(E,F)-12FM/883 AT28HC256L(E,F)-12LM/883 AT28HC256L(E,F)-12UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-88634 01 UX 5962-88634 01 XX 5962-88634 01 YX 5962-88634 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88634 02 UX 5962-88634 02 XX 5962-88634 02 YX 5962-88634 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

1 Megabit (64K x 16) Paged CMOS E^2PROM

Features

- Fast Read Access Time - 120ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Words
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10ms maximum
  - 1 to 64 Word Page Write Operation
- Low Power Dissipation
  - 100mA Active Current
  - 400µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Word-Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Description

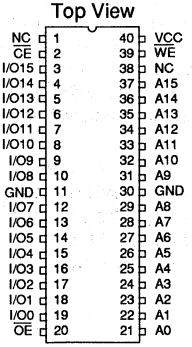
The AT28C1024 is a high performance Electrically Erasable and Programmable Read Only Memory. Its 1 MBit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times down to 120ns with power dissipation of just 550mW. When the device is deselected, the CMOS standby current is less than 400µA.

The AT28C1024 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-word page register to allow writing of up to 64 words simultaneously. During a write cycle, the addresses and 1 to 64 words of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7 or I/O15. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C1024 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 words of E^2PROM for device identification or tracking.

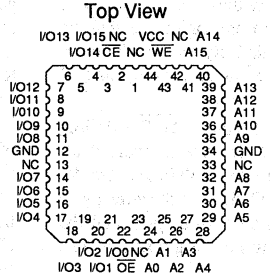
Pin Configurations

Top View

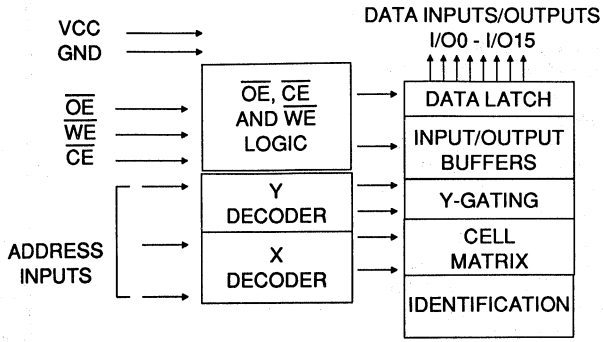


Pin Name	Function
A0 - A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

Top View



Block Diagram



Device Operation

READ: The AT28C1024 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28C1024 allows 1 to 64 words of data to be loaded into the device and then simultaneously written during the internal programming period. After the first word has been loaded into the device successive words may be loaded in the same manner. Each new word to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding word. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A15 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which words within the page are to be written. The words may be loaded in any order and may be changed within the same load period. Only words which are specified for writing will be written; unnecessary cycling of other words within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C1024 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a write cycle an attempted read of the last word written will result in the complement of the written data on I/07 and I/O15. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C1024 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O14 toggling between one and zero. Once the write has completed, I/O14 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C1024 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28C1024. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 64 words of E^2PROM memory are available to the user for device identification. By raising A9 to 12±0.5V and using address locations FFC0H to FFFFH the additional words may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to VCC +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to 13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28C1024-12	AT28C1024-15	AT28C1024-20	AT28C0124-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
VCC Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	DOUT
Write(2)	V_{IL}	V_{IH}	V_{IL}	DIN
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

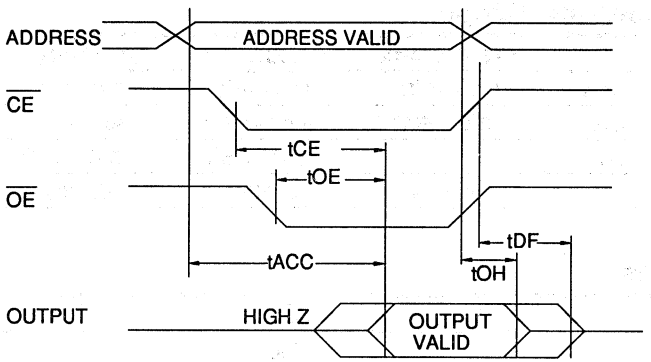
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to VCC + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to VCC		10	µA
I_{SB1}	VCC Standby Current CMOS	$\overline{CE}$=VCC-.3V to VCC + 1V		400	µA
I_{SB2}	VCC Standby Current TTL	$\overline{CE}$=2.0V to VCC + 1V		5	mA
ICC	VCC Active Current	f=5MHz; I_{OUT}=0mA		100	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA	2.4		V

A.C. Read Characteristics

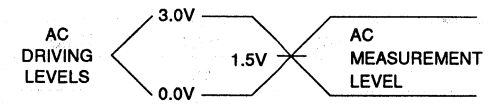
Symbol	Parameter	AT28C1024-12		AT28C1024-15		AT28C1024-20		AT28C1024-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



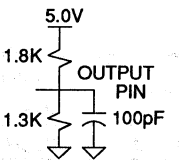
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



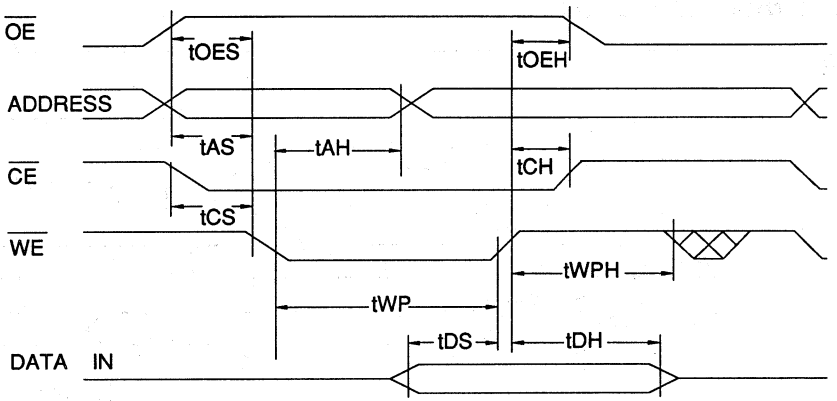
Pin Capacitance (f=1MHz T=25°C) (4)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

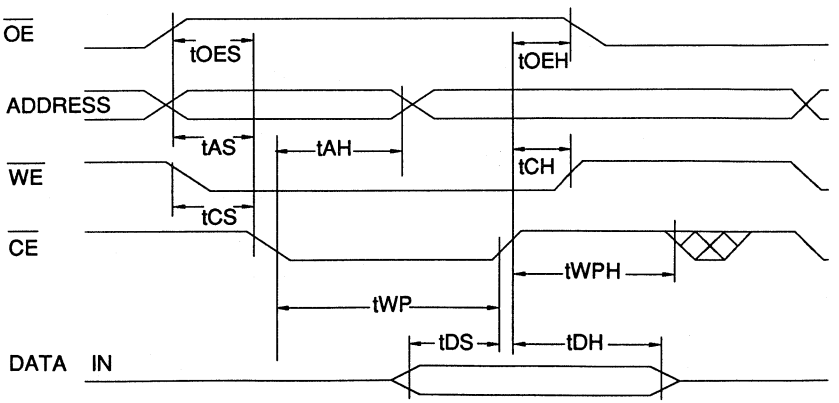
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



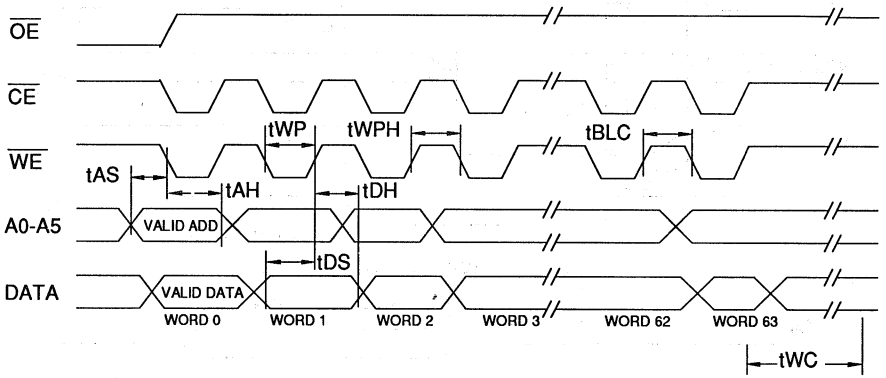
A.C. Write Waveforms- $\overline{CE}$ Controlled



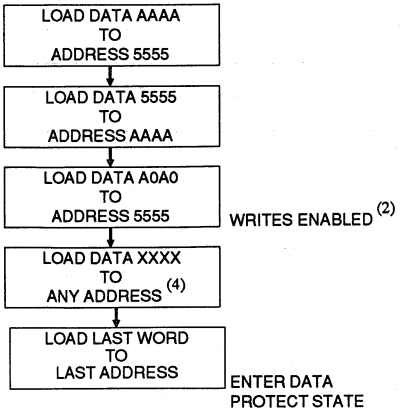
Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

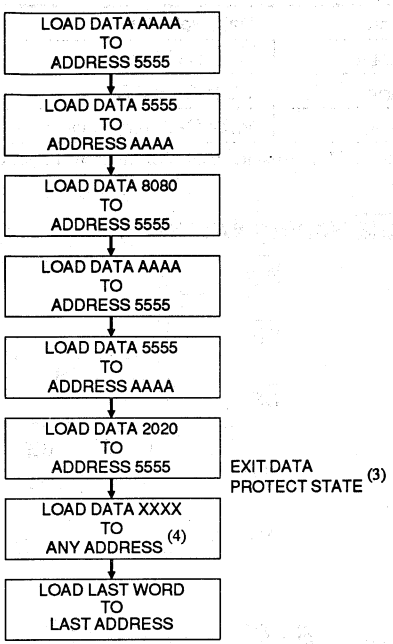
Page Mode Write Waveforms



Software Data Protection Enable Algorithm [1]

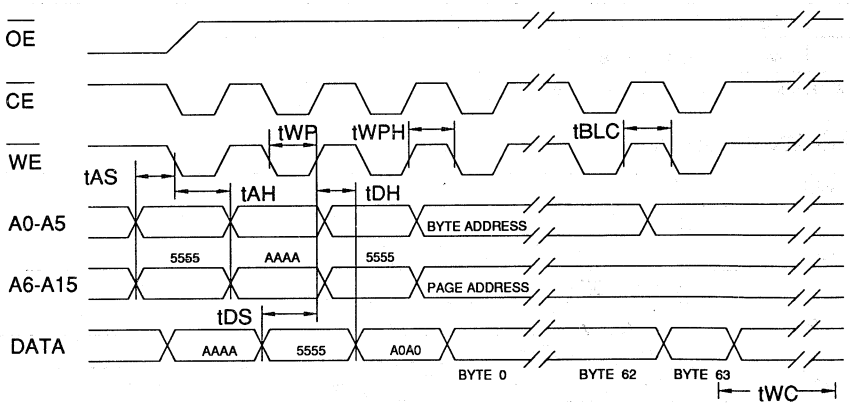


Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O15 - I/O0 (Hex);
   Address Format: A15 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 words of data are loaded.

Software Protected Program Cycle Waveform



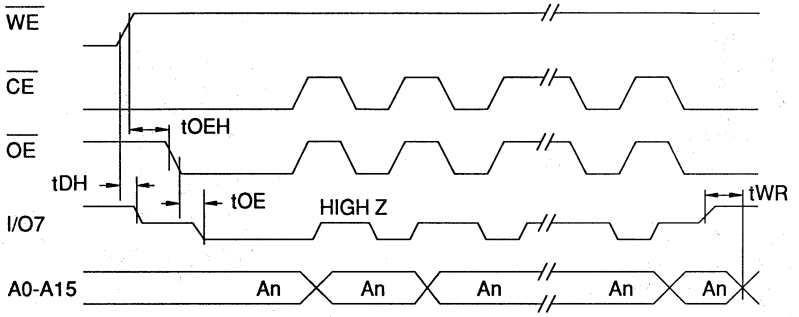
Notes: A6 through A15 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Data Polling Waveforms

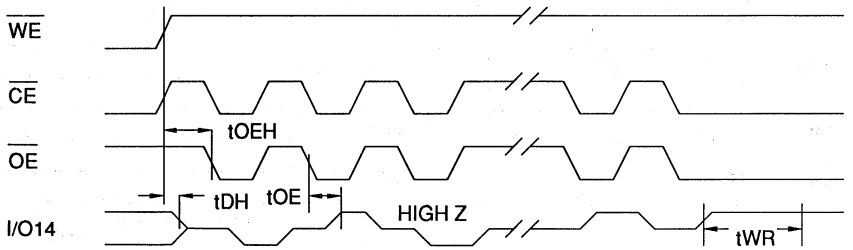


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O14 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	100	0.4	AT28C1024-12BC AT28C1024-12LC	40B 44L	Commercial (0° to 70°C)
			AT28C1024-12BI AT28C1024-12LI	40B 44L	Industrial (-40° to 85°C)
150	100	0.4	AT28C1024-15BC AT28C1024-15LC AT28C1024-15VC	40B 44L V	Commercial (0° to 70°C)
			AT28C1024-15BI AT28C1024-15LI AT28C1024-15VI	40B 44L V	Industrial (-40° to 85°C)
			AT28C1024-15BM AT28C1024-15LM AT28C1024-15VM	40B 44L V	Military (-55°C to 125°C)
			AT28C1024-15BM/883 AT28C1024-15LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	100	0.4	AT28C1024-20BC AT28C1024-20LC AT28C1024-20VC	40B 44L V	Commercial (0° to 70°C)
			AT28C1024-20BI AT28C1024-20LI AT28C1024-20VI	40B 44L V	Industrial (-40° to 85°C)
			AT28C1024-20BM AT28C1024-20LM AT28C1024-20VM	40B 44L V	Military (-55°C to 125°C)
			AT28C1024-20BM/883 AT28C1024-20LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	100	0.4	AT28C1024-25BC AT28C1024-25LC AT28C1024-25VC AT28C1024-W	40B 44L V DIE	Commercial (0° to 70°C)
			AT28C1024-25BI AT28C1024-25LI AT28C1024-25VI	40B 44L V	Industrial (-40° to 85°C)
			AT28C1024-25BM AT28C1024-25LM AT28C1024-25VM	40B 44L V	Military (-55°C to 125°C)
			AT28C1024-25BM/883 AT28C1024-25LM/883	40B 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

	Package Type
40B	40 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
V	Tape Automated Bond (TAB) Carrier
W	Die

1 Megabit (128K x 8) Paged CMOS E^2PROM

Features

- Fast Read Access Time - 120ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80mA Active Current
  - 300µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

Description

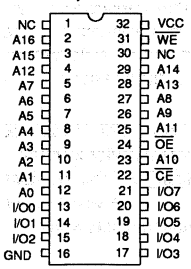
The AT28C010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its one megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 300µA.

The AT28C010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 128 bytes of E^2PROM for device identification or tracking.

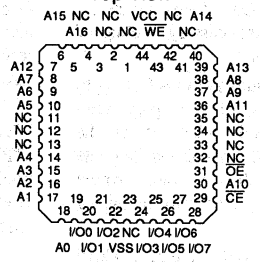
Pin Configurations

Top View

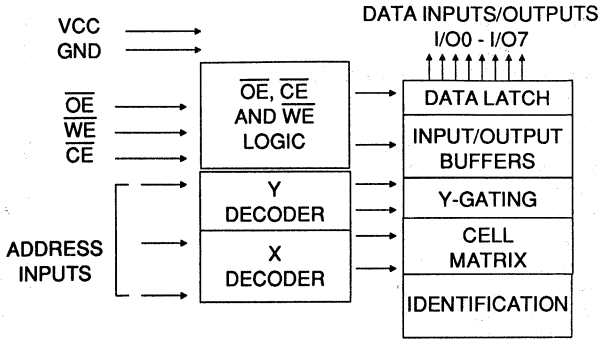


Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Top View



Block Diagram



Device Operation

READ: The AT28C010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28C010 allows one to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28C010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28C010 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28C010 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V (typical) the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28C010. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

DEVICE IDENTIFICATION: An extra 128 bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 1FF80H to 1FFFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

D.C. and A.C. Operating Range

		AT28C010-12	AT28C010-15	AT28C010-20	AT28C010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

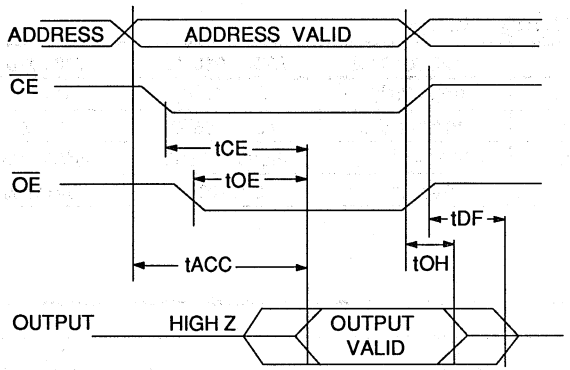
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC} + 1V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH1}	Output High Voltage	I_{OH}=-400µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH}=-100µA; V_{CC}=4.5V	4.2		V

A.C. Read Characteristics

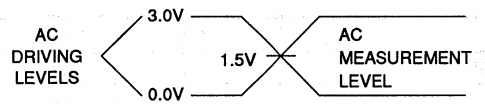
Symbol	Parameter	AT28C010-12		AT28C010-15		AT28C010-20		AT28C010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	55	0	55	0	55	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



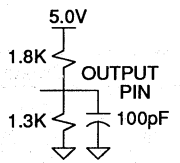
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



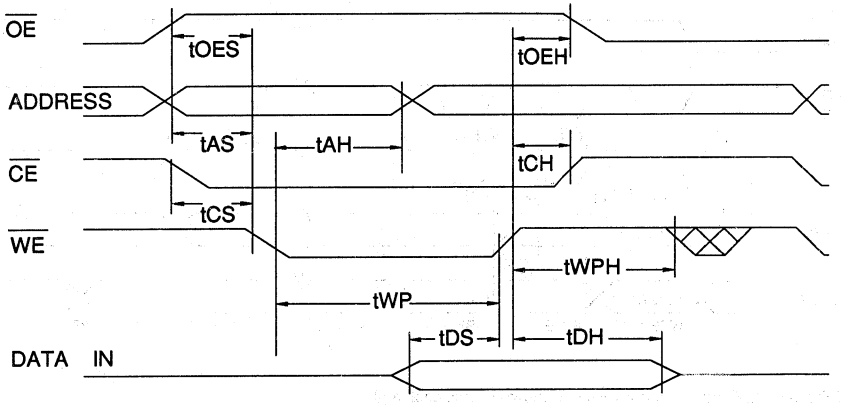
Pin Capacitance (f=1MHz T=25°C) (4)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

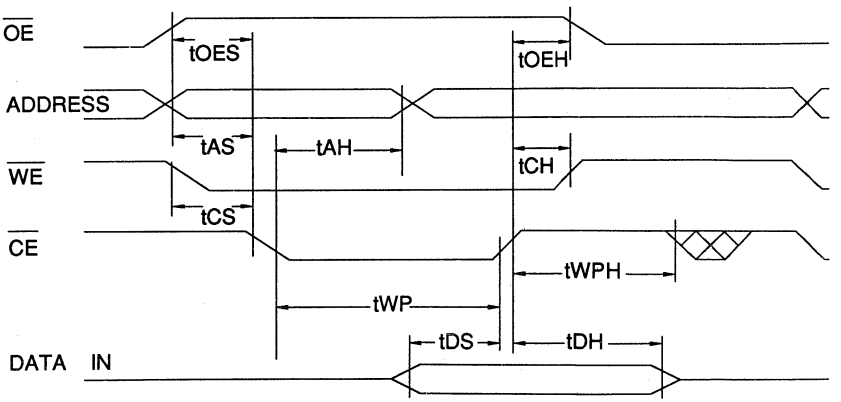
A.C. Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

A.C. Write Waveforms- $\overline{WE}$ Controlled



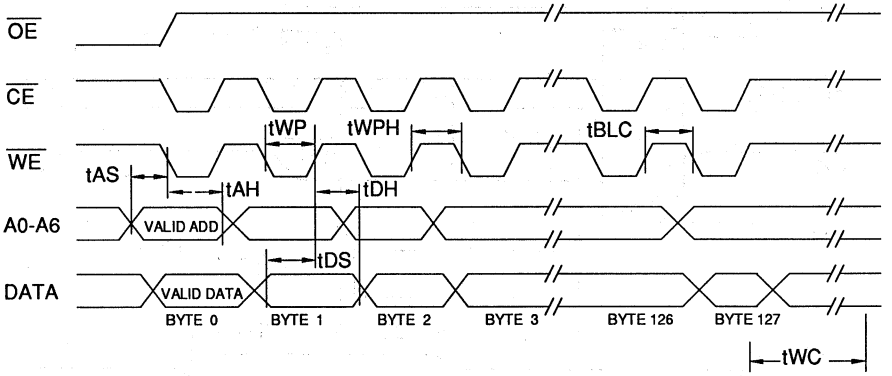
A.C. Write Waveforms- $\overline{CE}$ Controlled



Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms



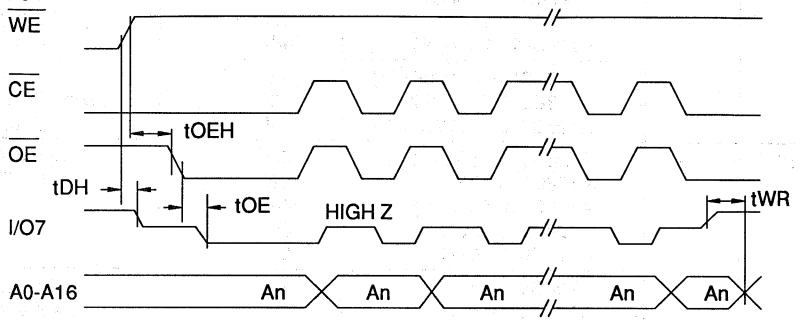
Notes: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

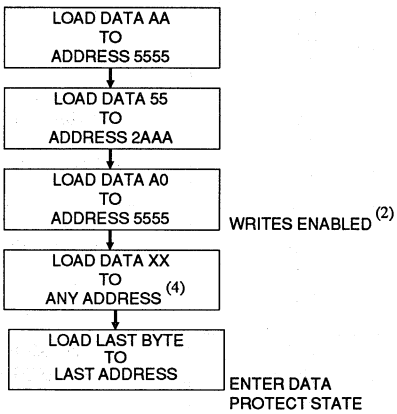
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

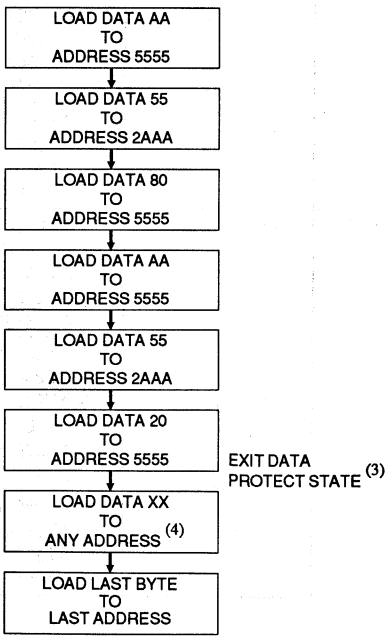
$\overline{\text{Data}}$ Polling Waveforms



Software Data Protection Enable Algorithm [1]



Software Data Protection Disable Algorithm [1]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT28C010-12BC (E) AT28C010-12FC AT28C010-12LC (E)	32B 32F 44L	Commercial (0° to 70°C)
			AT28C010-12BI (E) AT28C010-12FI AT28C010-12LI (E)	32B 32F 44L	Industrial (-40° to 85°C)
			AT28C010-12BM (E) AT28C010-12FM AT28C010-12LM (E)	32B 32F 44L	Military (-55°C to 125°C)
			AT28C010-12BM/883 (E) AT28C010-12FM/883 AT28C010-12LM/883 (E)	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT28C010-15BC (E) AT28C010-15FC AT28C010-15LC (E) AT28C010-15UC AT28C010-15VC	32B 32F 44L 30U V	Commercial (0° to 70°C)
			AT28C010-15BI (E) AT28C010-15FI AT28C010-15LI (E) AT28C010-15UI AT28C010-15VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-15BM (E) AT28C010-15FM AT28C010-15LM (E) AT28C010-15UM AT28C010-15VM	32B 32F 44L 30U V	Military (-55°C to 125°C)
			AT28C010-15BM/883 (E) AT28C010-15FM/883 AT28C010-15LM/883 (E) AT28C010-15UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT28C010-20BC (E) AT28C010-20FC AT28C010-20LC (E) AT28C010-20UC AT28C010-20VC	32B 32F 44L 30U V	Commercial (0° to 70°C)
			AT28C010-20BI (E) AT28C010-20FI AT28C010-20LI (E) AT28C010-20UI AT28C010-20VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-20BM (E) AT28C010-20FM AT28C010-20LM (E) AT28C010-20UM AT28C010-20VM	32B 32F 44L 30U V	Military (-55°C to 125°C)

Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	0.3	AT28C010-20BM/883 (E) AT28C010-20FM/883 AT28C010-20LM/883 (E) AT28C010-20UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C010-25BC (E) AT28C010-25FC AT28C010-25LC (E) AT28C010-25UC AT28C010-25VC AT28C010-W	32B 32F 44L 30U V DIE	Commercial (0° to 70°C)
			AT28C010-25BI (E) AT28C010-25FI AT28C010-25LI (E) AT28C010-25UI AT28C010-25VI	32B 32F 44L 30U V	Industrial (-40° to 85°C)
			AT28C010-25BM (E) AT28C010-25FM AT28C010-25LM (E) AT28C010-25UM AT28C010-25VM	32B 32F 44L 30U V	Military (-55°C to 125°C)
			AT28C010-25BM/883 (E) AT28C010-25FM/883 AT28C010-25LM/883 (E) AT28C010-25UM/883	32B 32F 44L 30U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	0.3	5962-38267 07M XX 5962-38267 07M ZX 5962-38267 07M YX	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	5962-38267 05M XX 5962-38267 05M YX 5962-38267 05M ZX	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	5962-38267 03M XX 5962-38267 03M YX 5962-38267 03M ZX	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	5962-38267 01M XX 5962-38267 01M YX 5962-38267 01M ZX	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
30U	30 Pin, Ceramic Pin Grid Array (PGA)
V	Tape Automated Bond (TAB) Carrier
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs

1 Megabit (128K x 8) Paged CMOS E^2PROM Module

Features

- **Fast Read Access Time - 120ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64 Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 10ms maximum**
  - **1 to 64 Byte Page Write Operation**
- **Low Power Dissipation**
  - **100mA Active Current**
  - **5mA Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10,000 cycles**
  - **Data Retention: 10 years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

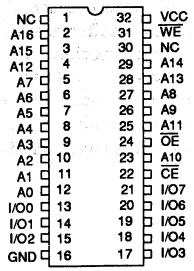
Description

The AT28MC010 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 1 MBit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120ns with power dissipation of just 550mW. When the device is deselected, the CMOS standby current is typically less than 100µA.

The AT28MC010 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

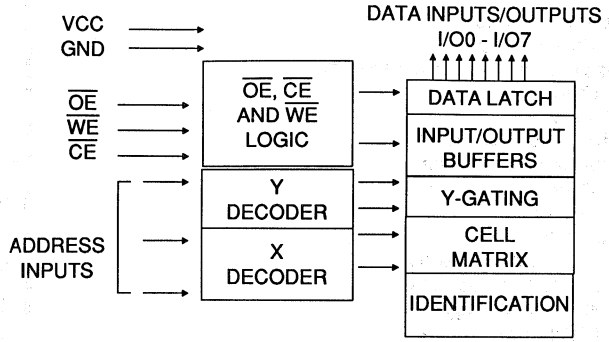
Atmel's 28MC010 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

Pin Configurations



Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Block Diagram



Device Operation

READ: The AT28MC010 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28MC010 allows one to 64 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end, and the internal programming period will start. A6 to A16 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC010 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28MC010 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero (A15 and A16 must address the page being written). Once the write has completed, I/O6 will stop toggling, and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28MC010 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited (b) Vcc power on delay— once Vcc has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28MC010. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to Vcc +0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28MC010-12	AT28MC010-15	AT28MC010-20	AT28MC010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	DOUT
Write(2)	V_{IL}	V_{IH}	V_{IL}	DIN
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

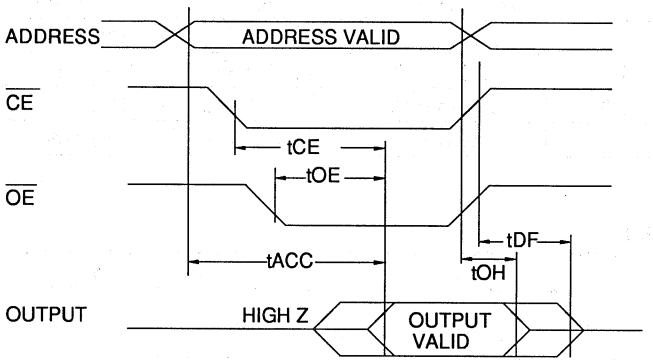
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to Vcc + 1V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to Vcc		20	µA
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$=Vcc-.3V to Vcc + 1V		5	mA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$=2.0V to Vcc + 1V		8	mA
Icc	Vcc Active Current	f=5MHz; I_{OUT}=0mA $\overline{CE}$=0V, $\overline{OE}$=$\overline{WE}$=Vcc		100	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA	2.4		V

A.C. Read Characteristics

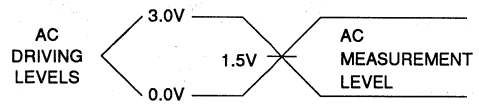
Symbol	Parameter	AT28MC010-12		AT28MC010-15		AT28MC010-20		AT28MC010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	60	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	50	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



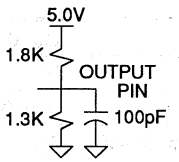
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

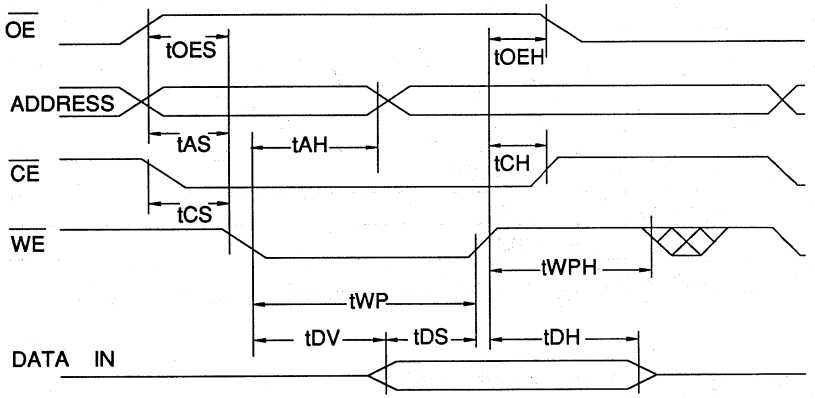
	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0V
C_{OUT}	20	40	pF	V_{OUT} = 0V

A.C. Write Characteristics

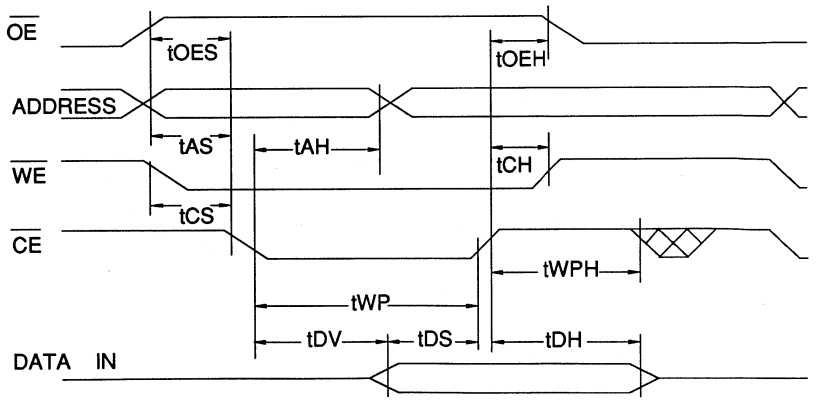
Symbol	Parameter	Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH} (1)	Address Hold Time	100			ns
t_{CS}	Chip Select Set-up Time	0			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150			ns
t_{DS}	Data Set-up Time	100			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{DV}	Time to Data Valid	NR(2)			
t_{WC}	Write Cycle Time		5.0	10	ms

Notes: 1. A15 and A16 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.
2. NR = No Restriction.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

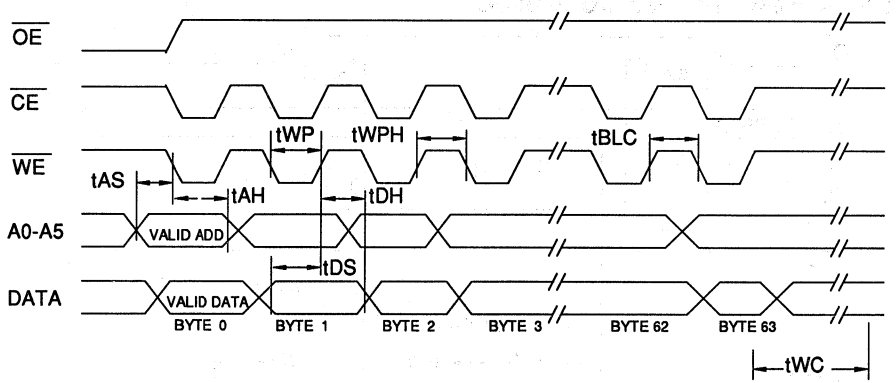


Page Mode Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Set-up Time	10			ns
t_{AH} (1)	Address Hold Time	100			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	10			ns
t_{WP}	Write Pulse Width	150			ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High	100			ns
t_{DW}	Delay to Next Write	0			ns

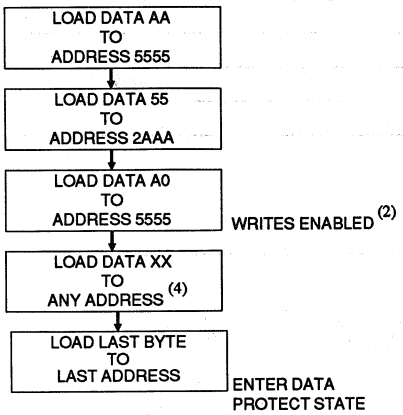
Notes: 1. A15 and A16 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

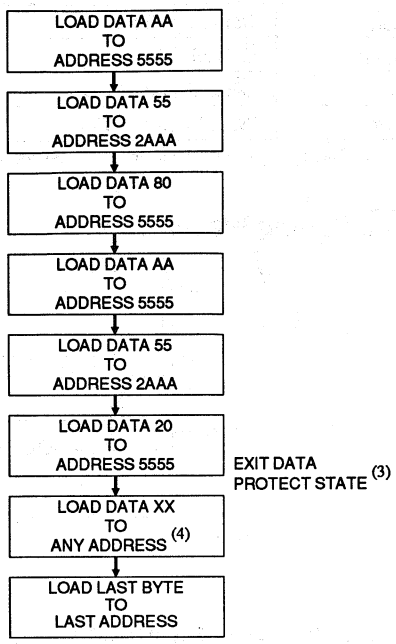


Notes: A6 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm (1,5,6)

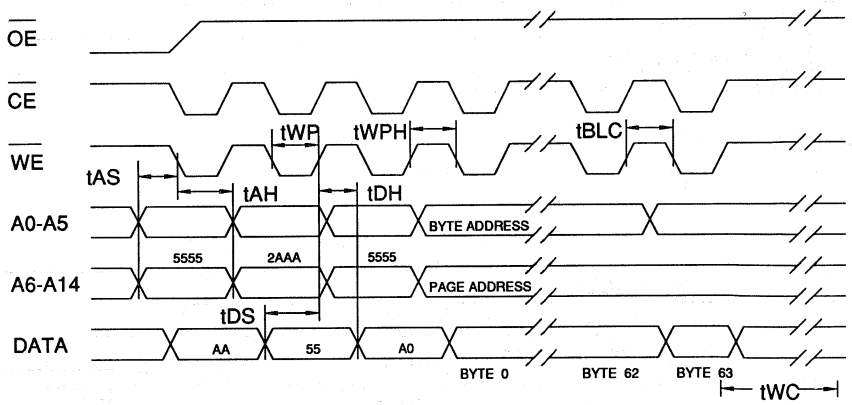


Software Data Protection Disable Algorithm (1,5,6)



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.
5. A15 and A16 must address page to be written.
6. Quadrants determined by A15 and A16 act independently.

Software Protected Program Cycle Waveform



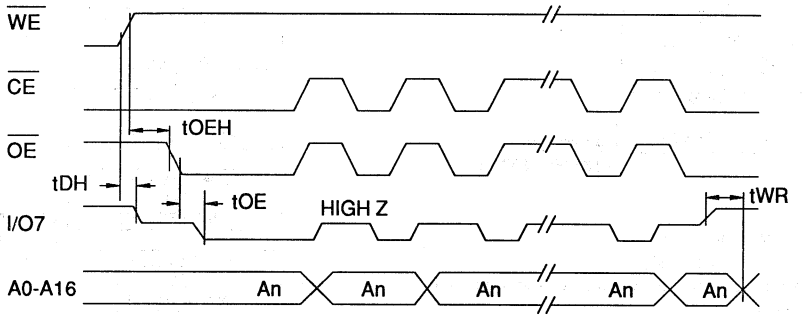
Notes: A6 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

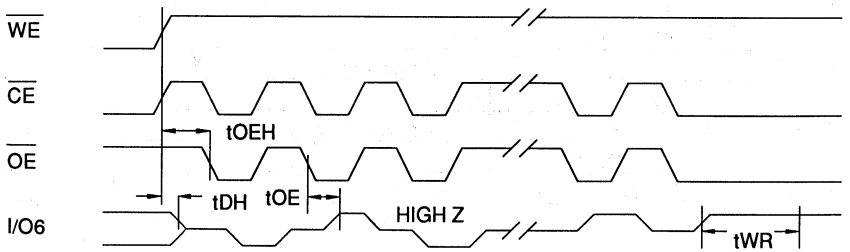


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms



Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location within the quadrant determined by A15 and A16 may be used but the address should not vary.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	100	0.5	AT28MC010-12MC	32M1	Commercial (0° to 70°C)
			AT28MC010-12MI	32M1	Industrial (-40° to 85°C)
			AT28MC010-12MM	32M1	Military (-55°C to 125°C)
			AT28MC010-12MMB	32M1	Military/883C Class B Components (-55°C to 125°C)
150	100	0.5	AT28MC010-15MC	32M1	Commercial (0° to 70°C)
			AT28MC010-15MI	32M1	Industrial (-40° to 85°C)
			AT28MC010-15MM	32M1	Military (-55°C to 125°C)
			AT28MC010-15MMB	32M1	Military/883C Class B Components (-55°C to 125°C)
200	100	0.5	AT28MC010-20MC	32M1	Commercial (0° to 70°C)
			AT28MC010-20MI	32M1	Industrial (-40° to 85°C)
			AT28MC010-20MM	32M1	Military (-55°C to 125°C)
			AT28MC010-20MMB	32M1	Military/883C Class B Components (-55°C to 125°C)
250	100	0.5	AT28MC010-25MC	32M1	Commercial (0° to 70°C)
			AT28MC010-25MI	32M1	Industrial (-40° to 85°C)
			AT28MC010-25MM	32M1	Military (-55°C to 125°C)
			AT28MC010-25MMB	32M1	Military/883C Class B Components (-55°C to 125°C)

Package Type	
32M1	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible LCC Module (Module)

2 Megabit (256K x 8) Paged CMOS E^2PROM Module

Preliminary

Features

- Fast Read Access Time - 150ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80mA Active Current
  - 5mA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

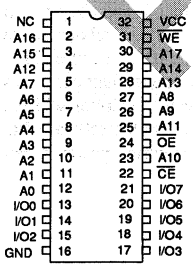
Description

The AT28MC020 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its two megabit of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 5mA.

The AT28MC020 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

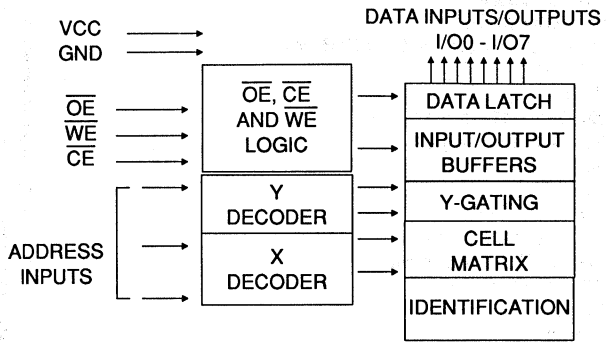
Atmel's 28MC020 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

Pin Configurations



Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

Block Diagram



Device Operation

READ: The AT28MC020 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28MC020 allows one to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A17 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC020 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28MC020 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28MC020 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V (typical) the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28MC020. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28MC020-15	AT28MC020-20	AT28MC020-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

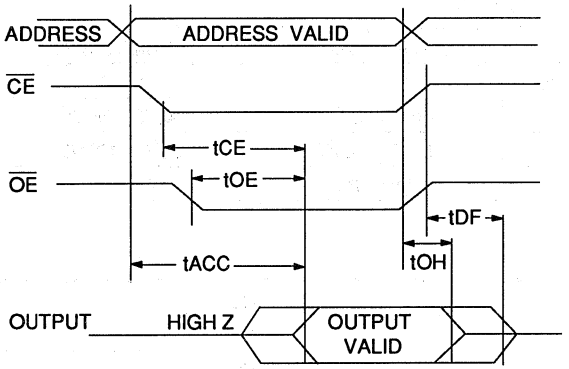
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}		20	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC} + 1V		5	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V		8	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA	2.4		V

A.C. Read Characteristics

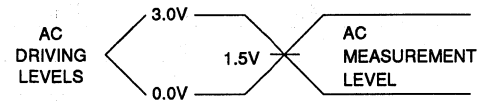
Symbol	Parameter	AT28MC020-15		AT28MC020-20		AT28MC020-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



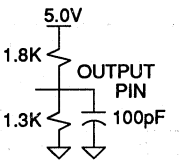
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

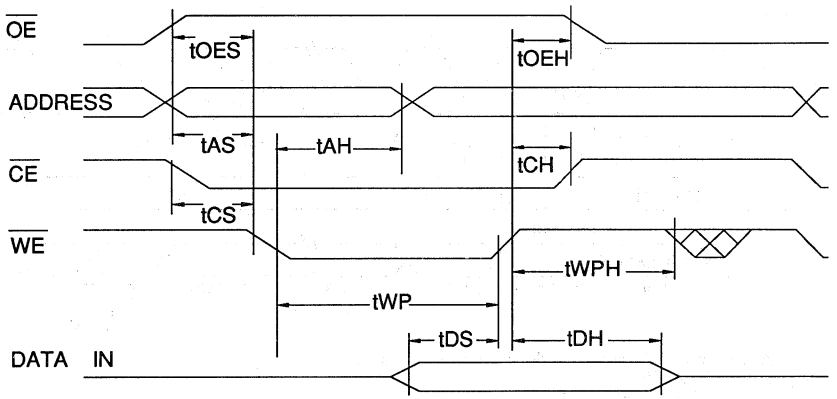
	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0V
C_{OUT}	20	40	pF	V_{OUT} = 0V

A.C. Write Characteristics

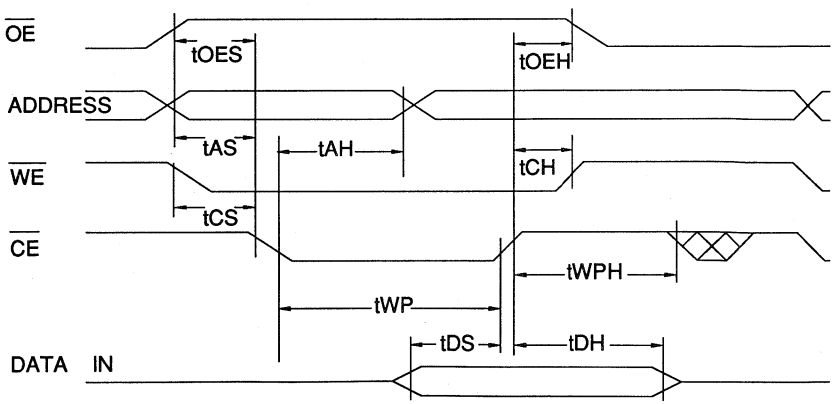
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

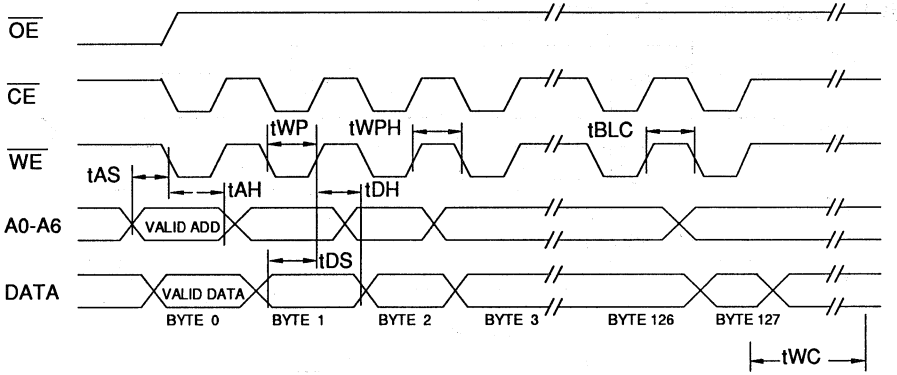


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

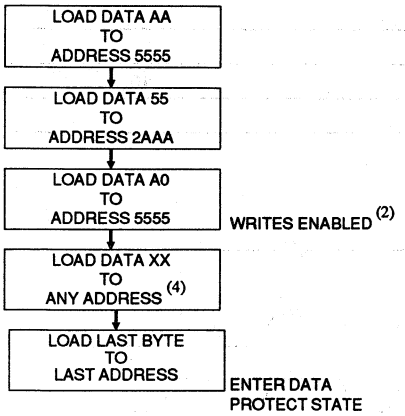
Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

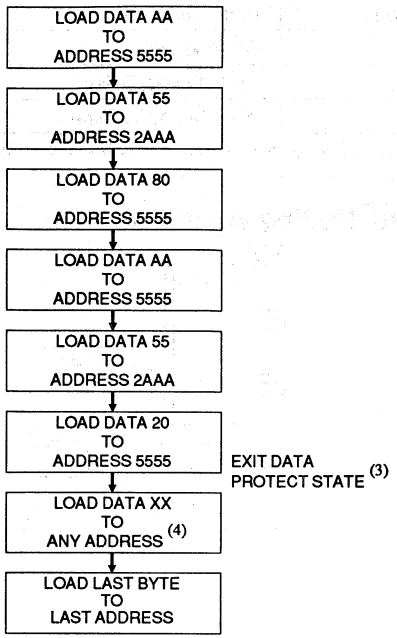


Notes: A7 through A17 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1,5,6]

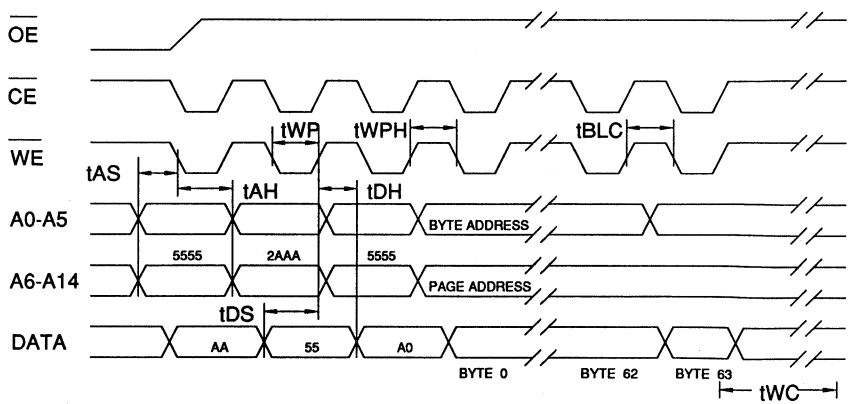


Software Data Protection Disable Algorithm [1,5,6]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A17 must address page to be written.
6. The quadrant determined by A17 acts independently.

Software Protected Program Cycle Waveform



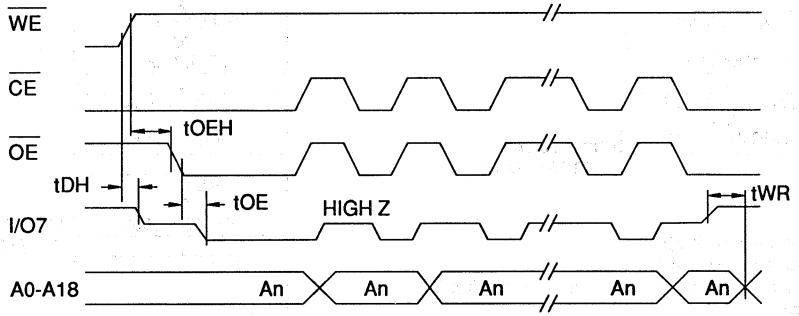
Notes: A6 through A17 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
A17 must address the desired quadrant while writing the software data protection code.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.5	AT28MC020-15MC AT28MC020-15ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC020-15MC AT28MC020-15ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC020-15MM AT28MC020-15ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC020-15MMB AT28MC020-15ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)
200	80	0.5	AT28MC020-20MC AT28MC020-20ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC020-20MI AT28MC020-20ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC020-20MM AT28MC020-20ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC020-20MMB AT28MC020-20ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)
250	80	0.5	AT28MC020-25MC AT28MC020-25ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC020-25MI AT28MC020-25ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC020-25MM AT28MC020-25ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC020-25MMB AT28MC020-25ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)

Package Type	
32M2	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)

4 Megabit (512K x 8) Paged CMOS E^2PROM Module

Preliminary

Features

- Fast Read Access Time - 150ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80mA Active Current
  - 5mA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

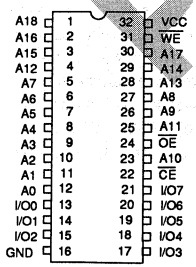
Description

The AT28MC040 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its four megabit of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 5mA.

The AT28MC040 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

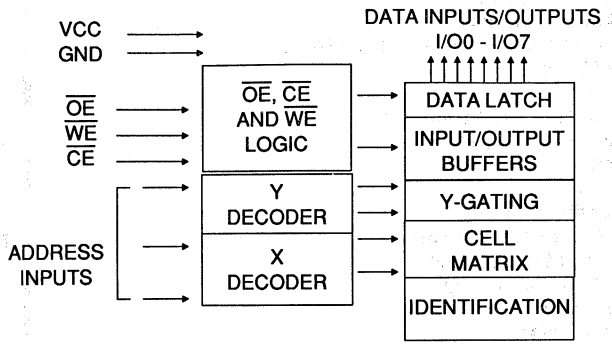
Atmel's 28MC040 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

Pin Configurations



Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs

Block Diagram



Device Operation

READ: The AT28MC040 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE MODE: The page write operation of the AT28MC040 allows one to 128 bytes of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data byte has been loaded into the device successive bytes may be loaded in the same manner. Each new byte to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A18 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be changed within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC040 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data on I/O7. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28MC040 provides another method for determining the end of a write cycle. During a write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during the write cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent writes to the AT28MC040 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8V (typical) the device will automatically time out 5ms (typical) before allowing a write. (c) Write inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT28MC040. Once the software protection is enabled a software algorithm must be issued to the device before a write may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three write commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three write commands must begin each write cycle in order for the writes to occur. All software write commands must obey the page write timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, but the software feature will guard against inadvertent writes during power transitions.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

		AT28MC040-15	AT28MC040-20	AT28MC040-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

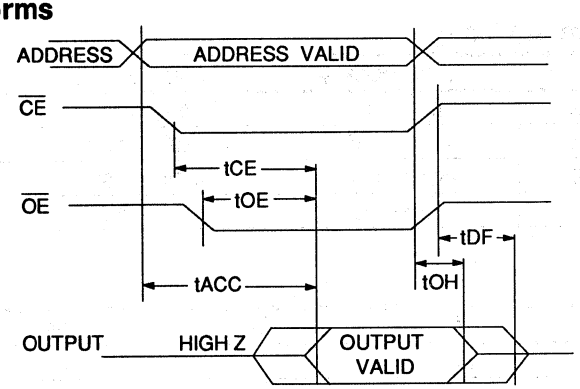
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC} + 1V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}		20	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC} + 1V		5	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC} + 1V		8	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH}=-400µA	2.4		V

A.C. Read Characteristics

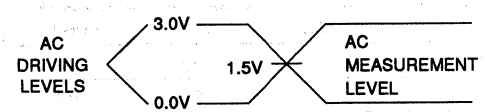
Symbol	Parameter	AT28MC040-15		AT28MC040-20		AT28MC040-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms



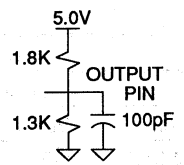
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

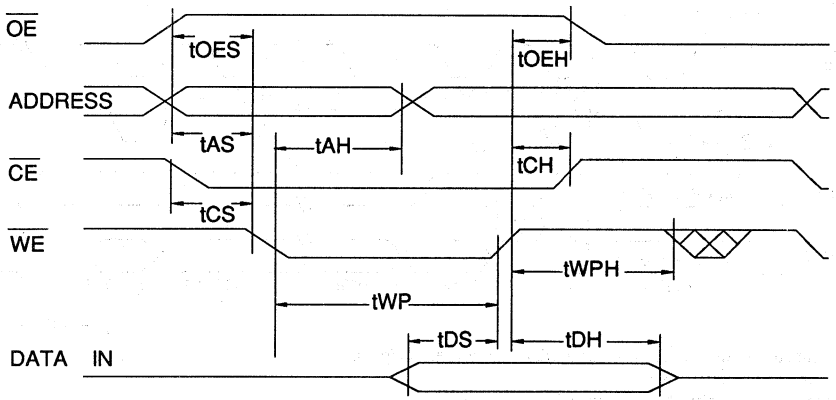
	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0V
C_{OUT}	20	40	pF	V_{OUT} = 0V

A.C. Write Characteristics

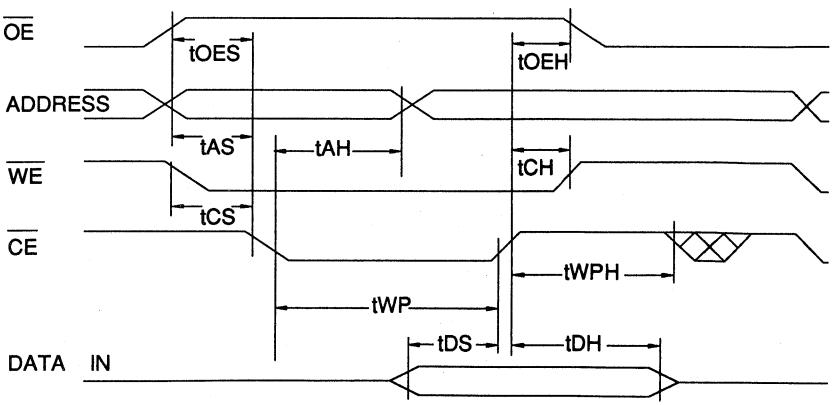
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

Notes: 1. A17 and A18 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

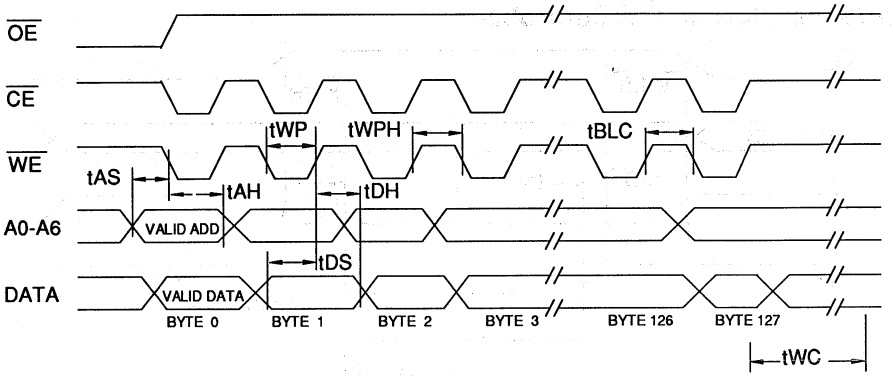


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

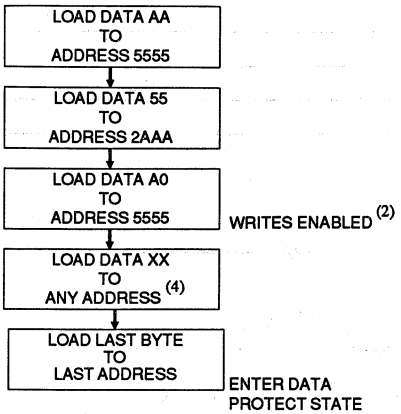
Notes: 1. A17 and A18 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

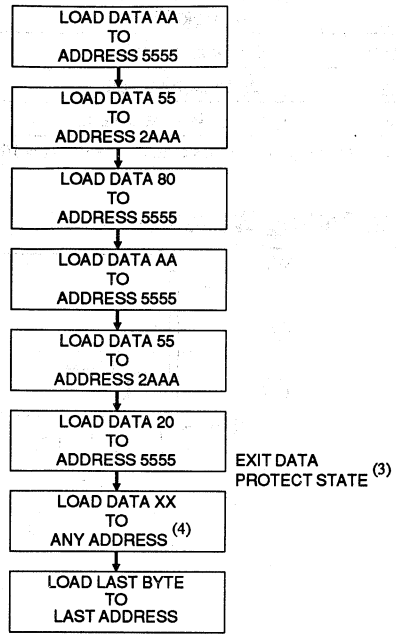


Notes: A7 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1,5,6]

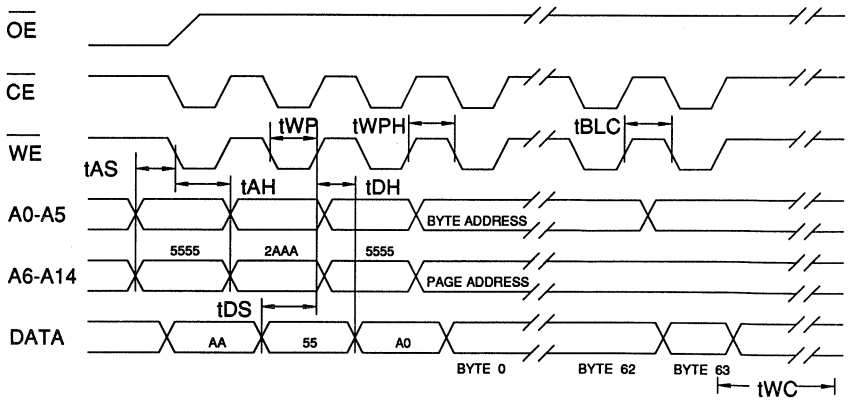


Software Data Protection Disable Algorithm [1,5,6]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A17 and A18 must address page to be written.
6. Quadrants determined by A17 and A18 act independently.

Software Protected Program Cycle Waveform



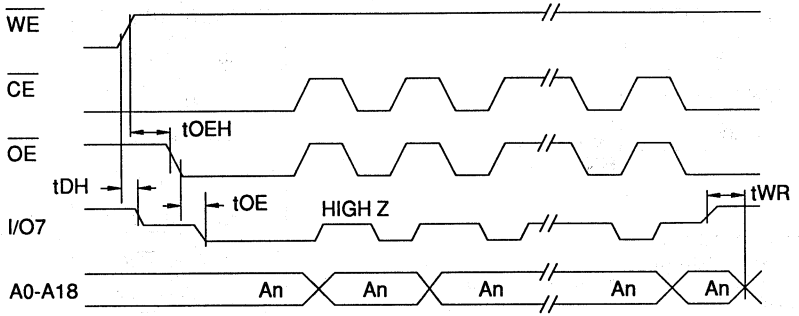
Notes: A6 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
A17 and A18 must address the desired quadrant while writing the software data protection code.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.5	AT28MC040-15MC AT28MC040-15ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC040-15MI AT28MC040-15ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC040-15MM AT28MC040-15ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC040-15MMB AT28MC040-15ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)
200	80	0.5	AT28MC040-20MC AT28MC040-15ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC040-20MI AT28MC040-20ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC040-20MM AT28MC040-20ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC040-20MMB AT28MC040-20ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)
250	80	0.5	AT28MC040-25MC AT28MC040-25ZC	32M2 32Z	Commercial (0° to 70°C)
			AT28MC040-25MI AT28MC040-25ZI	32M2 32Z	Industrial (-40° to 85°C)
			AT28MC040-25MM AT28MC040-25ZM	32M2 32Z	Military (-55°C to 125°C)
			AT28MC040-25MMB AT28MC040-25ZMB	32M2 32Z	Military/883C Class B Components (-55°C to 125°C)

Package Type	
32M2	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Flatpack Module (Module)
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)

Contents

256K (32K x 8) 5-Volt Only CMOS PEROM

Features

- Fast Read Access Time - 120ns
- Five Volt Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 64 Bytes
- Fast Program Cycle Times
  - Page (64 Byte) Program Time - 10ms
  - Chip Erase Time - 10ms
- Internal Program Control Timer
- Low Power Dissipation
  - 80mA Active Current
  - 300µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Erase/Program Cycles
  - 10 Year Data Retention
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

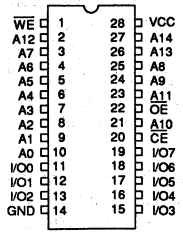
Description

The AT29C256 is a 5 volt only in system Programmable and Erasable Read Only Memory (PEROM). Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 300µA.

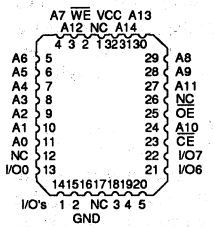
To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five volt only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C256 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations

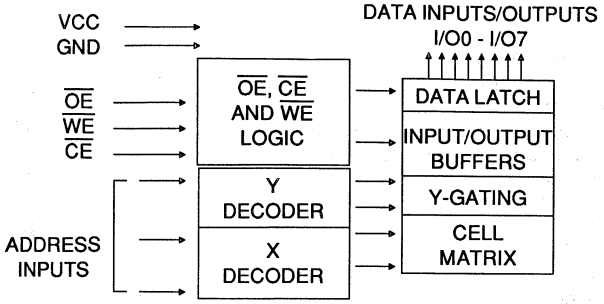


Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Device Operation

READ: The AT29C256 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

$\overline{DATA}$ POLLING: The AT29C256 features $\overline{DATA}$ Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical), the program function is inhibited. (b) Vcc power on delay— once Vcc has reached the Vcc sense level, the device will automatically time out 5ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

5 VOLT CHIP ERASE: The entire device may be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required.

HIGH VOLTAGE CHIP ERASE: The contents of the entire device may be set to the high state by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high; when $\overline{WE}$ is pulsed low for a minimum of 10ms, the contents of the entire device is erased.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware or software operation. For details, see Operating Modes or Software Product Identification.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

D.C. and A.C. Operating Range

		AT29C256-12	AT29C256-15	AT29C256-20	AT29C256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H [3]	V_{IL}	X	High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A14=V_{IL}, A9=V_H, A0=V_{IL}	Manufacturer Code[4]
				A1-A14=V_{IL}, A9=V_H, A0=V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0V \pm 0.5V$.
4. Manufacturer Code: 1F, Device Code: DC

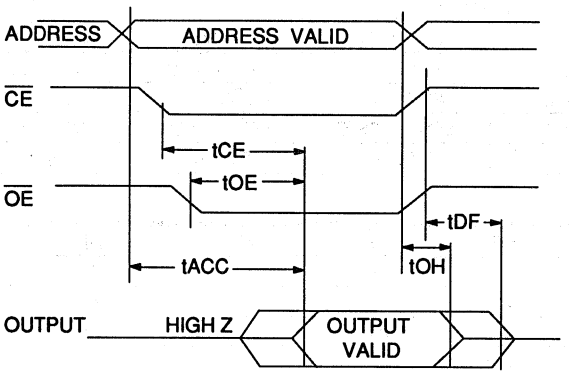
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH1}	Output High Voltage	I_{OH}=-400µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH}=-100µA;V_{CC}=4.5V	4.2		V

A.C. Read Characteristics

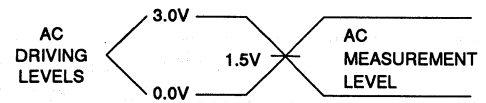
Symbol	Parameter	AT29C256-12		AT29C256-15		AT29C256-20		AT29C256-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



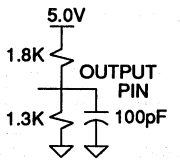
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

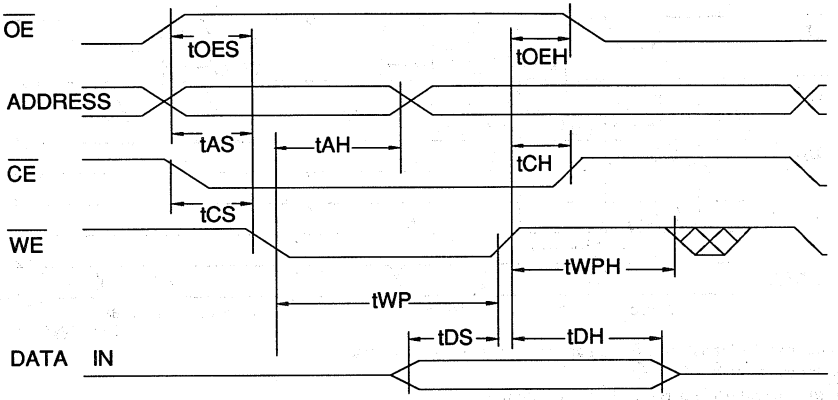
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Byte Load Characteristics

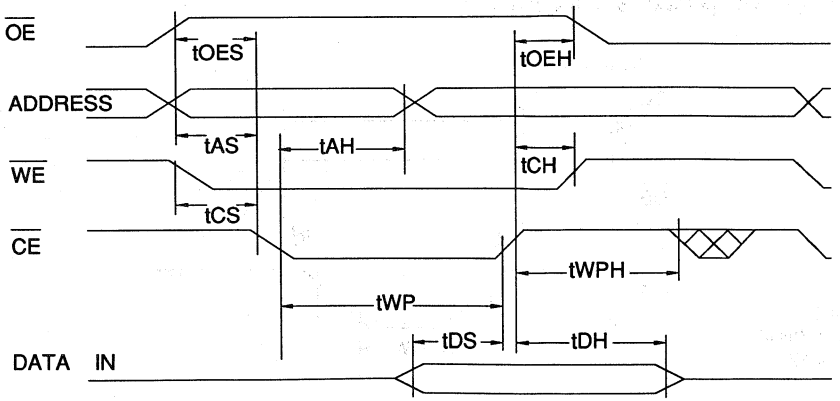
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

3

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



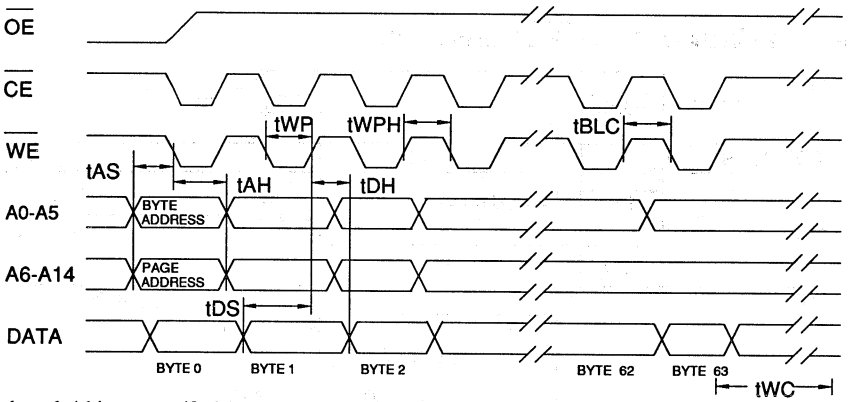
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

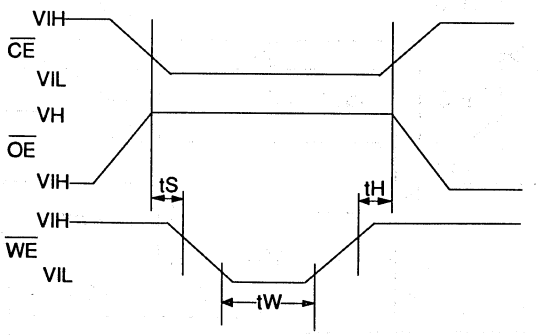
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms



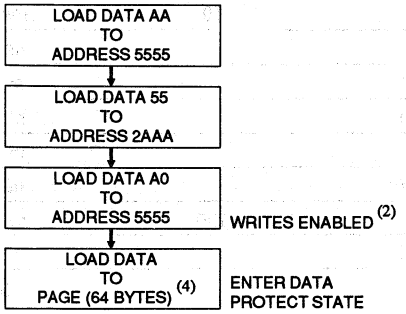
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

High Voltage Chip Erase Waveforms

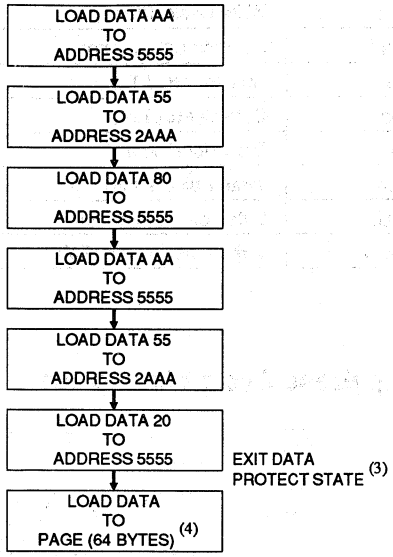


$t_S = 5\mu sec$ (min.)
$t_W = t_H = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

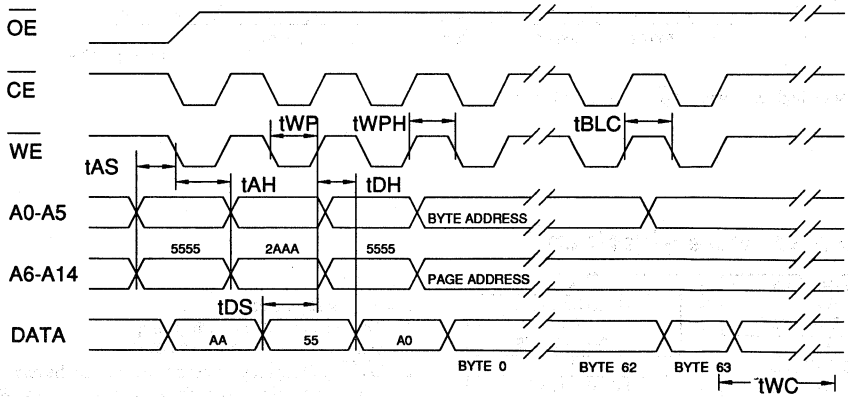


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data must be loaded.

Software Protected Program Cycle Waveform

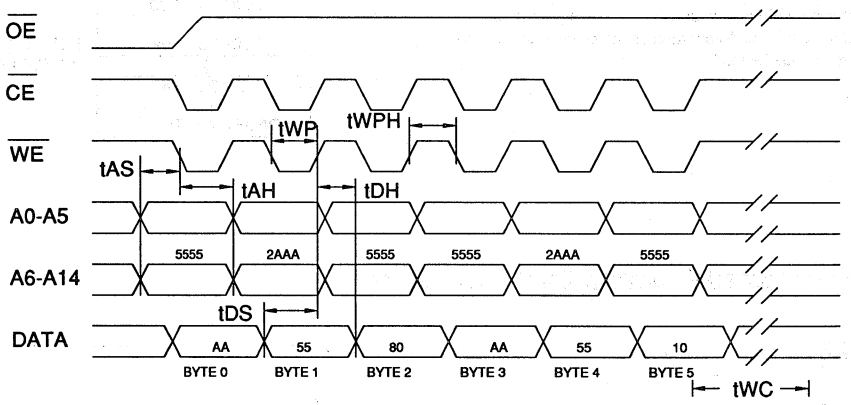


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Chip Erase Cycle Characteristics

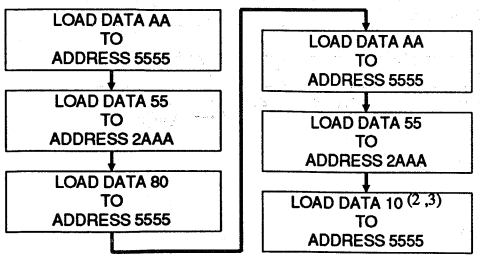
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Software Algorithm[1]



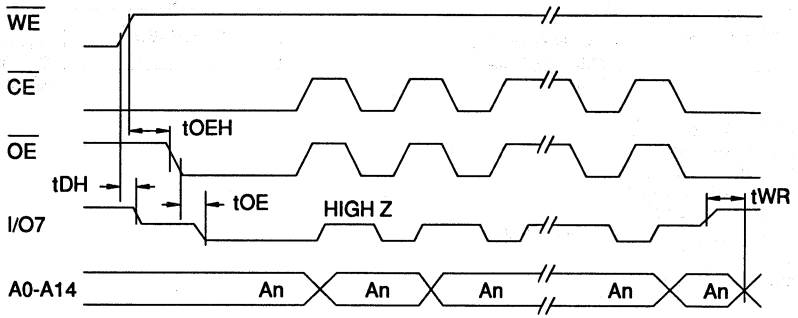
Notes for software erase code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. $\overline{DATA}$ polling may be used to determine the end of the erase cycle by checking any address for data equal to FF.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

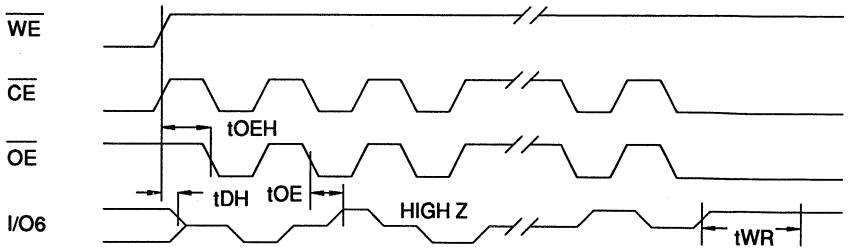


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

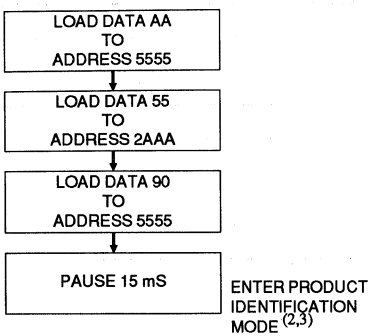
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

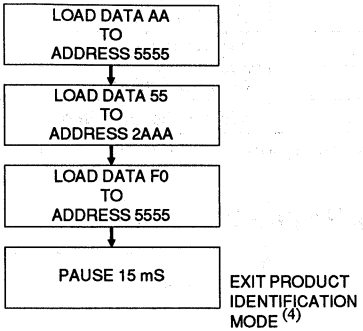


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

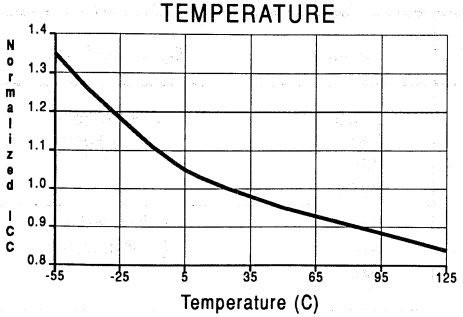


Software Product Identification Exit [1]

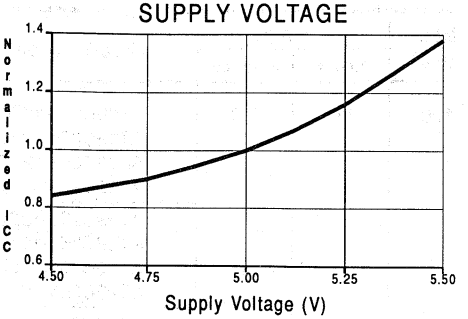


Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Manufacture code is read for A0 = V_{IL}
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

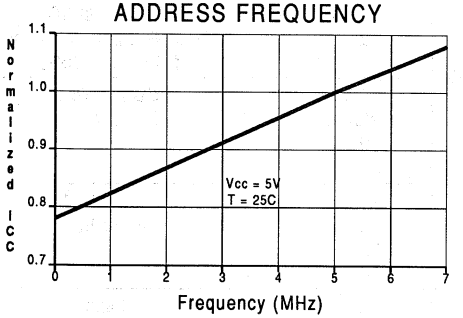
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT29C256-12DC AT29C256-12JC AT29C256-12LC AT29C256-12PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-12DI AT29C256-12JI AT29C256-12LI AT29C256-12PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-12DM AT29C256-12LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-12DM/883 AT29C256-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT29C256-15DC AT29C256-15JC AT29C256-15LC AT29C256-15PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-15DI AT29C256-15JI AT29C256-15LI AT29C256-15PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-15DM AT29C256-15LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-15DM/883 AT29C256-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C256-20DC AT29C256-20JC AT29C256-20LC AT29C256-20PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-20DI AT29C256-20JI AT29C256-20LI AT29C256-20PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-20DM AT29C256-20LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-20DM/883 AT29C256-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C256-25DC AT29C256-25JC AT29C256-25LC AT29C256-25PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-25DI AT29C256-25JI AT29C256-25LI AT29C256-25PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.3	AT29C256-25DM AT29C256-25LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-25DM/883 AT29C256-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

256K (32K x 8) 5-Volt Only CMOS PEROM

Preliminary

Features

- **Fast Read Access Time - 120ns**
- **Five Volt Only Reprogramming**
- **Page Program Operation**
  - **Single Cycle Reprogram (Erase and Program)**
  - **Internal Address and Data Latches for 64 Bytes**
- **Fast Program Cycle Times**
  - **Page (64 Byte) Program Time - 10ms**
  - **Chip Erase Time - 10ms**
- **Internal Program Control Timer**
- **Low Power Dissipation**
  - **80mA Active Current**
  - **300µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **DATA Polling for End of Program Detection**
- **High Reliability CMOS Technology**
  - **1000 Erase/Program Cycles**
  - **10 Year Data Retention**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Full Military, Commercial, and Industrial Temperature Ranges**

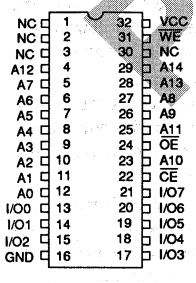
Description

The AT29C257 is a 5 volt only in system Programmable and Erasable Read Only Memory (PEROM). Its 256k of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 120ns with power dissipation of just 440mW. When the device is deselected, the CMOS standby current is less than 300µA.

To allow for simple in-system reprogrammability, the AT29C257 does not require high input voltages for programming. Five volt only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C257 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six byte software code (although erasure before programming is not needed).

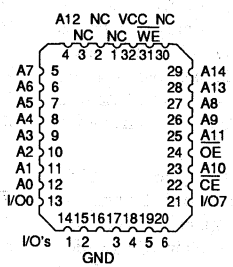
During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations

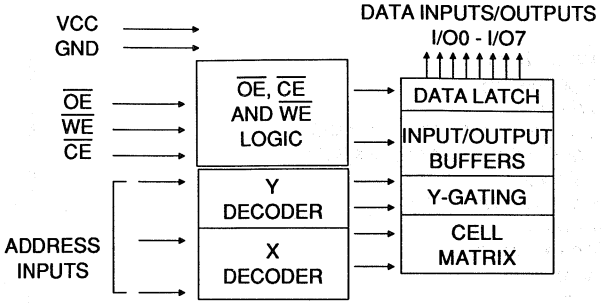


Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Notes:
1. PLCC package pin 30 is a DON'T CONNECT.
2. To upgrade to the 1M 29C010, pin 3 is A15 and pin 2 is A16.



Block Diagram



Device Operation

READ: The AT29C257 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

$\overline{DATA}$ POLLING: The AT29C257 features $\overline{DATA}$ Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT29C257 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C257 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical), the program function is inhibited. (b) Vcc power on delay— once Vcc has reached the Vcc sense level, the device will automatically time out 5ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C257. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

5 VOLT CHIP ERASE: The entire device may be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required.

HIGH VOLTAGE CHIP ERASE: The contents of the entire device may be set to the high state by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high; when $\overline{WE}$ is pulsed low for a minimum of 10ms, the contents of the entire device is erased.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware or software operation. For details, see Operating Modes or Software Product Identification.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

D.C. and A.C. Operating Range

		AT29C257-12	AT29C257-15	AT29C257-20	AT29C257-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X(1)	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H (3)	V_{IL}	X	High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A14=V_{IL}, A9=V_H, A0=V_{IL}	Manufacturer Code(4)
				A1-A14=V_{IL}, A9=V_H, A0=V_{IH}	Device Code(4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: DC

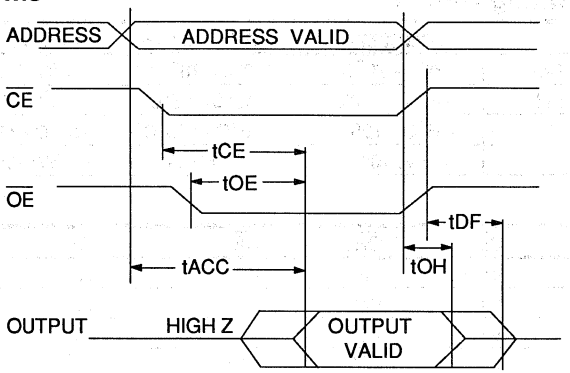
D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f=5MHz; I_{OUT}=0mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH1}	Output High Voltage	I_{OH}=-400µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH}=-100µA;V_{CC}=4.5V	4.2		V

A.C. Read Characteristics

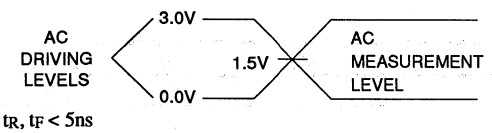
Symbol	Parameter	AT29C257-12		AT29C257-15		AT29C257-20		AT29C257-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



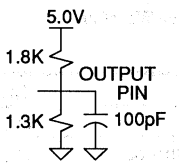
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

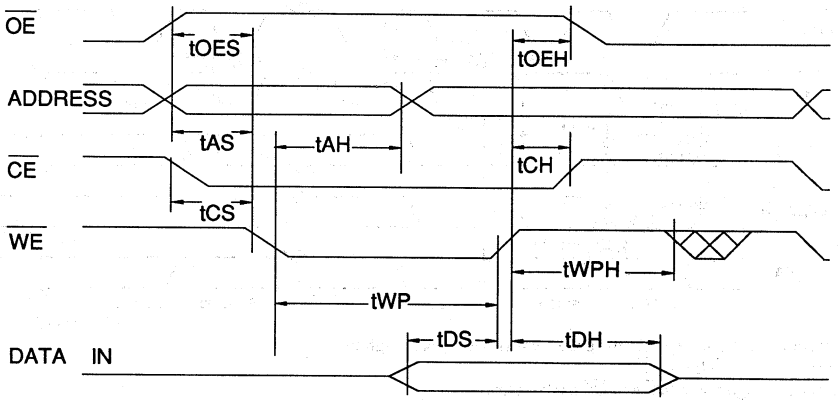
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Byte Load Characteristics

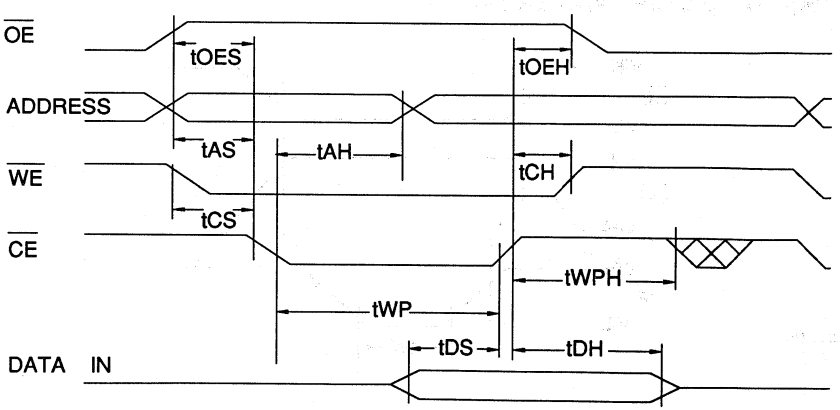
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

3

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



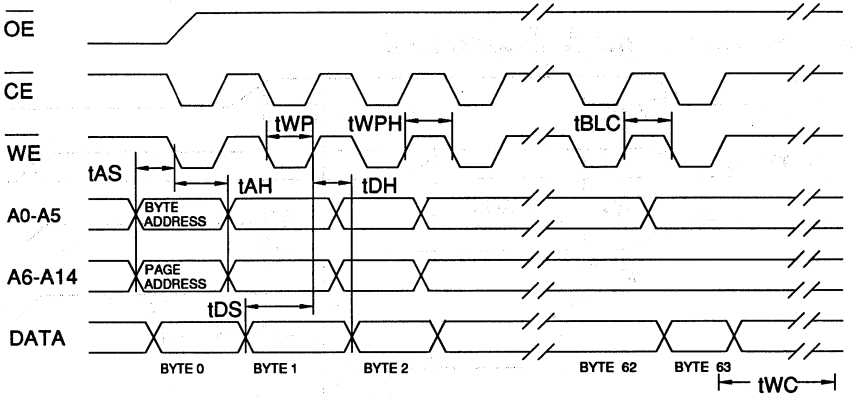
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

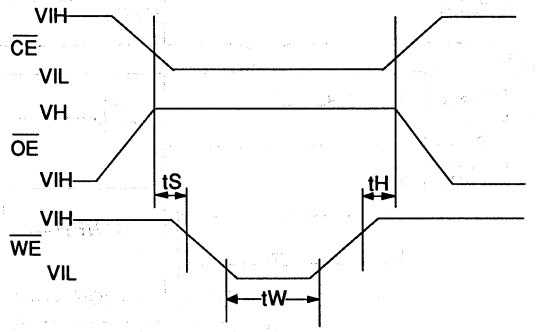
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms



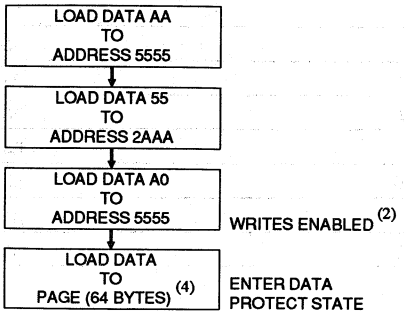
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

High Voltage Chip Erase Waveforms

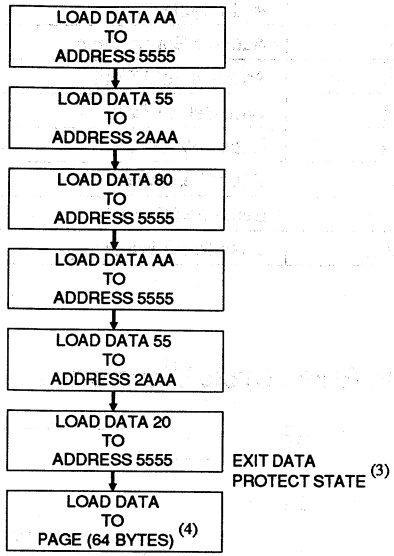


$t_S = 5\mu sec$ (min.)
$t_W = t_H = 10msec$ (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm [1]

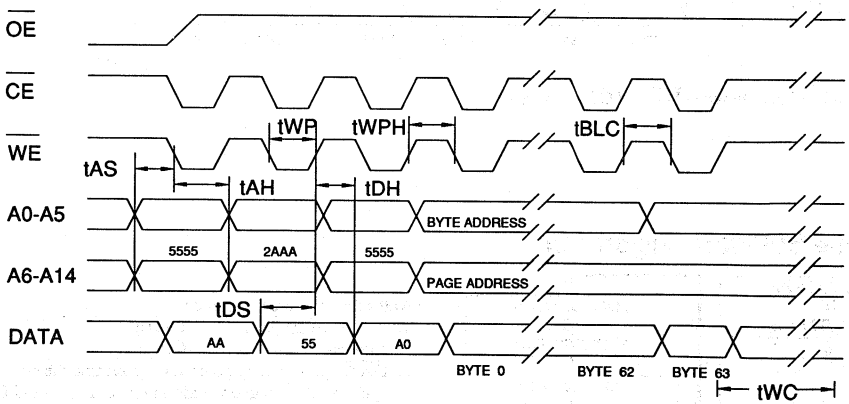


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data must be loaded.

Software Protected Program Cycle Waveform

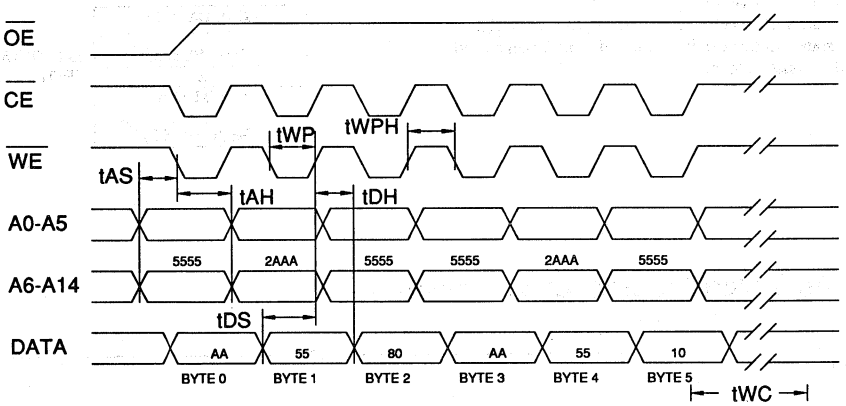


Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Chip Erase Cycle Characteristics

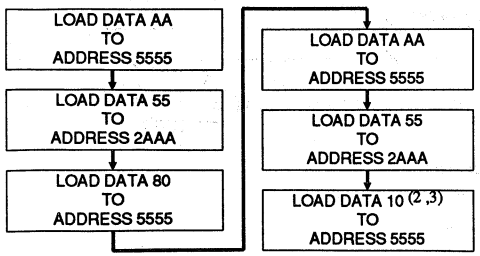
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Software Algorithm[1]



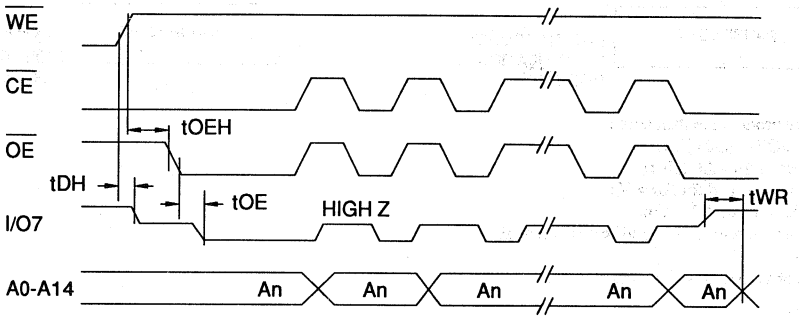
Notes for software erase code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. $\overline{DATA}$ polling may be used to determine the end of the erase cycle by checking any address for data equal to FF.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within t_{WC}.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

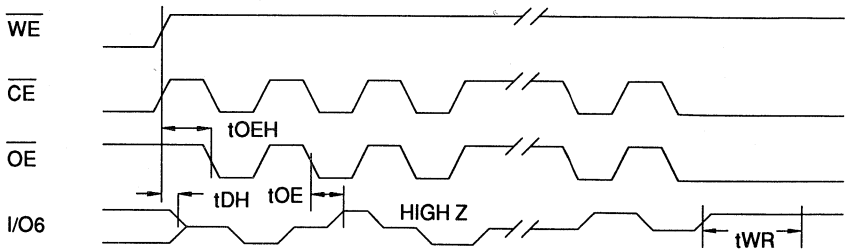


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

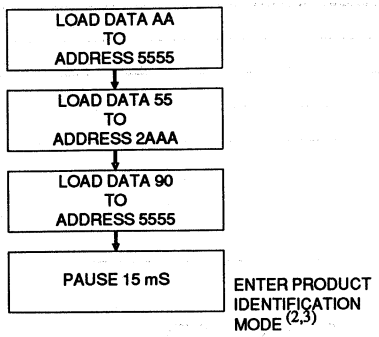
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

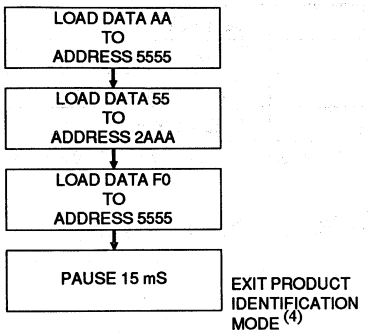


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]



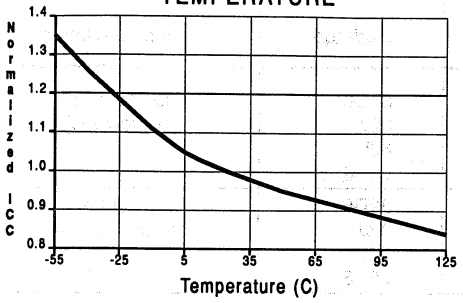
Software Product Identification Exit [1]



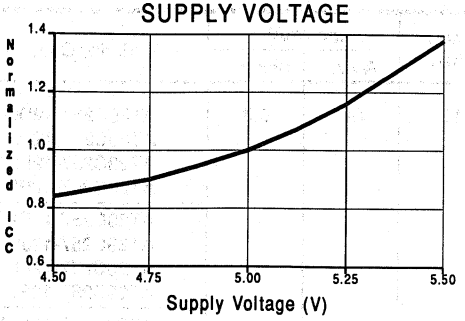
Notes for software product identification:

1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Manufacture code is read for A0 = V_{IL}
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.

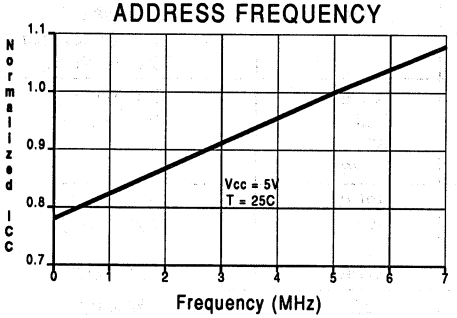
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



3

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	80	0.3	AT29C257-12DC AT29C257-12JC AT29C257-12LC AT29C257-12PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-12DI AT29C257-12JI AT29C257-12LI AT29C257-12PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C257-12DM	32D6	Military (-55°C to 125°C)
			AT29C257-12DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT29C257-15DC AT29C257-15JC AT29C257-15LC AT29C257-15PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-15DI AT29C257-15JI AT29C257-15LI AT29C257-15PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C) (-40° to 85°C)
			AT29C257-15DM	32D6	Military (-55°C to 125°C)
			AT29C257-15DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C257-20DC AT29C257-20JC AT29C257-20LC AT29C257-20PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-20DI AT29C257-20JI AT29C257-20LI AT29C257-20PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C257-20DM	32D6	Military (-55°C to 125°C)
			AT29C257-20DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT29C257-25DC AT29C257-25JC AT29C257-25LC AT29C257-25PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
			AT29C257-25DI AT29C257-25JI AT29C257-25LI AT29C257-25PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.3	AT29C257-25DM	32D6	Military (-55°C to 125°C)
			AT29C257-25DM/883	32D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

- Fast Read Access Time - 120 ns
- Five-Volt-Only Reprogramming
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - Internal Address and Data Latches for 128 Bytes
- Fast Program Cycle Times
  - Page Program Time - 10 ms
  - Chip Erase Time - 20 ms
- Internal Program Control Timer
- Low Power Dissipation
  - 50 mA Active Current
  - 100 µA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Program Detection
- High Reliability CMOS Technology
  - 1000 Erase/Program Cycles
  - 10 Year Data Retention
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Full Military, Commercial, and Industrial Temperature Ranges

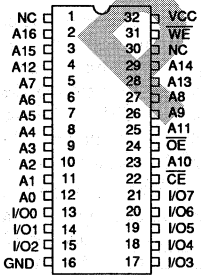
Description

The AT29C010 is a 5-volt-only in-system Programmable and Erasable Read Only Memory (PEROM). Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced non-volatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 275 mW. When the device is deselected, the CMOS standby current is less than 100 µA.

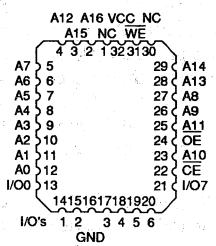
To allow for simple in-system reprogrammability, the AT29C010 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C010 is performed on a page basis; 128 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by DATA polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Pin Configurations



Pin Name	Function
A0 - A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect



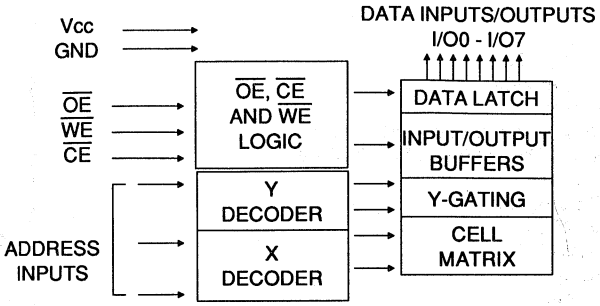
Note: PLCC package pin 30 is a DON'T CONNECT.

1 Megabit (128K x 8) 5-Volt Only CMOS PEROM

Preliminary

3

Block Diagram



Device Operation

READ: The AT29C010 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 128 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A7 to A16 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

$\overline{DATA}$ POLLING: The AT29C010 features $\overline{DATA}$ Polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT29C010 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C010 in the following ways: (a) Vcc sense— if Vcc is below 3.8V (typical), the program function is inhibited. (b) Vcc power on delay— once Vcc has reached the Vcc sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C010. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

5 VOLT CHIP ERASE: The entire device may be erased at one time by using a six byte software code. The erase code consists of six byte load commands to specific address locations with specific data patterns. Once the code has been entered, the device will set each byte to the high state (FFh). After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required.

OPTIONAL HIGH VOLTAGE CHIP ERASE: The contents of the entire device may be set to the high state by using an externally timed high voltage operation. $\overline{OE}$ is first raised to 12 volts with $\overline{CE}$ low and $\overline{WE}$ high; when $\overline{WE}$ is pulsed low for a minimum of 20 ms, the contents of the entire device is erased.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

D.C. and A.C. Operating Range

		AT29C010-12	AT29C010-15	AT29C010-20	AT29C010-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X(1)	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H (3)	V_{IL}	X	High Z
Product Identification	V_{IL}	V_{IL}	V_{IH}	A1-A16=V_{IL}, A9=V_H, A0=V_{IL}	
				A1-A16=V_{IL}, A9=V_H, A0=V_{IL}	Device Code(4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1F, Device Code: D5

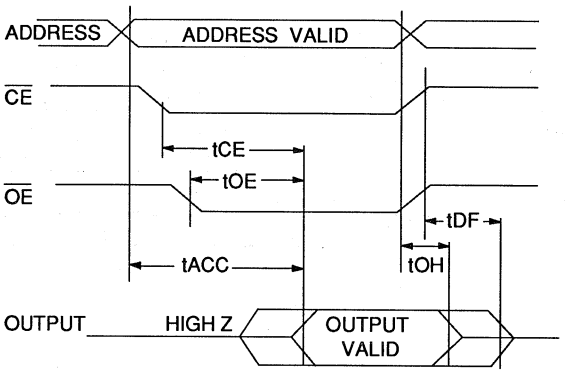
D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$=V_{CC}-.3V to V_{CC}	Com.		100	µA
			Ind., Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$=2.0V to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current	f=5 MHz; I_{OUT}=0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=2.1 mA			.45	V
V_{OH1}	Output High Voltage	I_{OH}=-400 µA		2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH}=-100 µA;V_{CC}=4.5V		4.2		V

A.C. Read Characteristics

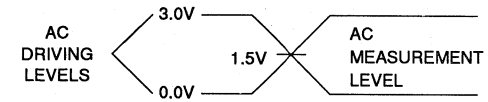
Symbol	Parameter	AT29C010-12		AT29C010-15		AT29C010-20		AT29C010-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		120		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	40	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

A.C. Read Waveforms



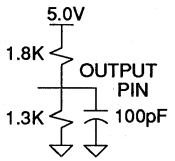
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f=1MHz T=25°C) (4)

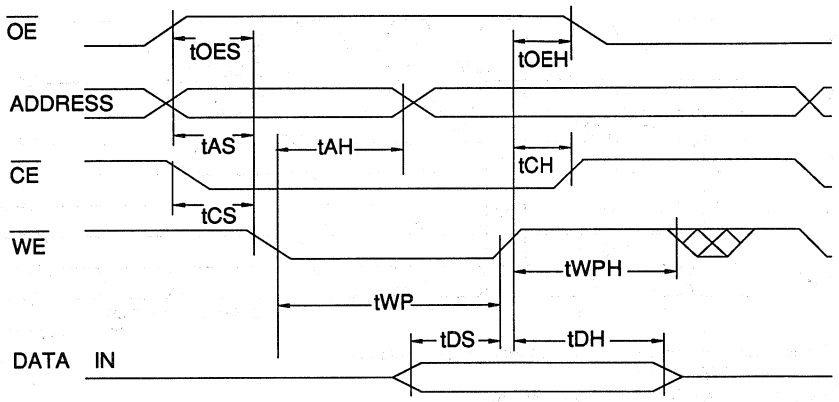
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Byte Load Characteristics

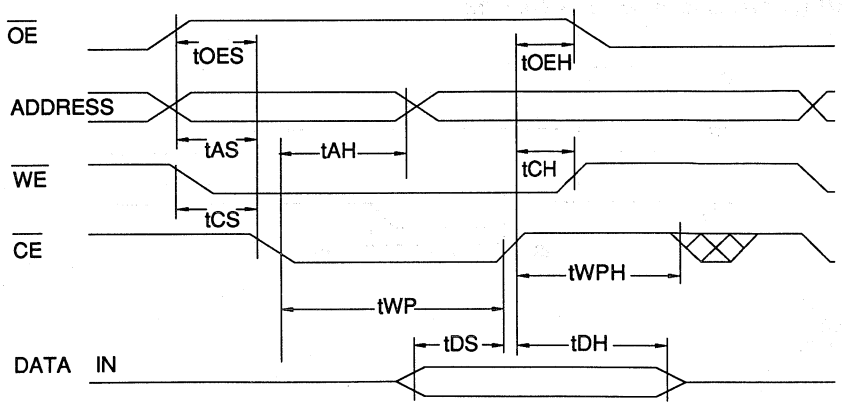
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WC}	Write Cycle Time		10	ms

3

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled



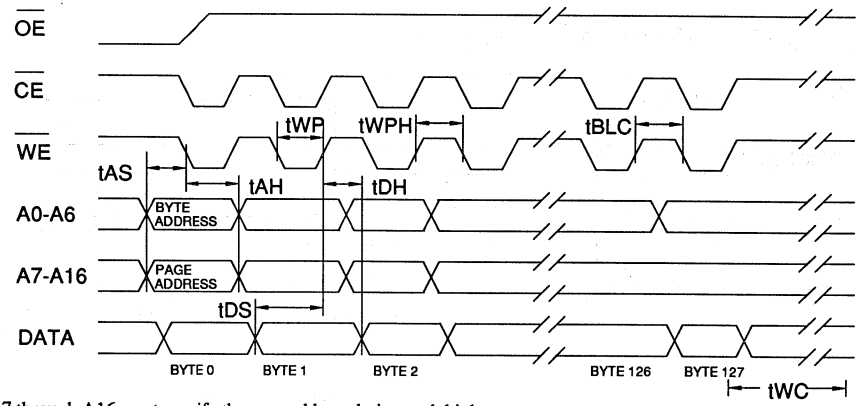
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled



Program Cycle Characteristics

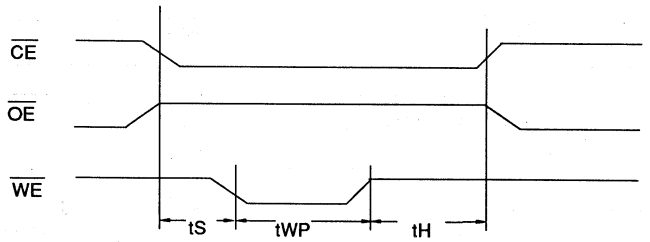
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Program Cycle Waveforms



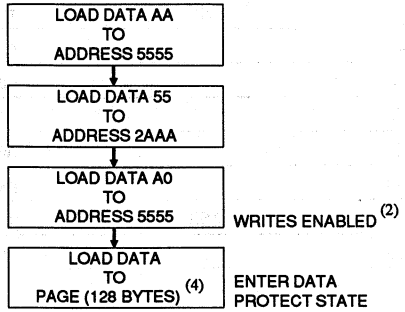
Notes: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

High Voltage Chip Erase Waveforms

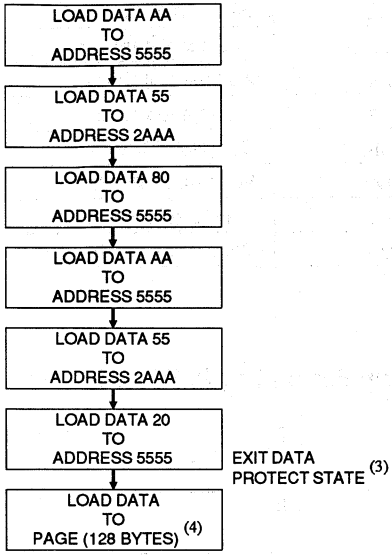


t_S = 5 µs (min.)
t_{WP} = 150 ns (min.)
t_H = 20 ms (min)
V_H = 12.0V ± 0.5V

Software Data Protection Enable Algorithm [1]

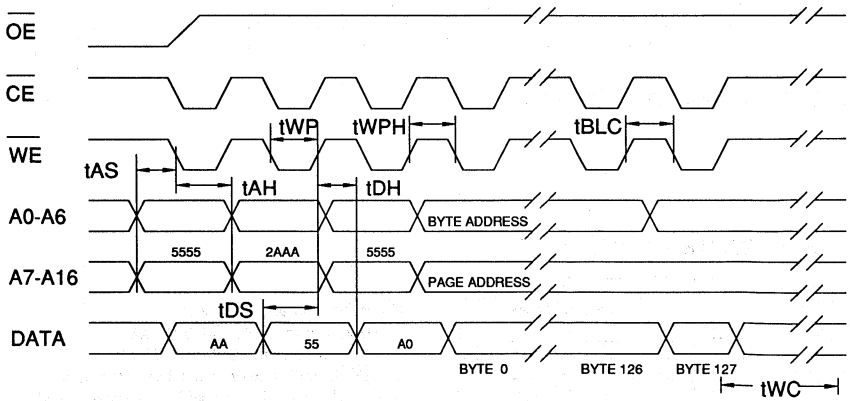


Software Data Protection Disable Algorithm [1]



Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 128 bytes of data are loaded.

Software Protected Program Cycle Waveform

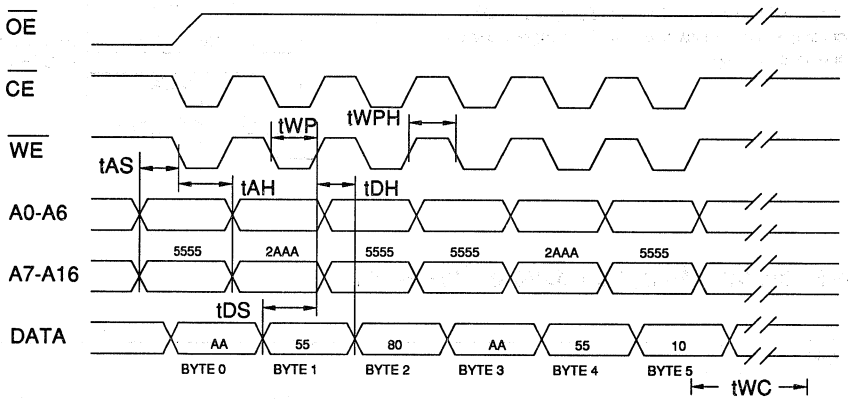


Notes: A7 through A16 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
All bytes that are not loaded within the page being programmed will be erased to FF.

Chip Erase Cycle Characteristics

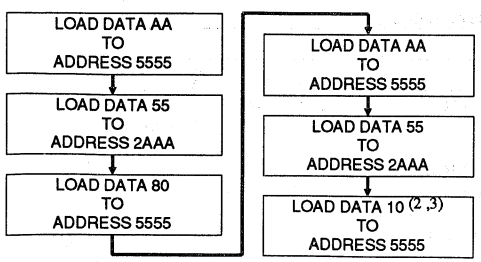
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		20	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	100		ns

Chip Erase Cycle Waveforms



Note: $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Software Algorithm[1]



Notes for software erase code:

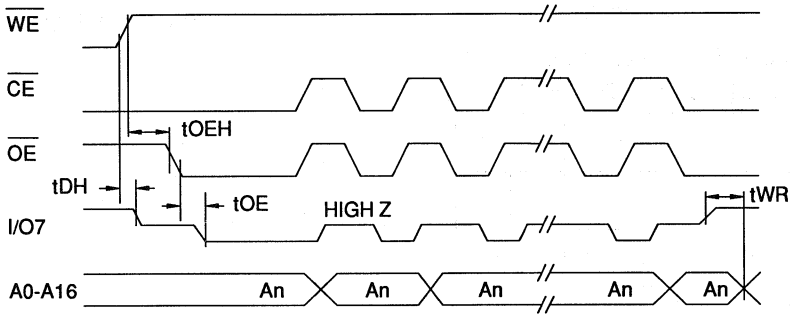
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. $\overline{DATA}$ polling may be used to determine the end of the erase cycle by checking any address for data equal to FF.
3. After loading the six byte code, no byte loads are allowed until the completion of the erase cycle. The erase cycle will time itself to completion within twc.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms

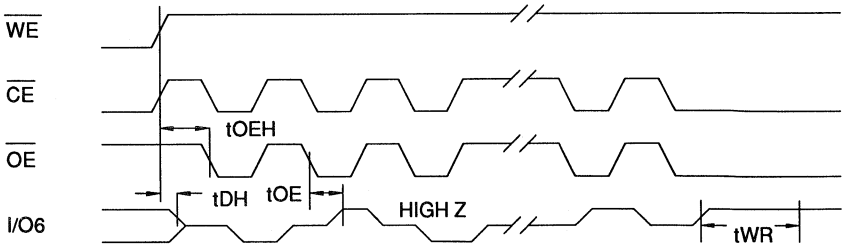


Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

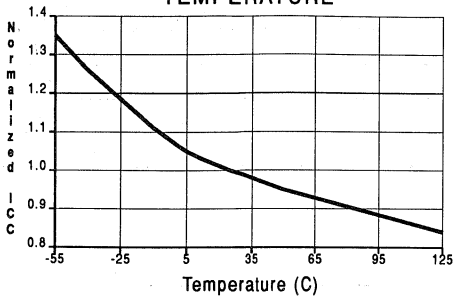
Note: 1. These parameters are characterized and not 100% tested.

Toggle Bit Waveforms

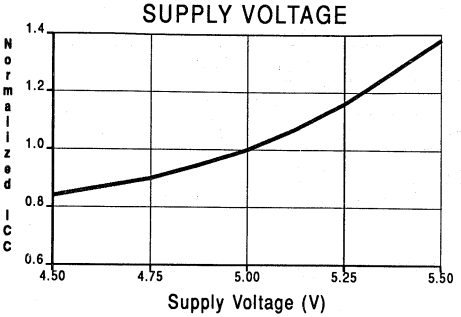


Notes:
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

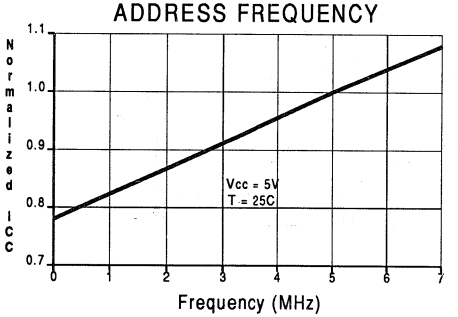
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT29C010-12DC AT29C010-12JC AT29C010-12LC AT29C010-12PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
	50	0.3	AT29C010-12DI AT29C010-12JI AT29C010-12LI AT29C010-12PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
150	50	0.1	AT29C010-15DC AT29C010-15JC AT29C010-15LC AT29C010-15PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
	50	0.3	AT29C010-15DI AT29C010-15JI AT29C010-15LI AT29C010-15PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-15DM AT29C010-15LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-15DM/883 AT29C010-15LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	AT29C010-20DC AT29C010-20JC AT29C010-20LC AT29C010-20PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
	50	0.3	AT29C010-20DI AT29C010-20JI AT29C010-20LI AT29C010-20PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-20DM AT29C010-20LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-20DM/883 AT29C010-20LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	50	0.1	AT29C010-25DC AT29C010-25JC AT29C010-25LC AT29C010-25PC	32D6 32J 32L 32P6	Commercial (0° to 70°C)
	50	0.3	AT29C010-25DI AT29C010-25JI AT29C010-25LI AT29C010-25PI	32D6 32J 32L 32P6	Industrial (-40° to 85°C)
			AT29C010-25DM AT29C010-25LM	32D6 32L	Military (-55°C to 125°C)
			AT29C010-25DM/883 AT29C010-25LM/883	32D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
32D6	32 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

ATMEL

Section 4

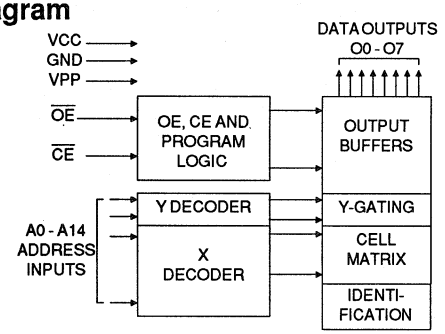
CMOS EPROMs

256K (32K x 8) UV Erasable CMOS EPROM

Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 90ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC
  - 32-Lead JLCC and OTP PLCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with AT27C256

Block Diagram



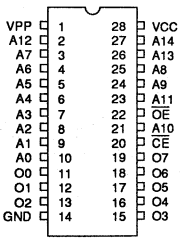
Description

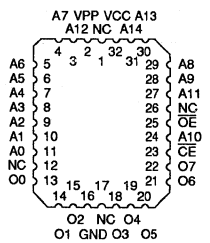
The AT27C256R chip is a low-power, high performance 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 32K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 90ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

The AT27C256R meets or exceeds all specifications for the AT27C256. Atmel's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10µA in Standby.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect





Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C256R comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), 32-pad ceramic leadless chip carrier (LCC), and 32 lead ceramic (JLCC),or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 32K byte storage capability, the AT27C256R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C256R				
		-90	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$=2.0 to V_{CC}+1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f=5MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-2.5mA		3.5		V
		I_{OH}=-400µA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC}=5±0.25V		3.8	V_{CC}+.3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

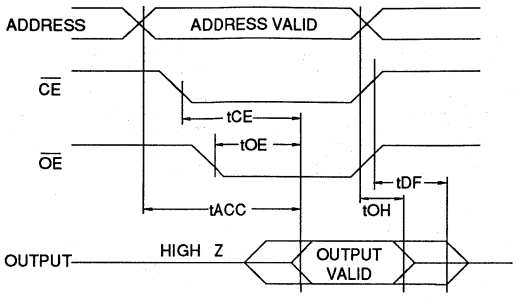
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C256R										
				-90		-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		90		120		150		200		250	ns
			Ind.,Mil.		90		120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			90		120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			40		50		60		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$=V_{IL}			30		30		45		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0		0	ns

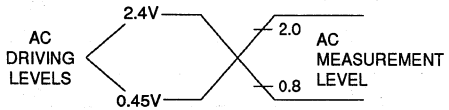
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



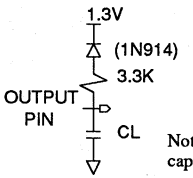
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



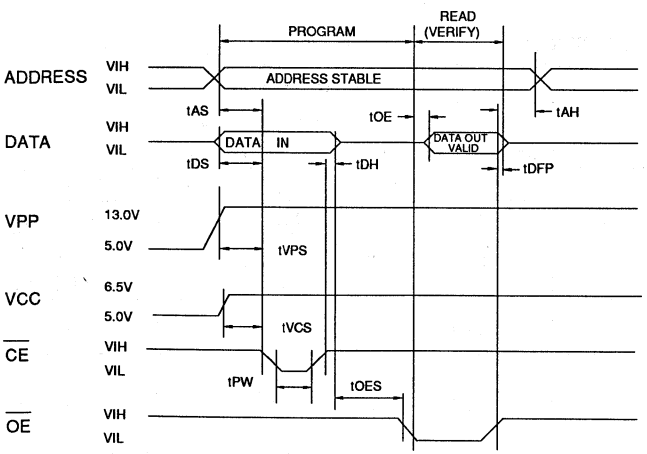
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C256R a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

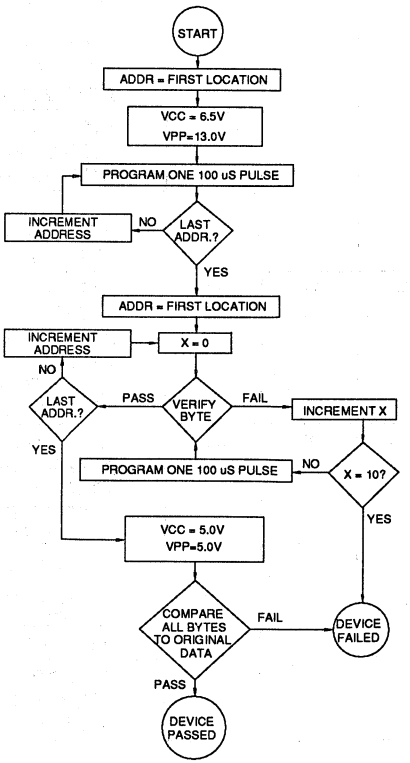
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C256R Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	20	0.1	AT27C256R-90DC AT27C256R-90JC AT27C256R-90KC AT27C256R-90LC AT27C256R-90PC AT27C256R-90RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
90	25	0.2	AT27C256R-90DI AT27C256R-90JI AT27C256R-90KI AT27C256R-90LI AT27C256R-90PI AT27C256R-90RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
120	20	0.1	AT27C256R-12DC AT27C256R-12JC AT27C256R-12KC AT27C256R-12LC AT27C256R-12PC AT27C256R-12RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
120	25	0.2	AT27C256R-12DI AT27C256R-12JI AT27C256R-12KI AT27C256R-12LI AT27C256R-12PI AT27C256R-12RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-12DM AT27C256R-12KM AT27C256R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-12DM/883 AT27C256R-12KM/883 AT27C256R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	20	0.1	AT27C256R-15DC AT27C256R-15JC AT27C256R-15KC AT27C256R-15LC AT27C256R-15PC AT27C256R-15RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
150	25	0.2	AT27C256R-15DI AT27C256R-15JI AT27C256R-15KI AT27C256R-15LI AT27C256R-15PI AT27C256R-15RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-15DM AT27C256R-15KM AT27C256R-15LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-15DM/883 AT27C256R-15KM/883 AT27C256R-15LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
170	20	0.1	AT27C256R-17DC AT27C256R-17JC AT27C256R-17KC AT27C256R-17LC AT27C256R-17PC AT27C256R-17RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
170	25	0.2	AT27C256R-17DI AT27C256R-17JI AT27C256R-17KI AT27C256R-17LI AT27C256R-17PI AT27C256R-17RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-17DM AT27C256R-17KM AT27C256R-17LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-17DM/883 AT27C256R-17KM/883 AT27C256R-17LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C256R-20DC AT27C256R-20JC AT27C256R-20KC AT27C256R-20LC AT27C256R-20PC AT27C256R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	25	0.2	AT27C256R-20DI AT27C256R-20JI AT27C256R-20KI AT27C256R-20LI AT27C256R-20PI AT27C256R-20RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C256R-20DM AT27C256R-20KM AT27C256R-20LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-20DM/883 AT27C256R-20KM/883 AT27C256R-20LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C256R-25DC AT27C256R-25JC AT27C256R-25KC AT27C256R-25LC AT27C256R-25PC AT27C256R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	25	0.2	AT27C256R-25DI AT27C256R-25JI AT27C256R-25KI AT27C256R-25LI AT27C256R-25PI AT27C256R-25RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)

Ordering Information

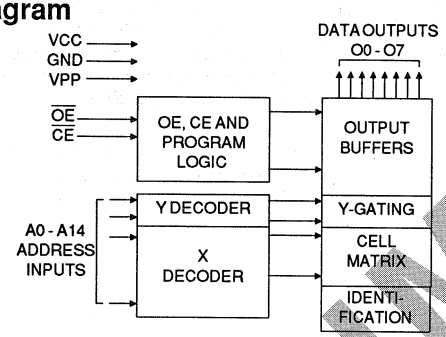
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	25	0.2	AT27C256R-25DM AT27C256R-25KM AT27C256R-25LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C256R-25DM/883 AT27C256R-25KM/883 AT27C256R-25LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.2	5962-86063 05 XX 5962-86063 05 YX 5962-86063 05 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	25	0.2	5962-86063 04 XX 5962-86063 04 YX 5962-86063 04 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.2	5962-86063 01 XX 5962-86063 01 YX 5962-86063 01 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.2	5962-86063 02 XX 5962-86063 02 YX 5962-86063 02 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	25	0.2	5962-86063 03 XX 5962-86063 03 YX 5962-86063 03 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

Features

- Bipolar Speed in JEDEC Standard EPROM Pinout
  - Read Access Time - 55ns
  - 28-Lead 600 mil CERDIP and OTP Plastic DIP
  - 32-Pad LCC, JLCC and OTP PLCC
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 50 mA max. Active at 10 MHz
- High Output Drive Capability
- High Reliablity Latch-Up Resistant CMOS Technology
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges
- Fully Compatible with AT27HC256/L

Block Diagram



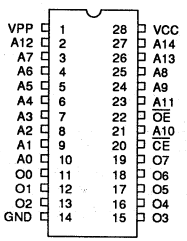
Description

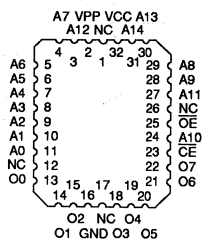
The AT27HC256R/RL chip family is a high-speed, low-power 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. The AT27HC256R is suited for very high-speed applications, while the AT27HC256RL features low Vcc Standby Current. Both require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 55ns on the AT27HC256, making this part ideal for high-performance systems. Power consumption is typically only 35mA in Active Mode on both parts, and less than 10µA in Standby Mode on the AT27HC256RL or 15mA on the AT27HC256R.

Atmel's 1.2-micron, high-speed CMOS technology provides optimum speed, lower power and high noise immunity. The high-speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly EPROM technology.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect
O0-O7	Outputs





Note: PLCC package pins 1 and 17 are DON'T CONNECT.

256K (32K x 8) High Speed UV Erasable CMOS EPROM

4

Preliminary

Description (Continued)

The AT27HC256R/256RL come in a choice of industry standard JEDEC-approved packages including: 28-pin DIP ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC), or OTP plastic (PLCC) J-leaded chip carrier. The device features two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With a storage capacity of 32K bytes, Atmel's 27HC256R / 256RL allow firmware to be stored reliably and to be accessed at very high speeds. The AT27HC256R/256RL have exceptional output drive capability - source 4mA and sink 16mA per output.

The AT27HC256R/256RL have additional features to ensure high-quality and efficient production use. The Rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27HC256R/256RL is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC256R	AT27HC256R / AT27HC256RL		
		-55	-70	-90	-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C(1)	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Notes: 1. AT27HC256R only.

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{PP} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V			20	µA
I_{SB1}/I_{SB2}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V	AT27HC256RL Com.		0.1/2	mA
			Ind.,Mil.		0.2/3	mA
		I_{SB2} (TTL) $\overline{CE}$=2.0 to V_{CC}+1.0V	AT27HC256R Com.		30/35	mA
			Ind.,Mil.		30/35	mA
I_{CC}	V_{CC} Active Current	f=10MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	Com.		50	mA
			Ind.,Mil.		55	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=16mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-2.5mA		3.5		V
		I_{OH}=-4.0mA		2.4		V
V_{PP}	V_{PP} Read Voltage	V_{CC}=5 ± 0.5V		3.8	V_{CC}+0.3	V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

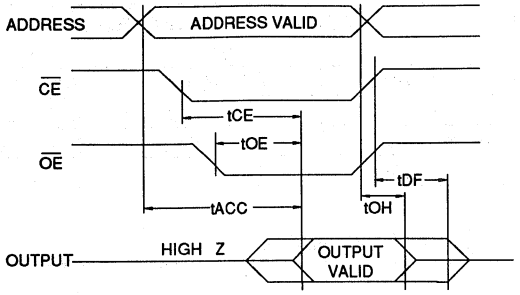
A.C. Characteristics for Read Operation

				AT27HC256R		AT27HC256R / AT27HC256RL						
				-55		-70		-90		-12		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.,Ind.		55		70		90		120	ns
			Mil.				70(1)		90		120	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			55		70		90		120	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			25		30		30		35	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$=V_{IL}			25		30		30		35	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0	ns

Notes: 1. AT27HC256R only.

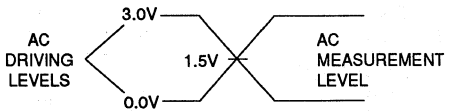
2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



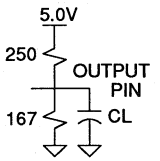
Notes:
1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
   C_L = 30pF, add 10ns for C_L = 100pF.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. t_{DF} is measured at V_{OH}-0.5V or V_{OL}+0.5V with C_L=5pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



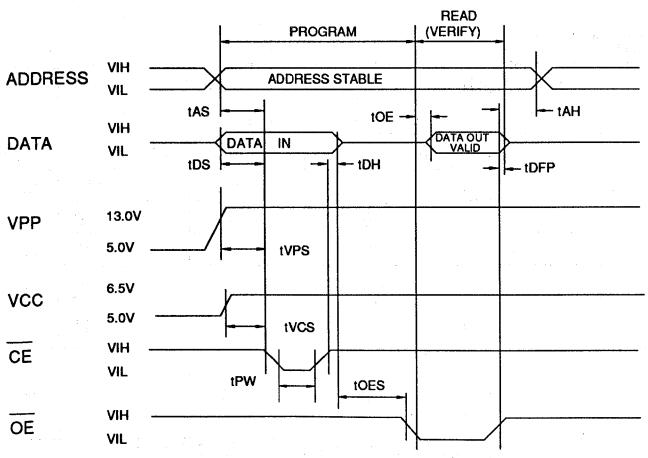
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC256R/256RL a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=16mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-4.0mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			60	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels .....0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:

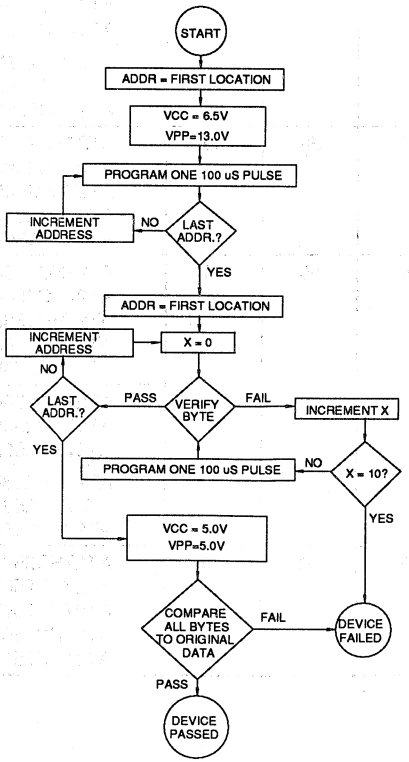
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27HC256R/RL Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	1	0	1	0	0	94

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	50	30	AT27HC256R-55DC AT27HC256R-55KC AT27HC256R-55LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
55	55	35	AT27HC256R-55DI AT27HC256R-55KI AT27HC256R-55LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
70	50	30	AT27HC256R-70DC AT27HC256R-70JC AT27HC256R-70KC AT27HC256R-70LC AT27HC256R-70PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
70	55	35	AT27HC256R-70DI AT27HC256R-70JI AT27HC256R-70KI AT27HC256R-70LI AT27HC256R-70PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256R-70DM AT27HC256R-70KM AT27HC256R-70LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256R-70DM/883 AT27HC256R-70KM/883 AT27HC256R-70LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	50	30	AT27HC256R-90DC AT27HC256R-90JC AT27HC256R-90KC AT27HC256R-90LC AT27HC256R-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	55	35	AT27HC256R-90DI AT27HC256R-90JI AT27HC256R-90KI AT27HC256R-90LI AT27HC256R-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256R-90DM AT27HC256R-90KM AT27HC256R-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256R-90DM/883 AT27HC256R-90KM/883 AT27HC256R-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	50	30	AT27HC256R-12DC AT27HC256R-12JC AT27HC256R-12KC AT27HC256R-12LC AT27HC256R-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	55	35	AT27HC256R-12DI AT27HC256R-12JI AT27HC256R-12KI AT27HC256R-12LI AT27HC256R-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256R-12DM AT27HC256R-12KM AT27HC256R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256R-12DM/883 AT27HC256R-12KM/883 AT27HC256R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	55	35	5962-86063 08 XX 5962-86063 08 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	0.1	AT27HC256RL-70DC AT27HC256RL-70KC AT27HC256RL-70LC	28DW6 32KW 32LW	Commercial (0°C to 70°C)
70	55	0.2	AT27HC256RL-70DI AT27HC256RL-70KI AT27HC256RL-70LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
90	50	0.1	AT27HC256RL-90DC AT27HC256RL-90JC AT27HC256RL-90KC AT27HC256RL-90LC AT27HC256RL-90PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
90	55	0.2	AT27HC256RL-90DI AT27HC256RL-90JI AT27HC256RL-90KI AT27HC256RL-90LI AT27HC256RL-90PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256RL-90DM AT27HC256RL-90KM AT27HC256RL-90LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256RL-90DM/883 AT27HC256RL-90KM/883 AT27HC256RL-90LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	50	0.1	AT27HC256RL-12DC AT27HC256RL-12JC AT27HC256RL-12KC AT27HC256RL-12LC AT27HC256RL-12PC	28DW6 32J 32KW 32LW 28P6	Commercial (0°C to 70°C)
120	55	0.2	AT27HC256RL-12DI AT27HC256RL-12JI AT27HC256RL-12KI AT27HC256RL-12LI AT27HC256RL-12PI	28DW6 32J 32KW 32LW 28P6	Industrial (-40°C to 85°C)
			AT27HC256RL-12DM AT27HC256RL-12KM AT27HC256RL-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27HC256RL-12DM/883 AT27HC256RL-12KM/883 AT27HC256RL-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	55	0.2	5962-86063 07 XX 5962-86063 07 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	55	0.2	5962-86063 06 XX 5962-86063 06 YX	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

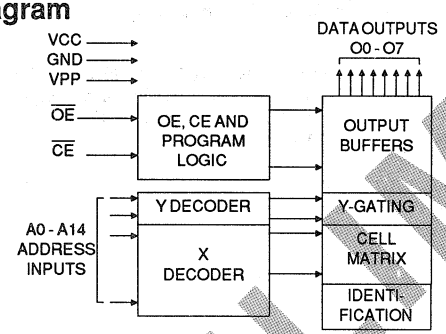
- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C256R
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26mW max. Active at 3.3 MHz for V_{CC} = 3.3 VDC
  - 110mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 300ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

256K (32K x 8) Low Voltage UV Erasable CMOS EPROM

Preliminary

4

Block Diagram



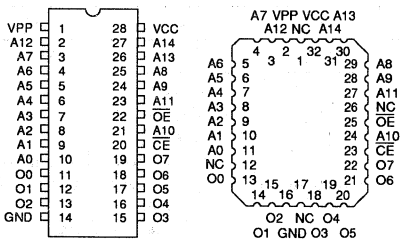
Description

The AT27LV256R chip is a low power, low voltage 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18mW at 3.3 MHz and V_{CC} at 3.3 VDC, the AT27LV256R will draw less than one fifth the power of a standard 5 volt EPROM. Standby mode supply current is typically less than 20µA.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT

Description (Continued)

The AT27LV256R comes in a choice of industry standard JEDEC-approved ceramic packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC) and 32-pad leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27LV256R operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV256R programs identically as an AT27C256R.

Erasure Characteristics

The entire memory array of the AT27LV256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is 6.5V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X(5)	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC} (2)	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (2)	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC} (2)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} Current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV256R -30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V_{CC} Power Supply		3.0V to 5.5V

D.C. and Operating Characteristics for Read Operation

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC}+0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}-0.7V to V_{CC}+0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0V			100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5V	Com.		20	mA
			Ind.		25	mA
		I_{CC2} f = 3.33MHz, I_{OUT} = 0mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3V	Com.		8	mA
			Ind.		10	mA
V_{IL}	Input Low Voltage	V_{IL1} 4.5 ≤ V_{CC} ≤ 5.5V		-0.6	0.8	V
		V_{IL2} 3.0 ≤ V_{CC} < 4.5V		-0.6	0.6	V
V_{IH}	Input High Voltage			2.0	6.5	V
V_{OL}	Output Low Voltage	V_{OL1} I_{OL} = 2.1mA, V_{CC} = 4.5V			.45	V
		V_{OL2} I_{OL} = 1.0mA, V_{CC} = 3.0V			0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -400µA		2.4		V

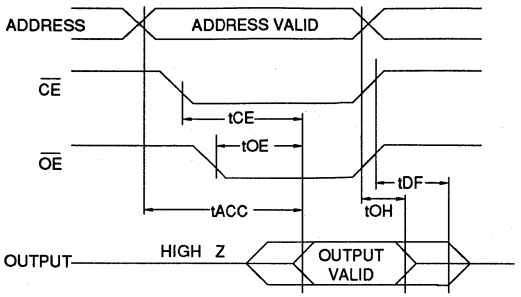
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation (V_{CC} = 3.0V to 5.5V)

Symbol	Parameter	Condition		AT27LV256R -30 Min	AT27LV256R -30 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}	Com.		270	ns
			Ind.		270	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			300	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			150	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			100	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$=V_{IL}			0	ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

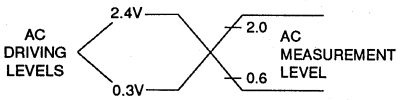
A.C. Waveforms for Read Operation [1]



Notes:
1. 3V timing measurement references are 0.6V and 2.0V. Input AC driving levels are 0.3V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

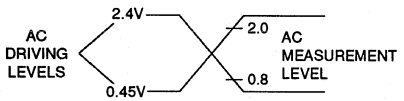
Input Test Waveforms and Measurement Levels

(V_{CC} = 3.0V)



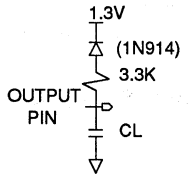
t_R, t_F < 20ns (10% to 90%)

(V_{CC} = 5.5V)



t_R, t_F < 20ns (10% to 90%)

Output Test Load



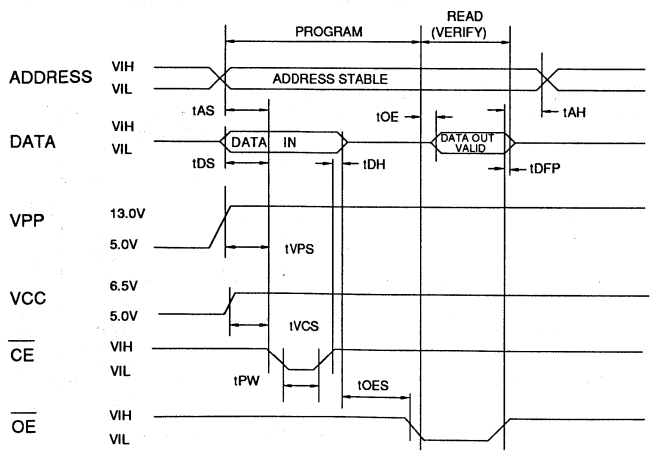
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for 5V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV256R a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

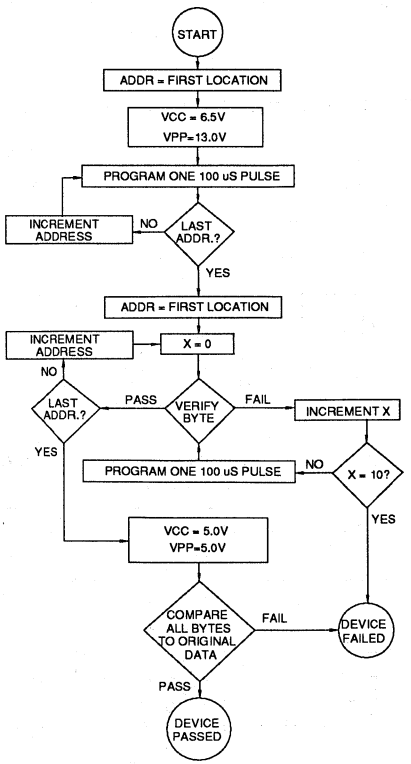
Atmel's 27LV256R Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27LV256R has the same Product Identification Code as the AT27C256R. Both are programming compatible.

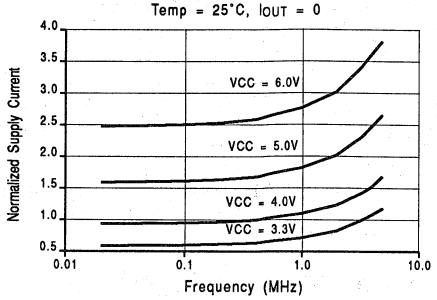
Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



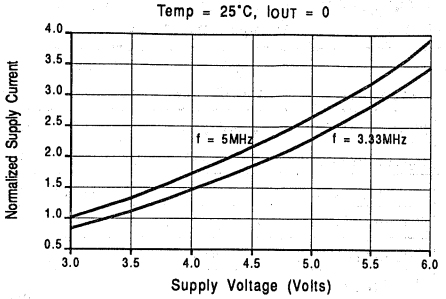
NORMALIZED SUPPLY CURRENT vs. FREQUENCY

Temp = 25°C, IOUT = 0

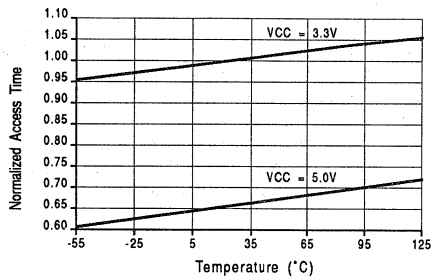


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

Temp = 25°C, IOUT = 0

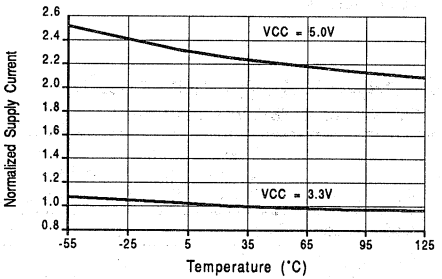


NORMALIZED ACCESS TIME vs. TEMPERATURE



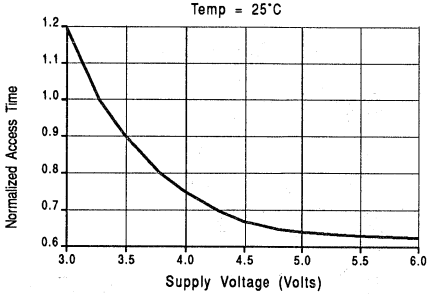
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

Frequency = 3.33MHz, IOUT = 0



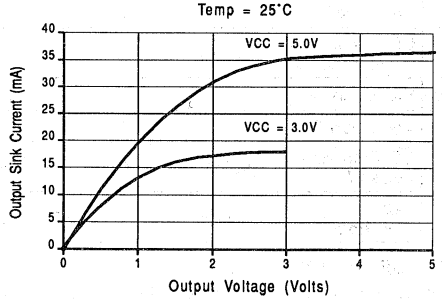
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

Temp = 25°C



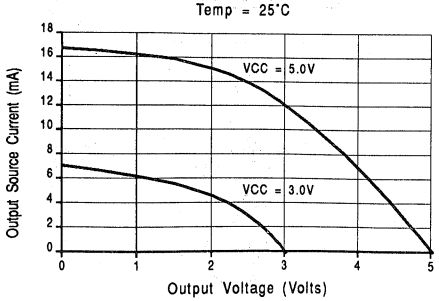
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active (3.3)	Standby			
270	8	0.1	AT27LV256R-30DC AT27LV256R-30JC AT27LV256R-30LC AT27LV256R-30PC AT27LV256R-30RC	28DW6 32J 32LW 28P6 28R	Commercial (0°C to 70°C)
270	10	0.1	AT27LV256R-30DI AT27LV256R-30LI	28DW6 32LW	Industrial (-40°C to 85°C)

4

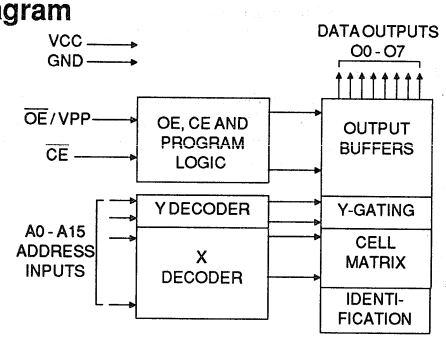
Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

512K (64K x 8) UV Erasable CMOS EPROM

Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 100ns
- Wide Selection of JEDEC Standard Packages including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC
  - 32-Lead JLCC and OTP PLCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with AT27C512

Block Diagram



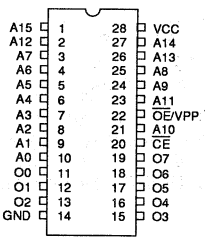
Description

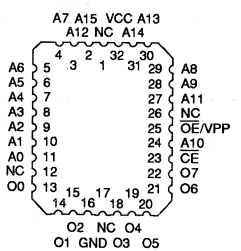
The AT27C512R chip is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 8. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 100ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

The AT27C512R meets or exceeds all specifications for the AT27C512. Atmel's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10µA in Standby.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /VPP	Output Enable
NC	No Connect





Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27C512R comes in a choice of industry standard JEDEC-approved packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Vcc	Outputs
Read	V_{IL}	V_{IL}	Ai	Vcc	DOUT
Output Disable	V_{IL}	V_{IH}	X(1)	Vcc	High Z
Standby	V_{IH}	X	X	Vcc	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	Vcc	DIN
PGM Verify	V_{IL}	V_{IL}	Ai	Vcc	DOUT
PGM Inhibit	V_{IH}	V_{PP}	X	Vcc	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	Vcc	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C512R				
		-10	-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V	Com.		100	µA
			Ind.,Mil.		200	µA
		I_{SB2} (TTL) $\overline{CE}$=2.0 to V_{CC}+1.0V	Com.		2	mA
			Ind.,Mil.		3	mA
I_{CC}	V_{CC} Active Current	f=5MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	Com.		20	mA
			Ind.,Mil.		25	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-2.5mA		3.5		V
		I_{OH}=-400µA		2.4		V

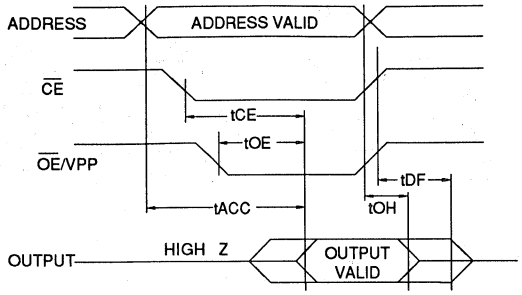
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation

				AT27C512R										
				-10		-12		-15		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE}$=$\overline{OE}/V_{PP}$ =VIL	Com.		100		120		150		200		250	ns
			Ind., Mil.				120		150		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$=V_{IL}			100		120		150		200		250	ns
t_{OE} (3,4)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$=V_{IL}			40		50		60		75		100	ns
t_{DF} (2,5)	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE}$=V_{IL}			30		45		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$=$\overline{OE}/V_{PP}$ =V_{IL}			0		0		0		0		0	ns

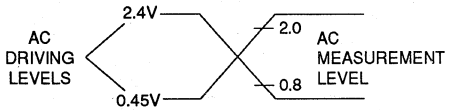
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



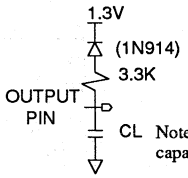
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ /V_{PP} or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$/V_{PP} may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ /V_{PP} may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



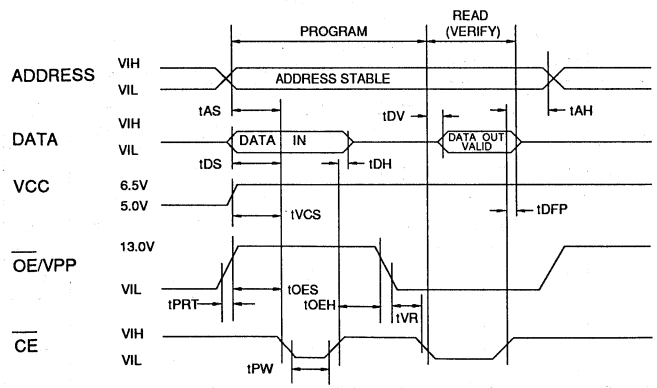
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

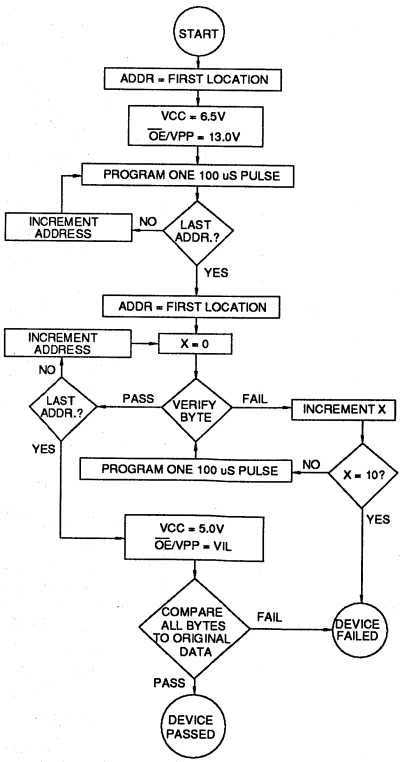
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C512R Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	20	0.1	AT27C512R-10DC AT27C512R-10JC AT27C512R-10KC AT27C512R-10LC AT27C512R-10PC AT27C512R-10RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
120	20	0.1	AT27C512R-12DC AT27C512R-12JC AT27C512R-12KC AT27C512R-12LC AT27C512R-12PC AT27C512R-12RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
120	25	0.2	AT27C512R-12DI AT27C512R-12JI AT27C512R-12KI AT27C512R-12LI AT27C512R-12PI AT27C512R-12RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-12DM AT27C512R-12KM AT27C512R-12LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-12DM/883 AT27C512R-12KM/883 AT27C512R-12LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	20	0.1	AT27C512R-15DC AT27C512R-15JC AT27C512R-15KC AT27C512R-15LC AT27C512R-15PC AT27C512R-15RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
150	25	0.2	AT27C512R-15DI AT27C512R-15JI AT27C512R-15KI AT27C512R-15LI AT27C512R-15PI AT27C512R-15RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-15DM AT27C512R-15KM AT27C512R-15LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-15DM/883 AT27C512R-15KM/883 AT27C512R-15LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C512R-20DC AT27C512R-20JC AT27C512R-20KC AT27C512R-20LC AT27C512R-20PC AT27C512R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	25	0.2	AT27C512R-20DI AT27C512R-20JI AT27C512R-20KI AT27C512R-20LI AT27C512R-20PI AT27C512R-20RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-20DM AT27C512R-20KM AT27C512R-20LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-20DM/883 AT27C512R-20KM/883 AT27C512R-20LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C512R-25DC AT27C512R-25JC AT27C512R-25KC AT27C512R-25LC AT27C512R-25PC AT27C512R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	25	0.2	AT27C512R-25DI AT27C512R-25JI AT27C512R-25KI AT27C512R-25LI AT27C512R-25PI AT27C512R-25RI	28DW6 32J 32KW 32LW 28P6 28R	Industrial (-40°C to 85°C)
			AT27C512R-25DM AT27C512R-25KM AT27C512R-25LM	28DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C512R-25DM/883 AT27C512R-25KM/883 AT27C512R-25LM/883	28DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	25	0.2	5962-87648 04 XX 5962-87648 04 YX 5962-87648 04 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	25	0.2	5962-87648 01 XX 5962-87648 01 YX 5962-87648 01 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.2	5962-87648 02 XX 5962-87648 02 YX 5962-87648 02 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.2	5962-87648 03 XX 5962-87648 03 YX 5962-87648 03 ZX	28DW6 32LW 32KW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

Features

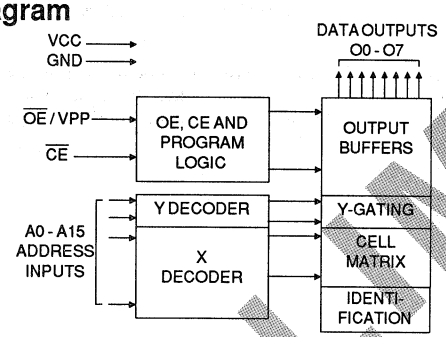
- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C512R
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26mW max. Active at 3.3 MHz for V_{CC} = 3.3 VDC
  - 110mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 300ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

512K (64K x 8) Low Voltage UV Erasable CMOS EPROM

4

Preliminary

Block Diagram



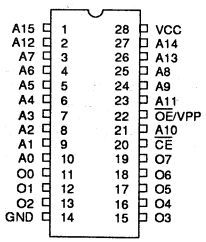
Description

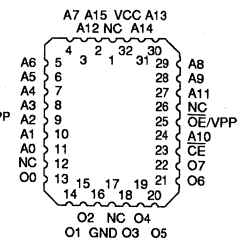
The AT27LV512R chip is a low power, low voltage 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18mW at 3.3 MHz and V_{CC} at 3.3 VDC, the AT27LV512R will draw less than one fifth the power of a standard 5 volt EPROM. Standby mode supply current is typically less than 20µA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ /V_{PP}	Output Enable
NC	No Connect





Note: LCC Package Pins 1 and 17 are DON'T CONNECT.

Description (Continued)

The AT27LV512R comes in a choice of industry standard JEDEC-approved ceramic packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC), and 32-pad leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27LV512R operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV512R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV512R programs identically as an AT27C512R.

Erasure Characteristics

The entire memory array of the AT27LV512R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is 6.5V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	V_{CC} (2)	D_{IN}
PGM Verify (2)	V_{IL}	V_{IL}	Ai	V_{CC} (2)	D_{OUT}
PGM Inhibit (2)	V_{IH}	V_{PP}	X	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC} (2)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV512R -30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
VCC Power Supply		3.0V to 5.5V

D.C. and Operating Characteristics for Read Operation

(VCC = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC}+0.1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0V			100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5V	Com.		20	mA
			Ind.		25	mA
		I_{CC2} f = 3.33MHz, I_{OUT} = 0mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3V	Com.		8	mA
			Ind.		10	mA
V_{IL}	Input Low Voltage	V_{IL1} 4.5 ≤ V_{CC} ≤ 5.5V		-0.6	0.8	V
		V_{IL2} 3.0 ≤ V_{CC} < 4.5V		-0.6	0.6	V
V_{IH}	Input High Voltage			2.0	6.5	V
V_{OL}	Output Low Voltage	V_{OL1} I_{OL} = 2.1mA, V_{CC} = 4.5V			.45	V
		V_{OL2} I_{OL} = 1.0mA, V_{CC} = 3.0V			0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -400µA		2.4		V

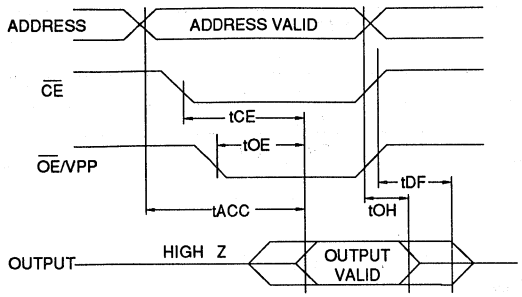
Notes: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

A.C. Characteristics for Read Operation (V_{CC} = 3.0V to 5.5V)

Symbol	Parameter	Condition		AT27LV512R -30 Min	AT27LV512R -30 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}/V_{PP}$=V_{IL}	Com.		270	ns
			Ind.		270	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP}$=V_{IL}			300	ns
t_{OE} (2,3)	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE}$=V_{IL}			150	ns
t_{DF} (4,5)	$\overline{OE}/V_{PP}$ High to Output Float	$\overline{CE}$=V_{IL}			100	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first	$\overline{CE}$=$\overline{OE}/V_{PP}$ =V_{IL}			0	ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

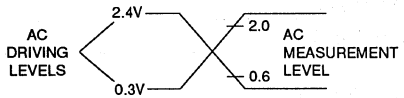
A.C. Waveforms for Read Operation [1]



Notes:
1. 3V timing measurement references are 0.6V and 2.0V. Input AC driving levels are 0.3V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

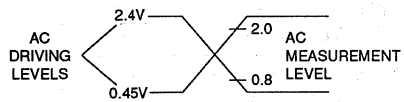
Input Test Waveforms and Measurement Levels

(VCC = 3.0V)



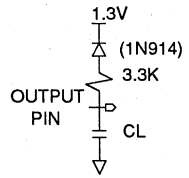
t_R, t_F < 20ns (10% to 90%)

(VCC = 5.5V)



t_R, t_F < 20ns (10% to 90%)

Output Test Load



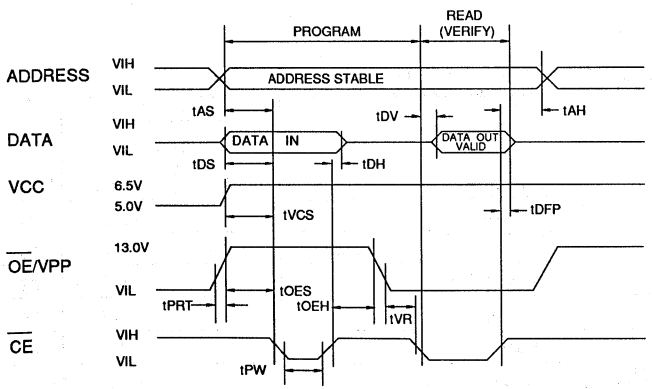
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max-	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for 5V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Current	$\overline{CE}=V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{OE}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{DV}	Data Valid from $\overline{CE}$	(Note 2)		1	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

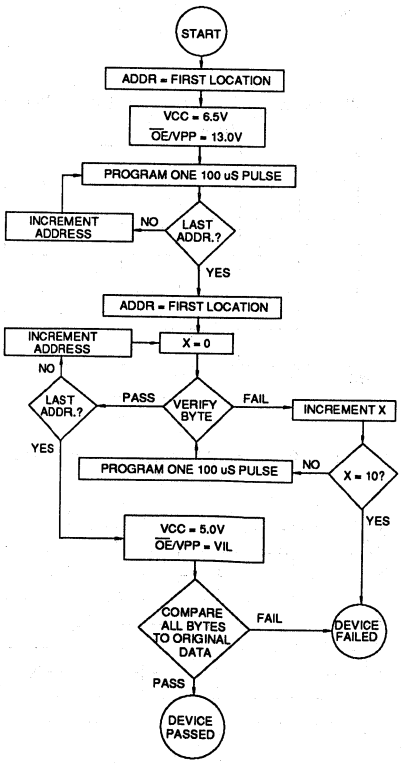
Atmel's 27LV512R Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

Note: 1. The AT27LV512R has the same Product Identification Code as the AT27C512R. Both are programming compatible.

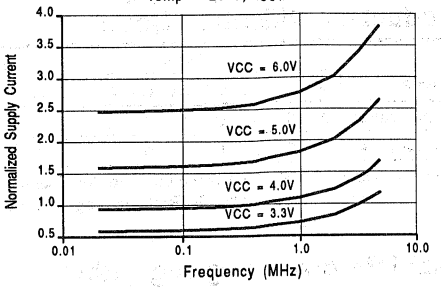
Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



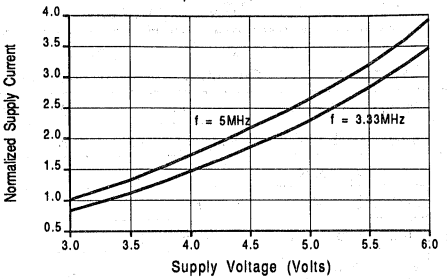
NORMALIZED SUPPLY CURRENT vs. FREQUENCY

Temp = 25°C, IOUT = 0

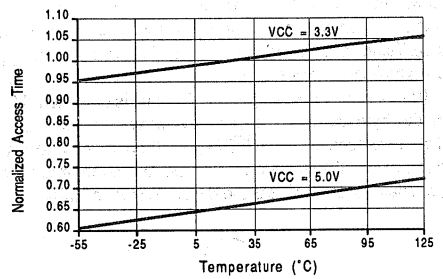


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

Temp = 25°C, IOUT = 0

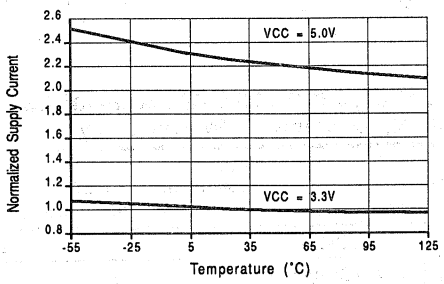


NORMALIZED ACCESS TIME vs. TEMPERATURE



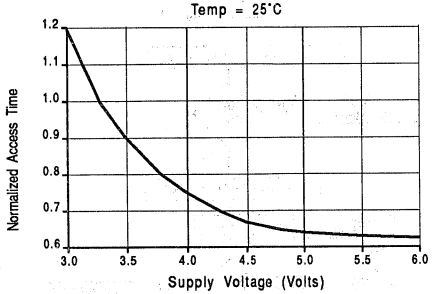
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

Frequency = 3.33MHz, IOUT = 0



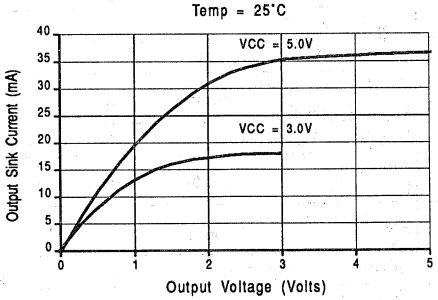
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

Temp = 25°C



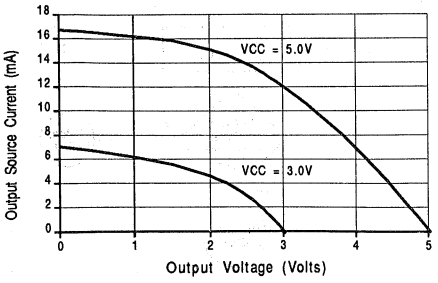
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active (3.3)	Standby			
270	8	0.1	AT27LV512R-30DC AT27LV512R-30JC AT27LV512R-30LC AT27LV512R-30PC AT27LV512R-30RC	28DW6 32J 32LW 28P6 28R	Commercial (0°C to 70°C)
270	10	0.1	AT27LV512R-30DI AT27LV512R-30LI	28DW6 32LW	Industrial (-40°C to 85°C)

4

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

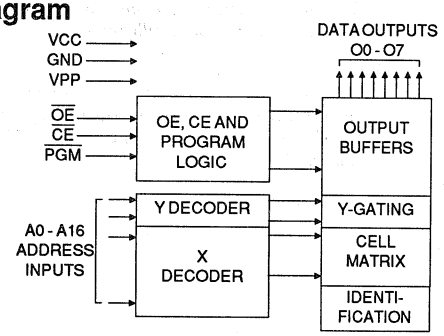
Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 25 mA max. Active at 5 MHz (AT27C010L)
  - 40 mA max. Active at 5 MHz (AT27C010)
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 32-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad LCC
  - 32-Lead JLCC and OTP PLCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

1 Megabit (128K x 8) UV Erasable CMOS EPROM

4

Block Diagram



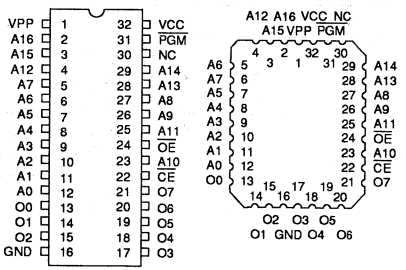
Description

The AT27C010/L chip family is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 128K x 8 bits. They require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

Two power versions are offered. In read mode, the AT27C010 typically consumes 25mA while the AT27C010L takes only 8mA. Standby mode supply current for both parts is typically less than 20µA.

Pin Configurations

Pin Name	Function
A0-A16	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect



Description (Continued)

The AT27C010/L come in a choice of industry standard JEDEC-approved packages including; 32-pin DIP in ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC) or OTP plastic (PLCC) J-leaded chip carrier. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 128K byte storage capability, the AT27C010/L allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C010/L have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C010/L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A16=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C010 / AT27C010L				
		-12	-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V				5	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V				100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V				1	mA
I_{CC}	V_{CC} Active Current	f=5MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	AT27C010L	Com.		25	mA
				Ind.,Mil.		30	mA
			AT27C010	Com.		40	mA
				Ind.,Mil.		50	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA				.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA			V_{CC}-0.3		V
		I_{OH}=-2.5mA			3.5		V
		I_{OH}=-400µA			2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

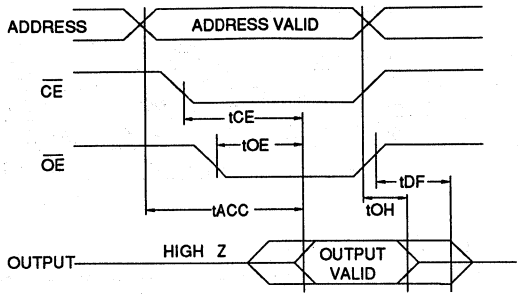
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C010 / AT27C010L									
				-12		-15		-17		-20		-25	
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		120		150		170		200		250	ns
			Ind.,Mil.		120		150		170		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			120		150		170		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			35		40		65		70		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			50		60		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0		0	ns

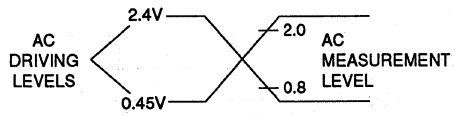
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



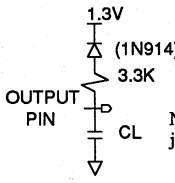
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



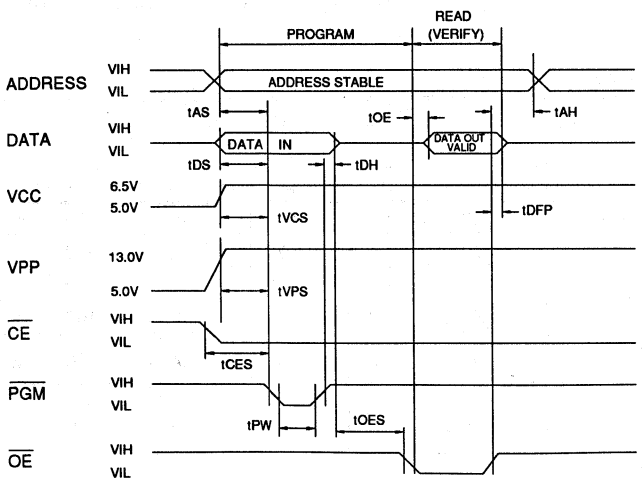
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C010/L a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			40	mA
I_{PP2}	Vpp Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	Vpp Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

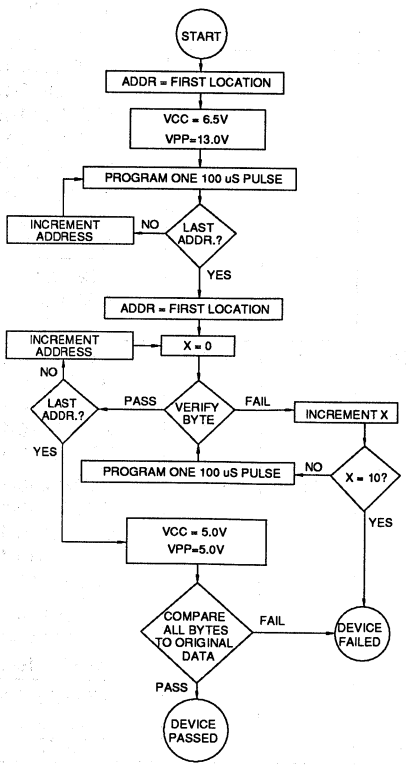
1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C010/L Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. Vcc is raised to 6.5V and Vpp is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0V and Vcc to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT27C010-12DC AT27C010-12JC AT27C010-12KC AT27C010-12LC AT27C010-12PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
120	50	0.1	AT27C010-12DI AT27C010-12JI AT27C010-12KI AT27C010-12LI AT27C010-12PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-12DM AT27C010-12KM AT27C010-12LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-12DM/883 AT27C010-12KM/883 AT27C010-12LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	40	0.1	AT27C010-15DC AT27C010-15JC AT27C010-15KC AT27C010-15LC AT27C010-15PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
150	50	0.1	AT27C010-15DI AT27C010-15JI AT27C010-15KI AT27C010-15LI AT27C010-15PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-15DM AT27C010-15KM AT27C010-15LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-15DM/883 AT27C010-15KM/883 AT27C010-15LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	40	0.1	AT27C010-17DC AT27C010-17JC AT27C010-17KC AT27C010-17LC AT27C010-17PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
170	50	0.1	AT27C010-17DI AT27C010-17JI AT27C010-17KI AT27C010-17LI AT27C010-17PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-17DM AT27C010-17KM AT27C010-17LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-17DM/883 AT27C010-17KM/883 AT27C010-17LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.1	AT27C010-20DC AT27C010-20JC AT27C010-20KC AT27C010-20LC AT27C010-20PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
200	50	0.1	AT27C010-20DI AT27C010-20JI AT27C010-20KI AT27C010-20LI AT27C010-20PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-20DM AT27C010-20KM AT27C010-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-20DM/883 AT27C010-20KM/883 AT27C010-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	40	0.1	AT27C010-25DC AT27C010-25JC AT27C010-25KC AT27C010-25LC AT27C010-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
250	50	0.1	AT27C010-25DI AT27C010-25JI AT27C010-25KI AT27C010-25LI AT27C010-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010-25DM AT27C010-25KM AT27C010-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010-25DM/883 AT27C010-25KM/883 AT27C010-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	50	0.1	5962-89614 04 M XX 5962-89614 04 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	5962-89614 03 M XX 5962-89614 03 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	50	0.1	5962-89614 02 M XX 5962-89614 02 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	50	0.1	5962-89614 01 M XX 5962-89614 01 M YX	32DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.1	AT27C010L-12DC AT27C010L-12JC AT27C010L-12KC AT27C010L-12LC AT27C010L-12PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
120	30	0.1	AT27C010L-12DI AT27C010L-12JI AT27C010L-12KI AT27C010L-12LI AT27C010L-12PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-12DM AT27C010L-12KM AT27C010L-12LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-12DM/883 AT27C010L-12KM/883 AT27C010L-12LM/883	32DW6 32KW 32LW	Military Class B, Fully Compliant (-55°C to 125°C)
150	25	0.1	AT27C010L-15DC AT27C010L-15JC AT27C010L-15LC AT27C010L-15KC AT27C010L-15PC	32DW6 32J 32LW 32KW 32P6	Commercial (0°C to 70°C)
150	30	0.1	AT27C010L-15DI AT27C010L-15JI AT27C010L-15KI AT27C010L-15LI AT27C010L-15PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-15DM AT27C010L-15KM AT27C010L-15LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-15DM/883 AT27C010L-15KM/883 AT27C010L-15LM/883	32DW6 32KW 32LW	Military Class B, Fully Compliant (-55°C to 125)
170	25	0.1	AT27C010L-17DC AT27C010L-17JC AT27C010L-17KC AT27C010L-17LC AT27C010L-17PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
170	30	0.1	AT27C010L-17DI AT27C010L-17JI AT27C010L-17KI AT27C010L-17LI AT27C010L-17PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-17DM AT27C010L-17KM AT27C010L-17LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-17DM/883 AT27C010L-17KM/883 AT27C010L-17LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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Ordering Information

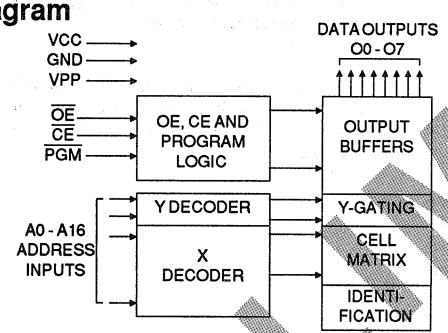
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	25	0.1	AT27C010L-20DC AT27C010L-20JC AT27C010L-20KC AT27C010L-20LC AT27C010L-20PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
200	30	0.1	AT27C010L-20DI AT27C010L-20JI AT27C010L-20KI AT27C010L-20LI AT27C010L-20PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-20DM AT27C010L-20KM AT27C010L-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-20DM/883 AT27C010L-20KM/883 AT27C010L-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.1	AT27C010L-25DC AT27C010L-25JC AT27C010L-25KC AT27C010L-25LC AT27C010L-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
250	30	0.1	AT27C010L-25DI AT27C010L-25JI AT27C010L-25KI AT27C010L-25LI AT27C010L-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27C010L-25DM AT27C010L-25KM AT27C010L-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27C010L-25DM/883 AT27C010L-25KM/883 AT27C010L-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

- Very Low Power CMOS Operation
  - 100 µA max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 150ns
- Compatible with JEDEC standard AT27C010
- Wide Selection of JEDEC Standard Packages Including OTP
  - 32-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad LCC
  - 32-Lead JLCC and OTP PLCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with AT27C010/L

Block Diagram



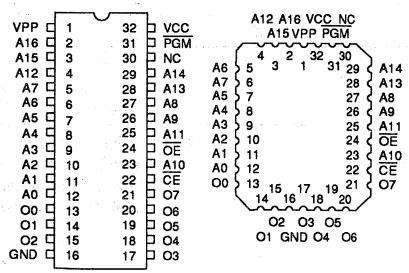
Description

The AT27CL010 chip is a very low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 128K x 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 150ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

In read mode, the AT27CL010 typically consumes 6mA. Standby mode supply current is typically less than 5µA.

Pin Configurations

Pin Name	Function
A0-A16	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect



1 Megabit (128K x 8) Low Power UV Erasable CMOS EPROM

Preliminary

4

Description (Continued)

The AT27CL010 comes in a choice of industry standard JEDEC-approved packages including; 32-pin DIP in ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead ceramic (JLCC) or OTP plastic (PLCC) J-leaded chip carrier. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 128K byte storage capability, the AT27CL010 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27CL010 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27CL010 programs identically to an AT27C010/L.

Erasure Characteristics

The entire memory array of the AT27CL010 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A16=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27CL010			
		-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

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D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V		5	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V		10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V		10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V		100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V		1	mA
I_{CC}	V_{CC} Active Current	f=5MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}		20	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA	V_{CC}-0.3		V
		I_{OH}=-2.5mA	3.5		V
		I_{OH}=-400µA	2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

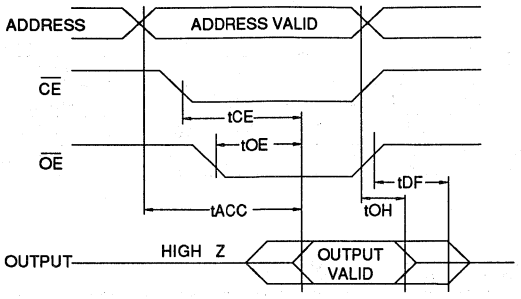
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27CL010								
				-15		-17		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		150		170		200		250	ns
			Ind.,Mil.				170		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			150		170		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			40		65		75		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			40		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0	ns

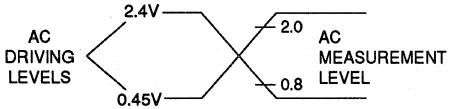
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



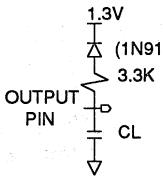
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



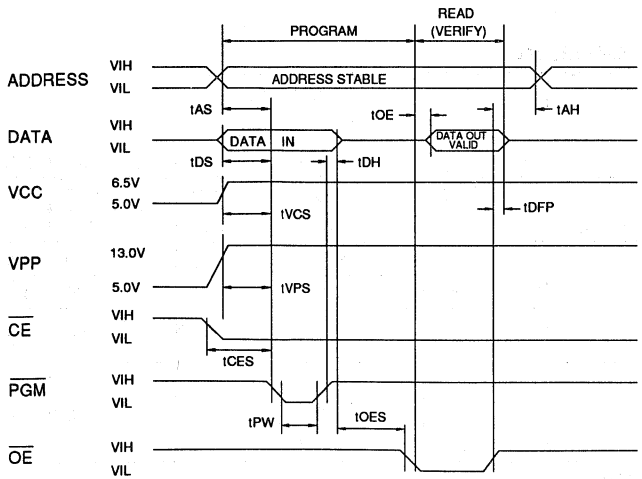
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27CL010 a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

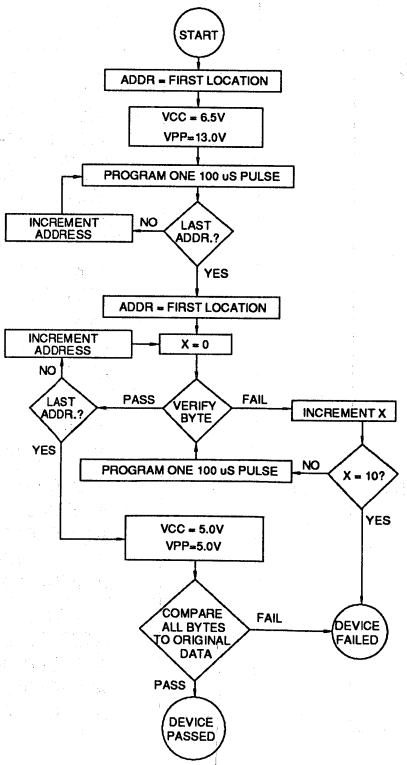
Atmel's 27CL010 Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	O5

Note: 1. The AT27CL010 has the same Product Identification Code as the AT27C010/L. Both are programming compatible.

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	20	0.1	AT27CL010-15DC AT27CL010-15JC AT27CL010-15KC AT27CL010-15LC AT27CL010-15PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
170	20	0.1	AT27CL010-17DC AT27CL010-17JC AT27CL010-17KC AT27CL010-17LC AT27CL010-17PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
			AT27CL010-17DI AT27CL010-17JI AT27CL010-17KI AT27CL010-17LI AT27CL010-17PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27CL010-17DM AT27CL010-17KM AT27CL010-17LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27CL010-17DM/883 AT27CL010-17KM/883 AT27CL010-17LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27CL010-20DC AT27CL010-20JC AT27CL010-20KC AT27CL010-20LC AT27CL010-20PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
			AT27CL010-20DI AT27CL010-20JI AT27CL010-20KI AT27CL010-20LI AT27CL010-20PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)
			AT27CL010-20DM AT27CL010-20KM AT27CL010-20LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27CL010-20DM/883 AT27CL010-20KM/883 AT27CL010-20LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27CL010-25DC AT27CL010-25JC AT27CL010-25KC AT27CL010-25LC AT27CL010-25PC	32DW6 32J 32KW 32LW 32P6	Commercial (0°C to 70°C)
			AT27CL010-25DI AT27CL010-25JI AT27CL010-25KI AT27CL010-25LI AT27CL010-25PI	32DW6 32J 32KW 32LW 32P6	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	20	0.1	AT27CL010-25DM AT27CL010-25KM AT27CL010-25LM	32DW6 32KW 32LW	Military (-55°C to 125°C)
			AT27CL010-25DM/883 AT27CL010-25KM/883 AT27CL010-25LM/883	32DW6 32KW 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

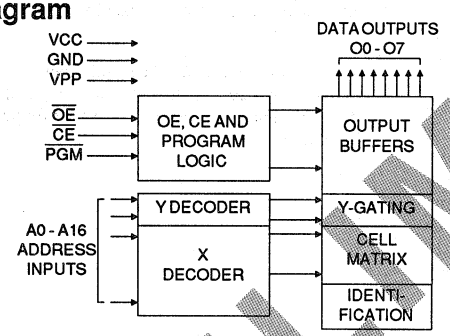
- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C010
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26mW max. Active at 3.3 MHz for V_{CC} = 3.3 VDC
  - 138mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 300ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 32-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

1 Megabit (128K x 8) Low Voltage UV Erasable CMOS EPROM

4

Preliminary

Block Diagram



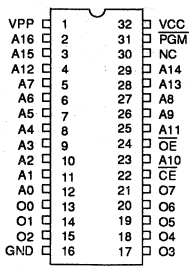
Description

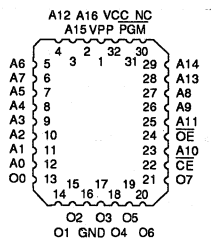
The AT27LV010 chip is a low power, low voltage 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 128K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18mW at 3.3 MHz and V_{CC} at 3.3 VDC, the AT27LV010 will draw less than one fifth the power of a standard 5 volt EPROM. Standby mode supply current is typically less than 20µA.

Pin Configurations

Pin Name	Function
A0-A16	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect





Description (Continued)

The AT27LV010 comes in a choice of industry standard JEDEC-approved ceramic packages including; 32-pin DIP in ceramic or one time programmable (OTP) plastic, 32-pad ceramic leadless chip carrier (LCC), and 32-lead OTP plastic J-Leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

The AT27LV010 operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV010 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV010 programs identically as an AT27C010.

Erasure Characteristics

The entire memory array of the AT27LV010 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is 6.5V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC} (2)	D_{IN}
PGM Verify(2)	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC} (2)	D_{OUT}
PGM Inhibit(2)	V_{IH}	X	X	X	V_{PP}	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A16=V_{IL}	X	V_{CC} (2)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV010 -30
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
VCC Power Supply		3.0V to 5.5V

D.C. and Operating Characteristics for Read Operation

(VCC = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC}+1V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC}+0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}-0.7V to V_{CC}+0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0V			100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V			1	mA
I_{CC}	V_{CC} Active Current	I_{CC1} f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5V	Com.		25	mA
			Ind.		30	mA
		I_{CC2} f = 3.33MHz, I_{OUT} = 0mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3V	Com.		8	mA
			Ind.		10	mA
V_{IL}	Input Low Voltage	V_{IL1} 4.5 ≤ V_{CC} ≤ 5.5V		-0.6	0.8	V
		V_{IL2} 3.0 ≤ V_{CC} < 4.5V		-0.6	0.6	V
V_{IH}	Input High Voltage			2.0	6.5	V
V_{OL}	Output Low Voltage	V_{OL1} I_{OL} = 2.1mA, V_{CC} = 4.5V			.45	V
		V_{OL2} I_{OL} = 1.0mA, V_{CC} = 3.0V			0.3	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -400µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

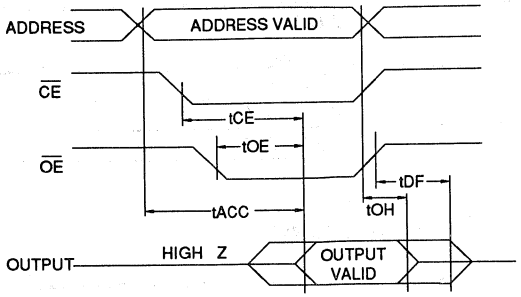
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation (VCC = 3.0V to 5.5V)

Symbol	Parameter	Condition		AT27LV010 -30 Min	AT27LV010 -30 Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}	Com.		270	ns
			Ind.		270	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			300	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			150	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			100	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0	ns

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

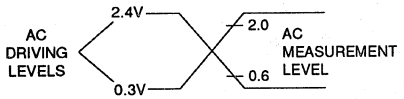
A.C. Waveforms for Read Operation [1]



Notes:
1. 3V timing measurement references are 0.6V and 2.0V. Input AC driving levels are 0.3V and 2.4V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

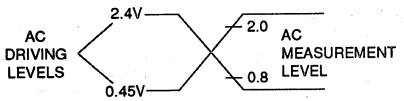
Input Test Waveforms and Measurement Levels

(VCC = 3.0V)



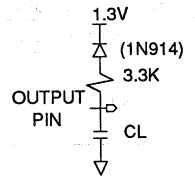
t_R, t_F < 20ns (10% to 90%)

(VCC = 5.5V)



t_R, t_F < 20ns (10% to 90%)

Output Test Load



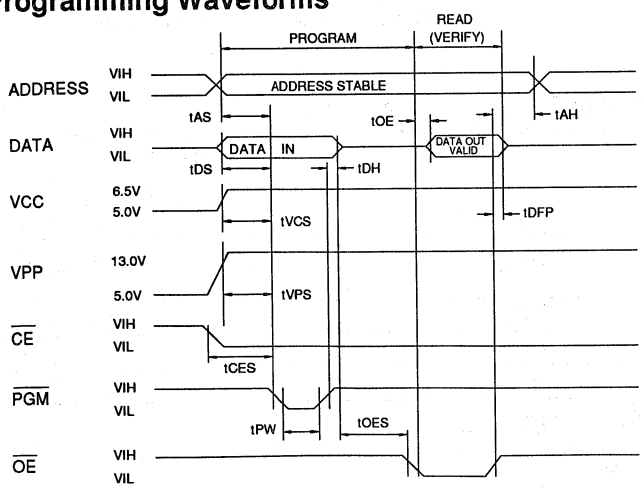
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for 5V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV010 a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

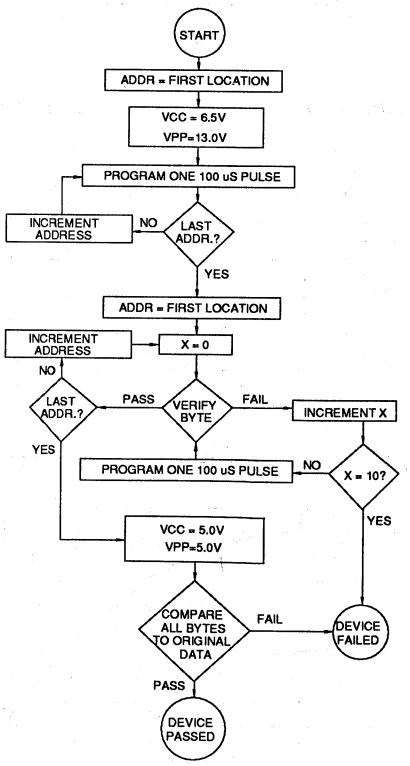
Atmel's 27LV010 Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	0	1	0	1	05

Note: 1. The AT27LV010 has the same Product Identification Code as the AT27C010/L. Both are programming compatible.

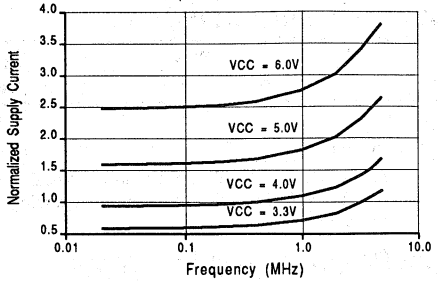
Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification/ reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



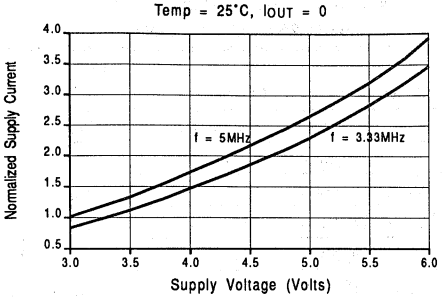
NORMALIZED SUPPLY CURRENT vs. FREQUENCY

Temp = 25°C, I_{OUT} = 0

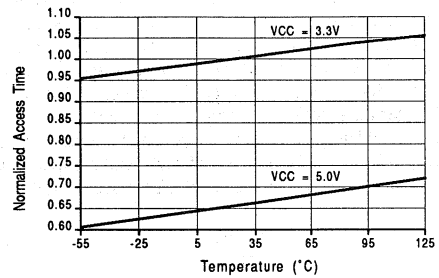


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

Temp = 25°C, I_{OUT} = 0

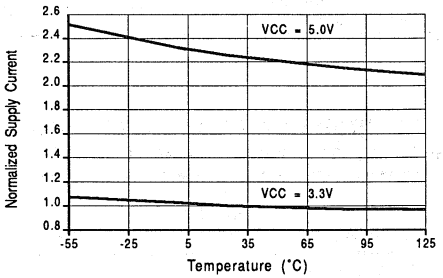


NORMALIZED ACCESS TIME vs. TEMPERATURE



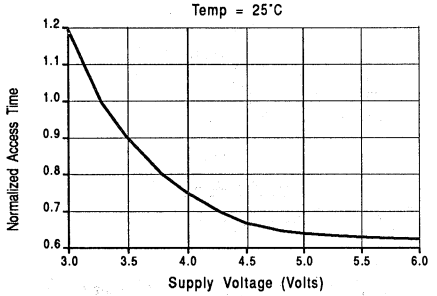
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

Frequency = 3.33MHz, I_{OUT} = 0



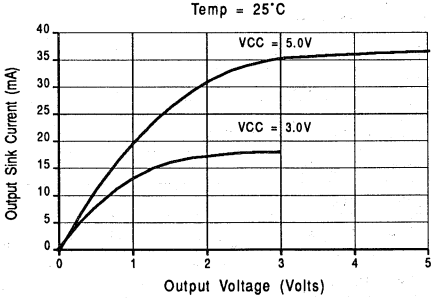
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

Temp = 25°C



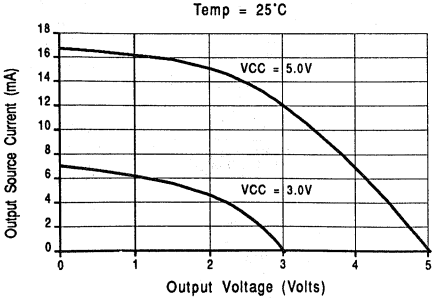
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active (3.3)	Standby			
270	8	0.1	AT27LV010-30DC AT27LV010-30JC AT27LV010-30LC AT27LV010-30PC	32DW6 32J 32LW 32P6	Commercial (0°C to 70°C)
270	10	0.1	AT27LV010-30DI AT27LV010-30LI	32DW6 32LW	Industrial (-40°C to 85°C)

4

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

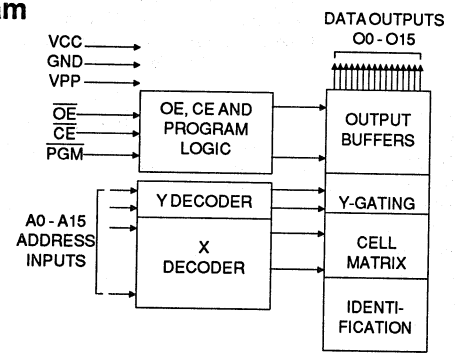
Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 30 mA max. Active at 5 MHz (AT27C1024L)
  - 50 mA max. Active at 5 MHz (AT27C1024)
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 40-Lead 600 mil Cerdip and OTP Plastic DIP
  - 44-Pad LCC and OTP PLCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Commercial and Industrial Temperature Ranges

1 Megabit (64K x 16) UV Erasable CMOS EPROM

4

Block Diagram



Description

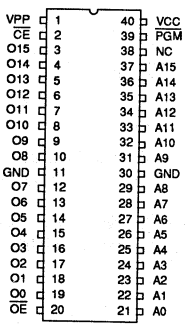
The AT27C1024/L chip family is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 16. They require only one 5V power supply in normal read mode operation. Any word can be accessed in less than 120ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16 and 32 bit microprocessor systems.

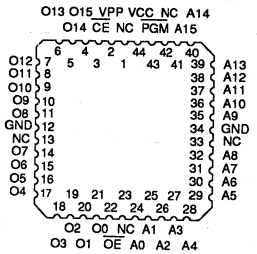
Two power versions are offered. In read mode, the AT27C1024 typically consumes 30mA while the AT27C1024L takes only 15mA. Standby mode supply current for both parts is typically less than 20µA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.





Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

Description (Continued)

The AT27C1024/L come in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K word storage capability, the AT27C1024/L allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C1024/L have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C1024/L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C1024 / AT27C1024L				
		-12	-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V				5	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V				100	µA
		I_{SB2} (TTL) $\overline{CE}$=2.0 to V_{CC}+1.0V				1	mA
I_{CC}	V_{CC} Active Current	f=5MHz, I_{OUT}=0mA, $\overline{CE}$=V_{IL}	AT27C1024L	Com.		30	mA
				Ind.,Mil.		40	mA
			AT27C1024	Com.		50	mA
				Ind.,Mil.		60	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA				.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA			V_{CC}-0.3		V
		I_{OH}=-2.5mA			3.5		V
		I_{OH}=-400µA			2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

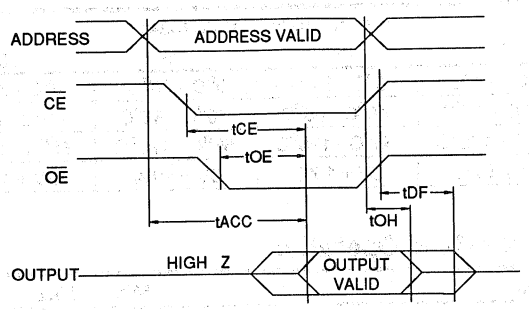
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C1024 / AT27C1024L										
				-12		-15		-17		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}	Com.		120		150		170		200		250	ns
			Ind.,Mil.						170		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			120		150		170		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			60		65		65		75		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			30		40		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$=V_{IL}			0		0		0		0		0	ns

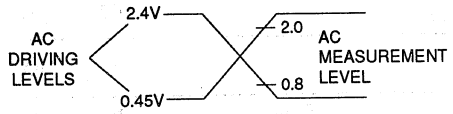
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



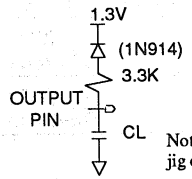
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



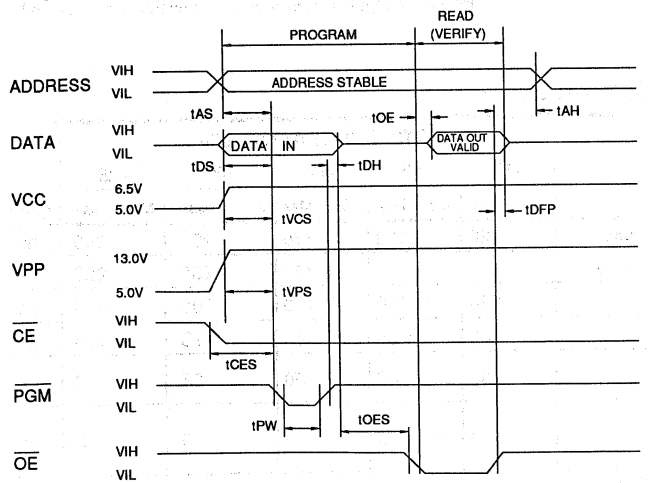
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C1024/L a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			50	mA
I_{PP2}	Vpp Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	Vpp Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

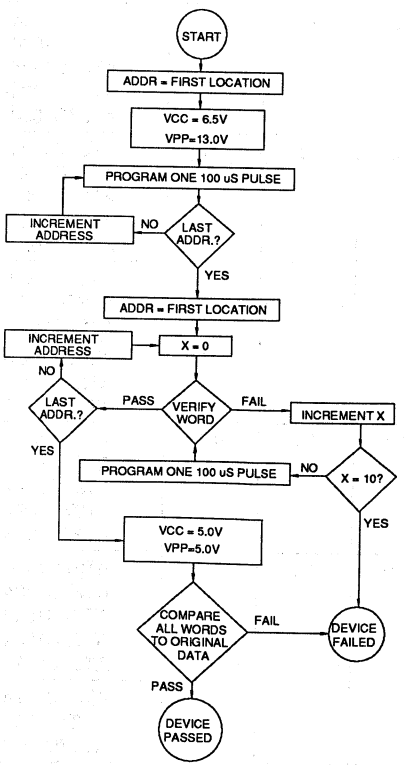
1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C1024/L Integrated Product Identification Code:

Codes	Pins A0	015-08 O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. Vcc is raised to 6.5V and Vpp is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0V and Vcc to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	50	0.1	AT27C1024-12DC AT27C1024-12KC AT27C1024-12LC	40DW6 44KW 44LW	Commercial (0°C to 70°C)
150	50	0.1	AT27C1024-15DC AT27C1024-15JC AT27C1024-15KC AT27C1024-15LC AT27C1024-15PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
150	60	0.1	AT27C1024-15DI AT27C1024-15JI AT27C1024-15KI AT27C1024-15LI AT27C1024-15PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024-15DM AT27C1024-15KM AT27C1024-15LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-15DM/883 AT27C1024-15KM/883 AT27C1024-15LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	50	0.1	AT27C1024-17DC AT27C1024-17JC AT27C1024-17KC AT27C1024-17LC AT27C1024-17PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
170	60	0.1	AT27C1024-17DI AT27C1024-17JI AT27C1024-17KI AT27C1024-17LI AT27C1024-17PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024-17DM AT27C1024-17KM AT27C1024-17LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-17DM/883 AT27C1024-17KM/883 AT27C1024-17LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.1	AT27C1024-20DC AT27C1024-20JC AT27C1024-20KC AT27C1024-20LC AT27C1024-20PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
200	60	0.1	AT27C1024-20DI AT27C1024-20JI AT27C1024-20KI AT27C1024-20LI AT27C1024-20PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024-20DM AT27C1024-20KM AT27C1024-20LM	40DW6 44KW 44LW	Military (-55°C to 125°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	60	0.1	AT27C1024-20DM/883 AT27C1024-20KM/883 AT27C1024-20LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	50	0.1	AT27C1024-25DC AT27C1024-25JC AT27C1024-25KC AT27C1024-25LC AT27C1024-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
250	60	0.1	AT27C1024-25DI AT27C1024-25JI AT27C1024-25KI AT27C1024-25LI AT27C1024-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024-25DM AT27C1024-25KM AT27C1024-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-25DM/883 AT27C1024-25KM/883 AT27C1024-25LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	60	0.1	5962-86805 04 QX 5962-86805 04 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	60	0.1	5962-86805 03 QX 5962-86805 03 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	60	0.1	5962-86805 02 QX 5962-86805 02 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	60	0.1	5962-86805 01 QX 5962-86805 01 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	30	0.1	AT27C1024L-12DC AT27C1024L-12KC AT27C1024L-12LC	40DW6 44KW 44LW	Commercial (0°C to 70°C)
150	30	0.1	AT27C1024L-15DC AT27C1024L-15JC AT27C1024L-15KC AT27C1024L-15LC AT27C1024L-15PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
150	40	0.1	AT27C1024L-15DI AT27C1024L-15JI AT27C1024L-15KI AT27C1024L-15LI AT27C1024L-15PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024L-15DM AT27C1024L-15KM AT27C1024L-15LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024L-15DM/883 AT27C1024L-15KM/883 AT27C1024L-15LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	30	0.1	AT27C1024L-17DC AT27C1024L-17JC AT27C1024L-17KC AT27C1024L-17LC AT27C1024L-17PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
170	40	0.1	AT27C1024L-17DI AT27C1024L-17JI AT27C1024L-17KI AT27C1024L-17LI AT27C1024L-17PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024L-17DM AT27C1024L-17KM AT27C1024L-17LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024L-17DM/883 AT27C1024L-17KM/883 AT27C1024L-17LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT27C1024L-20DC AT27C1024L-20JC AT27C1024L-20KC AT27C1024L-20LC AT27C1024L-20PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
200	40	0.1	AT27C1024L-20DI AT27C1024L-20JI AT27C1024L-20KI AT27C1024L-20LI AT27C1024L-20PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

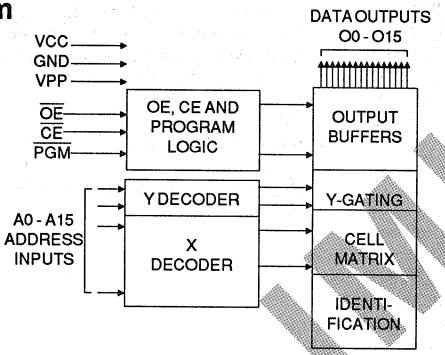
t_{ACC} (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.1	AT27C1024L-20DM AT27C1024L-20KM AT27C1024L-20LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024L-20DM/883 AT27C1024L-20KM/883 AT27C1024L-20LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT27C1024L-25DC AT27C1024L-25JC AT27C1024L-25KC AT27C1024L-25LC AT27C1024L-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
250	40	0.1	AT27C1024L-25DI AT27C1024L-25JI AT27C1024L-25KI AT27C1024L-25LI AT27C1024L-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024L-25DM AT27C1024L-25KM AT27C1024L-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024L-25DM/883 AT27C1024L-25KM/883 AT27C1024L-25LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

- Very Fast Read Access Time - 55ns
- Low Power CMOS Operation
  - 8 mA max. Standby
  - 80 mA max. Active at 10 MHz
- Wide Selection of JEDEC Standard Packages Including OTP
  - 40-Lead 600 mil Cerdip and OTP Plastic
  - 44-Pad LCC and OTP PLCC
- High Output Drive Capability
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges

Block Diagram



Description

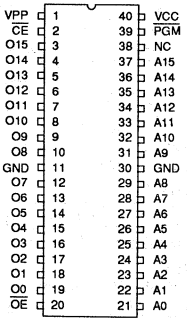
The AT27HC1024 chip is a high-speed, low-power 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 64K x 16 bits. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 55ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16 and 32 bit microprocessor and digital signal processor systems.

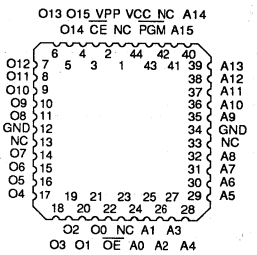
In read mode, the AT27HC1024 typically consumes 50mA, while in standby mode supply current is typically less than 1mA.

Pin Configurations

Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.





Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

1 Megabit (64K x 16) High Speed UV Erasable CMOS EPROM

Preliminary

Description (Continued)

The AT27HC1024 come in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K word storage capability, the AT27HC1024 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media. The AT27HC1024 has exceptional CMOS output device capability— source 4mA and sink 16mA per output.

Atmel's 27HC1024 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/word. Atmel's high speed single transistor floating poly EPROM cell technology also speeds up programming by eliminating the second program "Os" operation required for two transistor per cell designs. The AT27HC1024 uses the same widely accepted programming algorithm as the AT27C1024. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C1024/L is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC1024			
		-55	-70	-90	-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 5% 5V ± 10%	5V ± 10%	5V ± 10%

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D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			5	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V	Com.		8	mA
			Ind., Mil.		10	mA
		I_{SB2} (TTL) $\overline{CE}$=2.0 to V_{CC}+1.0V	Com.		17	mA
			Ind., Mil.		20	mA
I_{CC}	V_{CC} Active Current	f=10MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	Com.		80	mA
			Ind.,Mil.		90	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=16mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-4.0mA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

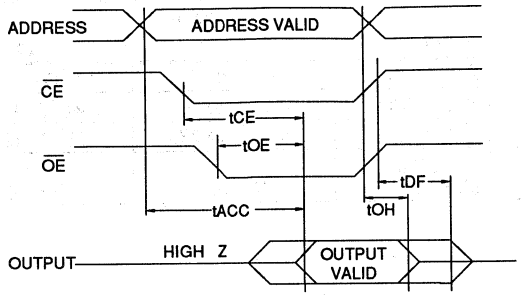
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27HC1024								
				-55		-70		-90		-12		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}	Com.		55		70		90		120	ns
			Ind.,Mil.				70		90		120	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			55		70		90		120	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			20		25		30		35	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			10		15		20		25	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$=V_{IL}			0		0		0		0	ns

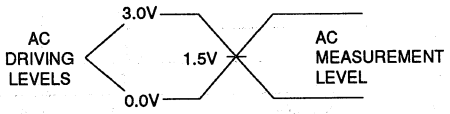
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



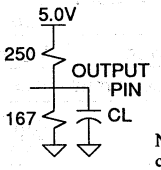
Notes:
1. Timing measurement references is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified. C_L=30pF, add 6ns for C_L=100pF.
2. t_{DF} is specified from $\overline{OE}$. t_{DF} is measured at V_{OH}-0.5V or V_{OL}+0.5V with C_L=5pF.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



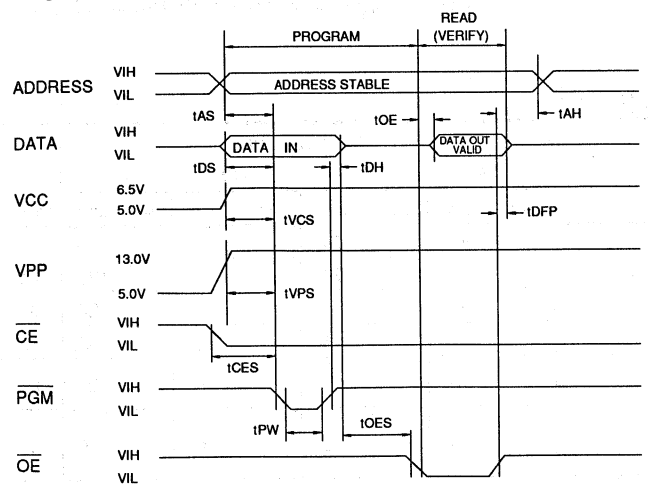
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27HC1024 a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=16mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-4mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			60	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		40	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels .....0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:

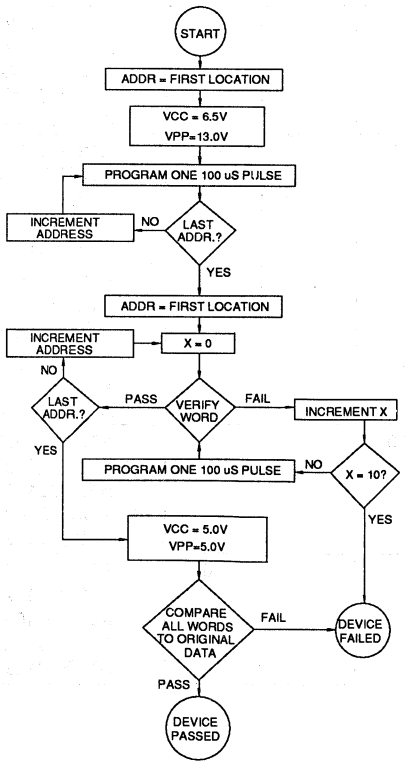
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27HC024 Integrated Product Identification Code:

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	0	1	1	0	0	0	0	1	0061

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
55	80	8	AT27HC1024-55DC AT27HC1024-55KC AT27HC1024-55LC	40DW6 44KW 44LW	Commercial (0°C to 70°C)
70	80	8	AT27HC1024-70DC AT27HC1024-70JC AT27HC1024-70KC AT27HC1024-70LC AT27HC1024-70PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
70	90	10	AT27HC1024-70DI AT27HC1024-70JI AT27HC1024-70KI AT27HC1024-70LI AT27HC1024-70PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27HC1024-70DM AT27HC1024-70KM AT27HC1024-70LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27HC1024-70DM/883 AT27HC1024-70KM/883 AT27HC1024-70LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	80	8	AT27HC1024-90DC AT27HC1024-90JC AT27HC1024-90KC AT27HC1024-90LC AT27HC1024-90PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
90	90	10	AT27HC1024-90DI AT27HC1024-90JI AT27HC1024-90KI AT27HC1024-90LI AT27HC1024-90PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27HC1024-90DM AT27HC1024-90KM AT27HC1024-90LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27HC1024-90DM/883 AT27HC1024-90KM/883 AT27HC1024-90LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	80	8	AT27HC1024-12DC AT27HC1024-12JC AT27HC1024-12KC AT27HC1024-12LC AT27HC1024-12PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
120	90	10	AT27HC1024-12DI AT27HC1024-12JI AT27HC1024-12KI AT27HC1024-12LI AT27HC1024-12PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	90	10	AT27HC1024-12DM AT27HC1024-12KM AT27HC1024-12LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27HC1024-12DM/883 AT27HC1024-12KM/883 AT27HC1024-12LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	90	10	5962-86805 08 QX 5962-86805 08 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	90	10	5962-86805 07 QX 5962-86805 07 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

4

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

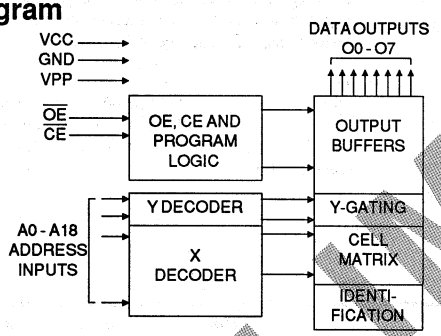
- Low Power CMOS Operation
  - 100 µA max. Standby
  - 25 mA max. Active at 5 MHz
- Fast Read Access Time - 120 ns
- JEDEC Standard Packages
  - 32-Lead 600 mil Cerdip and OTP Plastic DIP
- Surface Mount Packages
  - 44-Pin PLCC and LCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges

4 Megabit (512K x 8) UV Erasable CMOS EPROM

Preliminary

4

Block Diagram



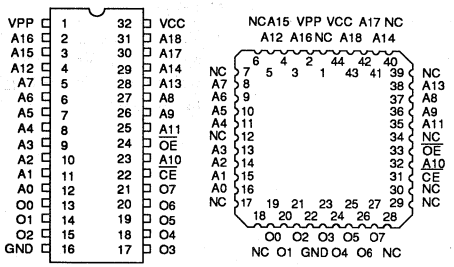
Description

The AT27C040 chip family is a low-power, high-performance 4,194,304 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 512K x 8 bits. The AT27C040 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's 1.0 micron scaled CMOS technology provides for significantly lower active power consumption than competing designs. Power consumption is typically 20 mA in active mode and less than 20 µA in standby mode.

Pin Configurations

Pin Name	Function
A0-A18	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable



Note: PLCC Package Pin 1 is a DON'T CONNECT.

Description (Continued)

The AT27C040 comes in a 44-pin PLCC, a 44-pad LCC, and two JEDEC-approved packages: a 32-pin ceramic and a one time programmable (OTP) plastic DIP. The device features two line control ($\overline{CE}$, $\overline{OE}$) which gives designers the flexibility to avoid bus contentions. With 512K byte of storage capability, the AT27C040 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C040 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of the AT27C040 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	X(1)	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	High Z
Fast Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	X	V_{IL}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A18=V_{IL}	X	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C040		
		-12	-15	-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			5	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V			100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V			1	mA
I_{CC}	V_{CC} Active Current	f=5MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	Com.		25	mA
			Ind.,Mil.		30	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-2.5mA		3.5		V
		I_{OH}=-400µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

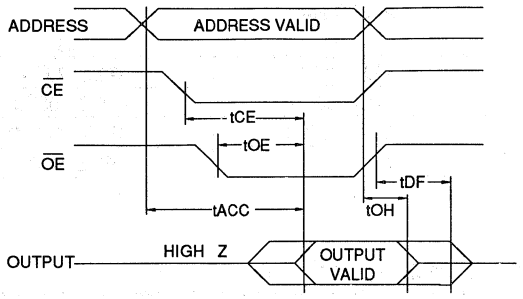
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C040						
				-12		-15		-20		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		120		150		200	ns
			Ind.,Mil.				150		200	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			120		150		200	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			35		40		70	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			35		40		55	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}		0		0		0		ns

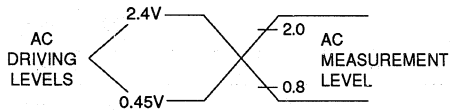
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



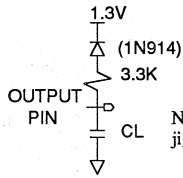
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



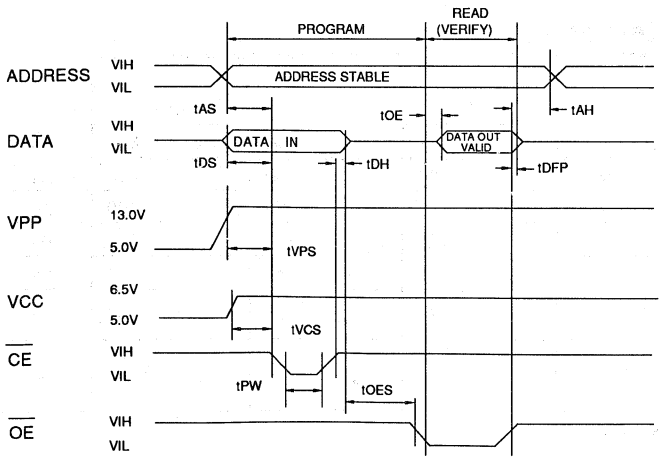
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C040 a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	Vcc Supply Current (Program and Verify)			40	mA
I_{PP2}	Vpp Supply Current	$\overline{CE}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	Vpp Setup Time		2		µs
t_{VCS}	Vcc Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

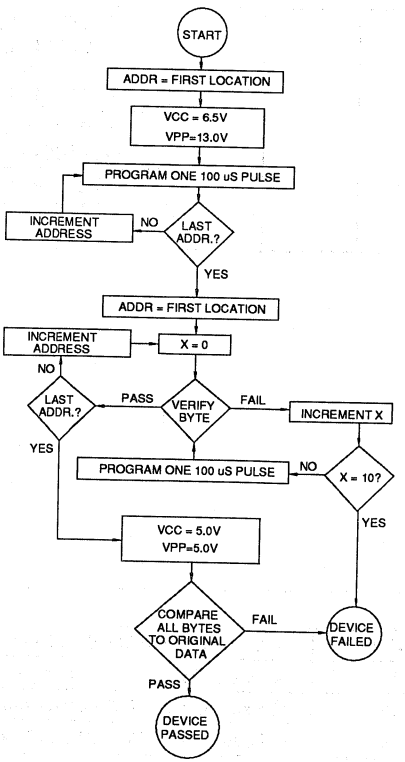
1. Vcc must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27C040 Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Rapid Programming Algorithm

A 100µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. Vcc is raised to 6.5V and Vpp is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. Vpp is then lowered to 5.0V and Vcc to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



5

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.1	AT27C040-12DC	32DW6	Commercial (0°C to 70°C)
150	25	0.1	AT27C040-15DC AT27C040-15JC AT27C040-15LC AT27C040-15PC	32DW6 44J 44LW 32P6	Commercial (0°C to 70°C)
150	30	0.1	AT27C040-15DI AT27C040-15JI AT27C040-15LI AT27C040-15PI	32DW6 44J 44LW 32P6	Industrial (-40°C to 85°C)
			AT27C040-15DM AT27C040-15LM	32DW6 44LW	Military (-55°C to 125°C)
			AT27C040-15DM/883 AT27C040-15LM/883	32DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.1	AT27C040-20DC AT27C040-20JC AT27C040-20LC AT27C040-20PC	32DW6 44J 44LW 32P6	Commercial (0°C to 70°C)
200	30	0.1	AT27C040-20DI AT27C040-20JI AT27C040-20LI AT27C040-20PI	32DW6 44J 44LW 32P6	Industrial (-40°C to 85°C)
			AT27C040-20DM AT27C040-20LM	32DW6 44LW	Military (-55°C to 125°C)
			AT27C040-20DM/883 AT27C040-20LM/883	32DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
32DW6	32 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
32P6	32 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Contents

Section 5

CMOS PROMs

5

Features

- Fast Access Time - 35ns
- Low Power Dissipation
  - 100 µA Standby Current (AT28HC191L)
  - 80 mA Active Current
- E^2PROM Technology - 100% Reprogrammable
- Direct Replacement for Bipolar PROMs
- Reprogrammable 1000 times
- Chip Clear
- JEDEC Approved Byte-Wide Pinout
  - Industry Standard 600 mil Wide Package
- CMOS and TTL Compatible Inputs and Outputs
- High Reliability High Speed CMOS Technology
- Full Military, Commercial, and Industrial Temperature Ranges

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

5

Description

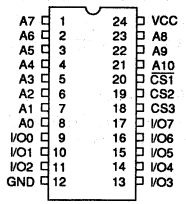
The AT28HC191/191L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC191 offers access times to 35ns while the AT28HC191L provides low standby current consumption of just 100µA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC191 and AT28HC191L are packaged in the industry standard 600 mil wide package.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC191L brings bipolar speeds to battery powered systems.

The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^2PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

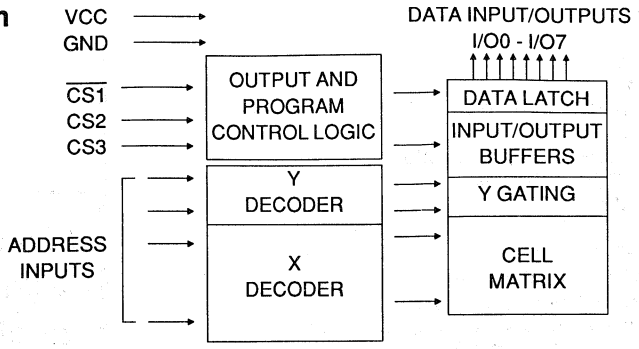
The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data

Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	D_{OUT}
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	D_{IN}
Verify	V_{IH}	V_{IH}	V_H	D_{OUT}
Chip Clear	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC191L consumes less than 550µW when deselected by raising $\overline{CS1}$ to V_{CC}-0.3V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC191.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to V_{IH}. The verify works exactly as a device read except that $\overline{CS1}$ is at 12 volts rather than V_{IL}.

MEMORY CELL: The AT28HC191 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning, and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5

D.C. and A.C. Operating Range

		AT28HC191-35	AT28HC191-45 AT28HC191L-45	AT28HC191-55 AT28HC191L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	—	-40°C - 85°C	-40°C - 85°C
	Mil.	—	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$=V_{IH} ADDR=0/V_{CC}	AT28HC191L		3	mA
			AT28HC191		60	mA
I_{CC}	V_{CC} Active Current	f=10MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=12mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4		V

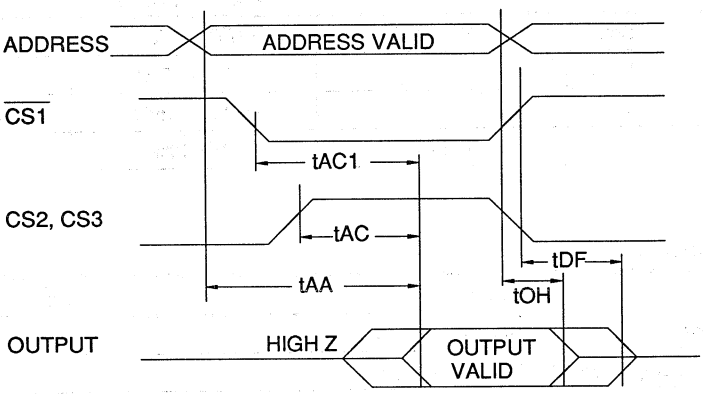
Pin Capacitance (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Characteristics for Read Operation [1]

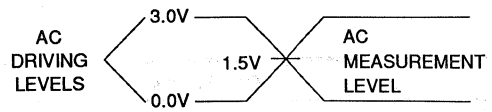
Symbol	Parameter	AT28HC191 -35 Min	AT28HC191 -35 Max	AT28HC191 -45 Min	AT28HC191 -45 Max	AT28HC191 -55 Min	AT28HC191 -55 Max	AT28HC191L -45 Min	AT28HC191L -45 Max	AT28HC191L -55 Min	AT28HC191L -55 Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



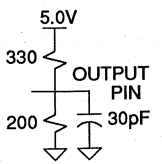
Notes:
1. CL=30pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns

Output Test Load

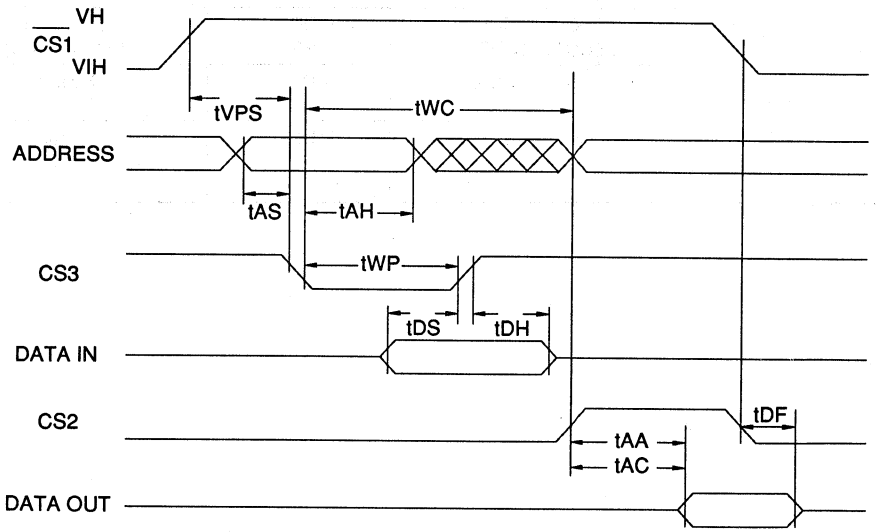


A.C. Write Characteristics

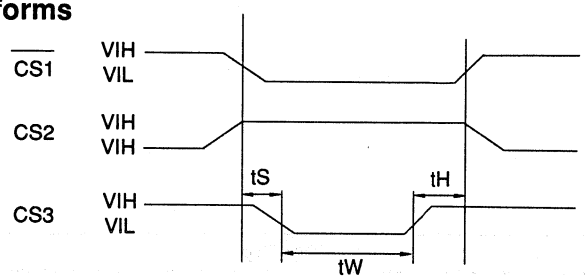
Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			µs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

5

A.C. Write Waveforms



Chip Erase Waveforms



$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12 \pm 0.5V$

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	AT28HC191-35DC AT28HC191-35PC	24D6 24P6	Commercial (0° to 70°C)
45	80	60	AT28HC191-45DC AT28HC191-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-45DI AT28HC191-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-45DM	24D6	Military (-55° to 125°C)
			AT28HC191-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC191-55DC AT28HC191-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191-55DI AT28HC191-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191-55DM	24D6	Military (-55° to 125°C)
			AT28HC191-55DM/883	24D6	Military Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC191L-45DC AT28HC191L-45PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-45DI AT28HC191L-45PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-45DM	24D6	Military (-55° to 125°C)
			AT28HC191L-45DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC191L-55DC AT28HC191L-55PC	24D6 24P6	Commercial (0° to 70°C)
			AT28HC191L-55DI AT28HC191L-55PI	24D6 24P6	Industrial (-40° to 85°C)
			AT28HC191L-55DM	24D6	Military (-55° to 125°C)
			AT28HC191L-55DM/883	24D6	Military/883C Class B, Fully Compliant (-55° to 125°C)

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Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

16K (2K x 8) High Speed Electrically Erasable CMOS PROM

Features

- Fast Access Time - 35ns
- Low Power Dissipation
  - 100 µA Standby Current (AT28HC291L)
  - 80 mA Active Current
- E^2PROM Technology - 100% Reprogrammable
- Direct Replacement for Bipolar PROMs
- Reprogrammable 1000 times
- Chip Clear
- JEDEC Approved Byte-Wide Pinout
  - Space-Saving 300 mil Wide Package
- CMOS and TTL Compatible Inputs and Outputs
- High Reliability High Speed CMOS Technology
- Full Military, Commercial, and Industrial Temperature Ranges

Description

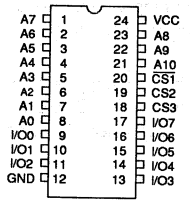
The AT28HC291/291L are a pair of high-speed, low-power 2,048 words by 8 bit CMOS PROMs. The high speed AT28HC291 offers access times to 35ns while the AT28HC291L provides low standby current consumption of just 100µA. Both devices are packaged in 24 pin dual inline packages using the JEDEC approved pinout for byte-wide PROMs. The AT28HC291 and AT28HC291L are supplied in space-saving 300 mil wide packages and also in 28 pad leadless chip carriers.

These devices are plug-in replacements for 16k bipolar PROMs, while offering distinct advantages in power consumption, performance and programming. Atmel's low power CMOS devices provide a direct power saving upgrade to systems originally using bipolar PROMs. The ultra-low standby power of the 28HC291L brings bipolar speeds to battery powered systems.

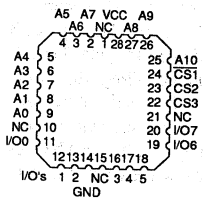
The electrically erasable and programmable memory cell allows for 100% testing of each memory location. The E^2PROM cell's low programming current permits devices to be programmed one byte at a time. On chip circuitry automatically erases each byte and rewrites it with the new data, permitting in socket reprogramming. The entire memory array can also be erased simultaneously, if desired, by using the device's "chip- clear" mode.

The fast access time of the devices makes them suitable for high-performance applications such as micro-control storage. In such an application the device allows for fast execution speeds, without penalizing storage density or power consumption. With a memory capacity of 2K bytes, these devices provide economical, reliable, and high-performance means of storing program instructions. System reliability is enhanced by the low power and inherent reliability of Atmel's 1.5 micron floating poly technology.

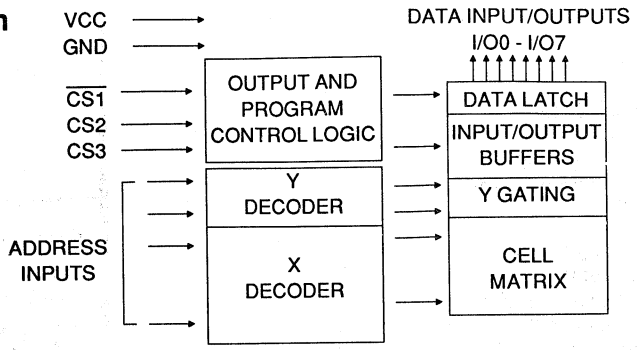
Pin Configurations



Pin Name	Function
A0-A10	Addresses
$\overline{CS1}$	Chip Select (Power Down Option)
CS2	Chip Select
CS3	Chip Select
I/O0-I/O7	Data
NC	No Connect



Block Diagram



Operating Modes

Mode	CS3	CS2	$\overline{CS1}$	I/O
Read	V_{IH}	V_{IH}	V_{IL}	D_{OUT}
Standby	X(1)	X	V_{IH}	High Z
Output Disable	V_{IL}	X	X	High Z
Output Disable	X	V_{IL}	X	High Z
Write(2)	V_{IL}	V_{IL}	V_H (3)	D_{IN}
Verify	V_{IH}	V_{IH}	V_H	D_{OUT}
Chip Clear	V_{IL}	V_H	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0 \pm 0.5V$.

Device Operation

READ: When $\overline{CS1}$ is low and CS2 and CS3 are high, the data stored at the memory location determined by the address inputs is asserted on the outputs of the device. The outputs are put in a high impedance state whenever CS2 or CS3 is low or whenever $\overline{CS1}$ is high. The availability of three control lines gives the designer flexibility in preventing bus contention.

STANDBY: The AT28HC291L consumes less than 550µW when deselected by raising $\overline{CS1}$ to Vcc-0.3V. This part retains the fast chip select times from CS2 and CS3 that are common to the AT28HC291.

PROGRAMMING: A 12 volt input is required on the $\overline{CS1}$ pin in order to program the devices. This input voltage is not needed to supply the programming current required by the memory cells as all high voltages used inside the chip are self-generated. After $\overline{CS1}$ is raised to 12 volts with CS2 low and CS3 high, CS3 is pulsed low to begin the internally timed write cycle. The address location presented to the device on the falling edge of the CS3 signal is written with the data that is presented to the device on the rising edge of CS3. An entire eight bit byte is programmed during each programming cycle. Any byte can be programmed to any data pattern regardless of the current data in that byte. An internal timer uses 1 ms to program a byte. No additional time is required nor are any additional programming pulses.

VERIFY: A verify of programmed data may be performed with $\overline{CS1}$ at 12 volts by taking CS2 and CS3 to VIH. The verify works exactly as a device read except that CS1 is at 12 volts rather than VIL.

MEMORY CELL: AT28HC291 family of parts uses fully reprogrammable E^2PROM cells to store data. Unlike the one time programmable fuse link cells commonly found in bipolar PROMs, E^2PROM cells allow each bit to be fully tested before shipment by Atmel. The electrical reprogrammability of E^2PROM cells allows for multiple patterns to be written into each device during testing to ensure proper programming, functioning and timing. All cells may be reprogrammed up to 1000 times by the user.

CHIP CLEAR: The entire contents of these memory devices may be set to the high state by the chip clear function. By setting $\overline{CS1}$ low and CS2 to 12 volts, the chip is cleared when a 10 msec low pulse is applied to CS3.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} +0.6V
Voltage on $\overline{CS1}$, CS2 and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. and A.C. Operating Range

		AT28HC291-35	AT28HC291-45 AT28HC291L-45	AT28HC291-55 AT28HC291L-55
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	—	-40°C - 85°C	-40°C - 85°C
	Mil.	—	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=0V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{CC1}	V_{CC} Standby Current	$\overline{CS1}$=V_{IH} ADDR=0/V_{CC}	AT28HC291L		3	mA
			AT28HC291		60	mA
I_{CC}	V_{CC} Active Current	f=10MHz; I_{OUT}=0mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL}=12mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4		V

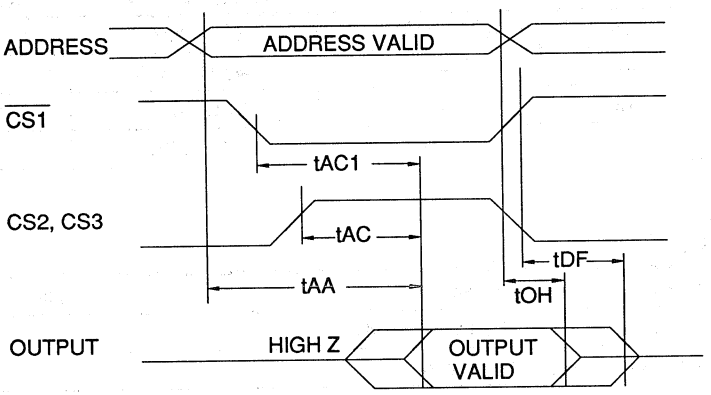
Pin Capacitance (f=1MHz T=25°C) [4]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

A.C. Characteristics for Read Operation [1]

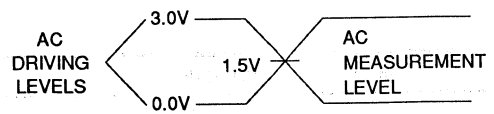
Symbol	Parameter	AT28HC291 -35 Min	AT28HC291 -35 Max	AT28HC291 -45 Min	AT28HC291 -45 Max	AT28HC291 -55 Min	AT28HC291 -55 Max	AT28HC291L -45 Min	AT28HC291L -45 Max	AT28HC291L -55 Min	AT28HC291L -55 Max	Units
t_{AA} [2]	Address to Output Delay		35		45		55		45		55	ns
t_{AC} [2]	CS2, CS3 to Output Delay		25		30		40		30		40	ns
t_{AC1} [2]	$\overline{CS1}$ to Output Delay		30		35		40		45		55	ns
t_{DF} [3,4]	$\overline{CS1}$, CS2, CS3 to Output Float	0	25	0	30	0	40	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{CS1}$,CS2, CS3, or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms



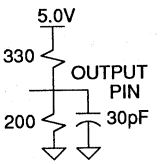
Notes:
1. CL=30pF
2. $\overline{CS}$, CS2 or CS3 may be delayed up to t_{AA}-t_{AC} after the address transition without impact on t_{AA}.
3. t_{DF} is specified from $\overline{CS1}$, CS2, or CS3, whichever occurs first.
4. This parameter is only characterized and is not 100% tested.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns

Output Test Load



A.C. Write Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width	50		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WC}	Write Cycle Time	1			ms
t_{VPS}	Programming Set-up Time	2			µs
t_{AA}	Address to Output Delay			100	ns
t_{AC}	CSn to Output Delay			100	ns
t_{DF}	CSn to Output Float			60	ns

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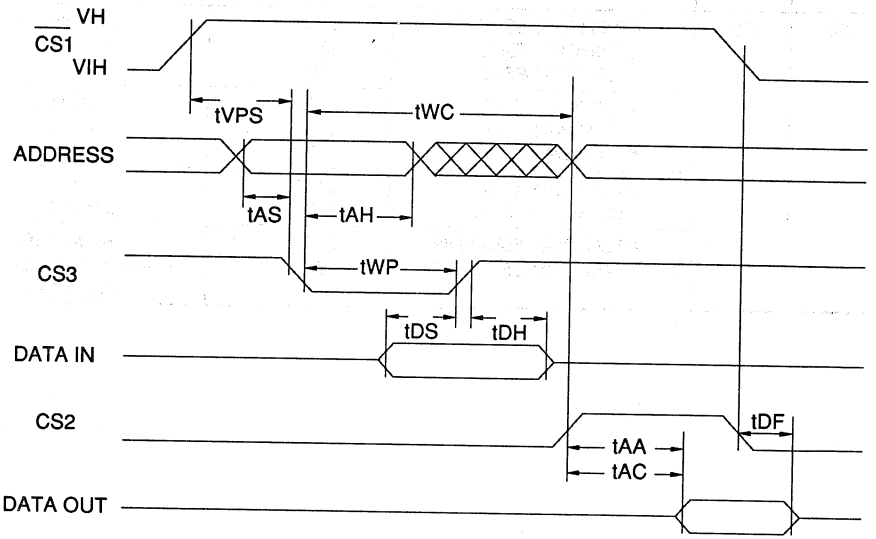
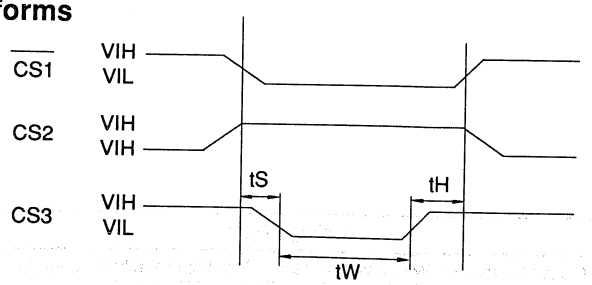
A.C. Write Waveforms



Chip Erase Waveforms



$t_S = t_H = 1\mu sec$ (min.)
$t_W = 10msec$ (min.)
$V_H = 12 \pm 0.5V$

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	80	60	AT28HC291-35DC AT28HC291-35PC	24D3 24P3	Commercial (0° to 70°C)
45	80	60	AT28HC291-45DC AT28HC291-45LC AT28HC291-45PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291-45DI AT28HC291-45LI AT28HC291-45PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291-45DM AT28HC291-45LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291-45DM/883 AT28HC291-45LM/883	24D3 28L	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	60	AT28HC291-55DC AT28HC291-55LC AT28HC291-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291-55DI AT28HC291-55LI AT28HC291-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291-55DM AT28HC291-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291-55DM/883 AT28HC291-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Ordering Information

tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	80	3	AT28HC291L-45DC AT28HC291L-45PC	24D3 24P3	Commercial (0° to 70°C)
			AT28HC291L-45DI AT28HC291L-45PI	24D3 24P3	Industrial (-40° to 85°C)
			AT28HC291L-45DM	24D3	Military (-55° to 125°C)
			AT28HC291L-45DM/883	24D3	Military/883C Class B, Fully Compliant (-55° to 125°C)
55	80	3	AT28HC291L-55DC AT28HC291L-55LC AT28HC291L-55PC	24D3 28L 24P3	Commercial (0° to 70°C)
			AT28HC291L-55DI AT28HC291L-55LI AT28HC291L-55PI	24D3 28L 24P3	Industrial (-40° to 85°C)
			AT28HC291L-55DM AT28HC291L-55LM	24D3 28L	Military (-55° to 125°C)
			AT28HC291L-55DM/883 AT28HC291L-55LM/883	24D3 28L	Military/883 Class B, Fully Compliant (-55° to 125°C)

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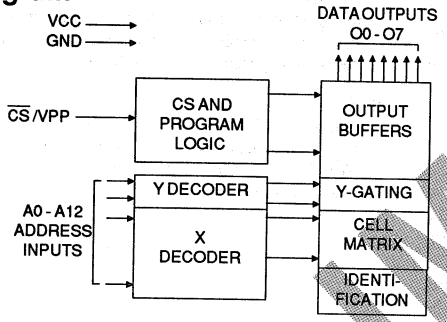
Package Type	
24D3	24 Lead, 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Features

- Bipolar Speed
  - Read Access Time - 35ns
- Low Power CMOS Operation
  - 25 mA max. Standby
  - 45 mA max. Active at 10 MHz
- Direct Bipolar PROM Replacement
- High Output Drive Capability
- Reprogrammable - 100µs/byte (typical)
  - Tested 100% for Programmability
- JEDEC Approved Byte-Wide Pinout
  - 300 mil DIP, 600 mil DIP and LCC packages
- CMOS and TTL Compatible Inputs and Outputs
- High Reliability Latch-Up Resistant CMOS Technology
- Integrated Product Identification Code
- Full Military, Industrial and Commercial Temperature Ranges
- Fully Compatible with AT27HC641/2

Block Diagram



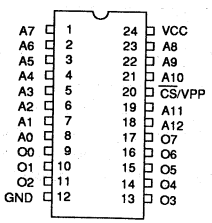
Description

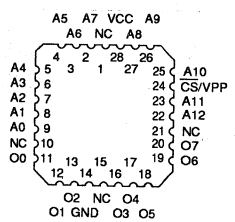
The AT27HC641R/642R chip family is a high-speed, low-power 65,536 bit reprogrammable read only memory (PROM), which is UV erasable, organized as 8K x 8 bits. All devices require only one 5V power supply in normal read mode operation. All bytes on the 641R and 642R parts can be accessed in less than 35ns, making these parts ideal for high-performance systems without penalizing bit density or power consumption.

The 640R series of devices come in a choice of JEDEC-approved 24-pin DIP or 28 pad LCC packages, providing a direct power saving CMOS upgrade for systems originally using Bipolar PROMs. The AT27HC641R is available in a standard 600 mil cerdip or one-time programmable plastic (OTP) package, and LCC package, while the AT27HC642R is available in a space-saving 300 mil cerdip or plastic (OTP) package.

Pin Configurations

Pin Name	Function
A0-A12	Addresses
$\overline{CS}$/V_{PP}	Chip Select/V_{PP}
O0-O7	Outputs





64K (8K x 8) Reprogrammable CMOS PROM

Preliminary

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Description (Continued)

Atmel's 1.2 micron, high-speed CMOS technology provides optimum speed, low-power and high noise immunity. Power consumption on the AT27HC641 and AT27HC642 is typically only 30 mA in Active Mode and less than 10 mA in Standby. The high speed CMOS process is an extension of Atmel's high quality and highly manufacturable floating poly PROM technology. The ability to reprogram the PROM, which is fully tested before shipment, provides inherently better programmability and reliability than one-time fusable PROMs.

With a storage capacity of 8K bytes, Atmel's 640R series parts allow firmware to be stored reliably and to be accessed at bipolar PROM speeds. All the 640R series parts have exceptional output drive capability - source 4 mA and sink 16 mA per output.

Atmel's 640R series chips also have additional features to ensure high-quality and efficient production use. The Rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Erasure Characteristics

The entire memory array of an Atmel 640R series chip is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any PROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
$\overline{CS}/V_{PP}$ Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CS}/V_{PP}$	Ai	Vcc	Outputs
Read	V_{IL}	Ai	Vcc	DOUT
Standby	V_{IH}	X(1)	Vcc	High Z
Rapid Program(2)	V_{PP}	Ai	Vcc	DIN
PGM Verify	V_{IL}	Ai	Vcc	DOUT
Product Identification(4)	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A12=V_{IL}	Vcc	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

D.C. and A.C. Operating Conditions for Read Operation

		AT27HC641R / AT27HC642R				
		-35	-45	-55	-70	-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{PP1}	$\overline{CS}/V_{PP}$ (1) Read/Standby Current	$\overline{CS}/V_{PP}$=-0.1V to V_{CC}+1V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CS}/V_{PP}$=V_{CC}-0.3 to V_{CC}+1.0V	Com.		25	mA
			Ind.,Mil.		30	mA
		I_{SB2} (TTL) $\overline{CS}/V_{PP}$=2.0 to V_{CC}+1.0V	Com.		25	mA
			Ind.,Mil.		30	mA
I_{CC}	V_{CC} Active Current	f=10MHz,I_{OUT}=0mA, $\overline{CS}/V_{PP}$=V_{IL}	Com.		45	mA
			Ind.,Mil.		50	mA
I_{OS} (2)	Output Short Circuit Current	V_{OUT}=0V			-100	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=16mA			.4	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-4.0mA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$, and removed simultaneously or after $\overline{CS}/V_{PP}$.

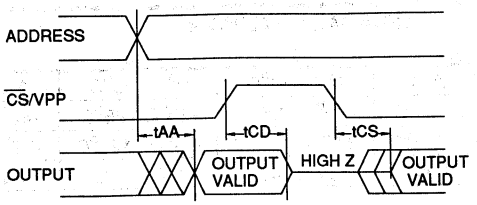
2. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

A.C. Characteristics for Read Operation

			AT27HC641R / AT27HC642R										
			-35		-45		-55		-70		-90		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{AA} (4)	Address to Output Delay	Com.		35		45		55		70		90	ns
		Ind.,Mil				45		55		70		90	ns
t_{CS} (2,4)	$\overline{CS}/V_{PP}$ to Output Delay			25		30		35		45		55	ns
t_{CD} (3,4,5)	$\overline{CS}/V_{PP}$ to Output Float		0	25	0	30	0	35	0	40	0	45	ns

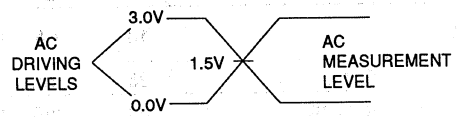
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



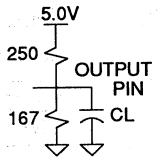
Notes:
1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.
2. Asserting $\overline{CS}/V_{PP}$ may be delayed up to t_{AA} - t_{CS} after the address transition without impact on access time.
3. This parameter is only sampled and is not 100% tested.
4. C_L = 30pF, add 10ns for C_L = 100pF.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



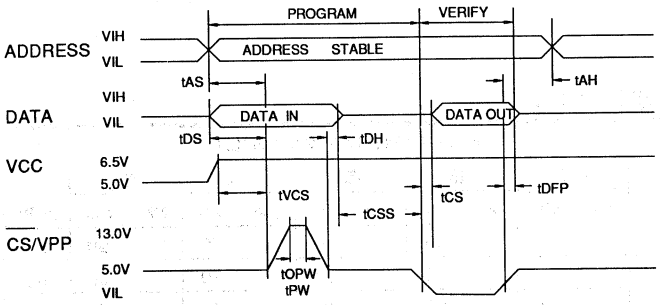
Note: C_L=30pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing References are 0.0V for V_{IL} and 3.0V for V_{IH}.
2. t_{CS} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{CS}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=16mA		.4	V
V_{OH}	Output High Volt.	I_{OH}=-4.0mA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	$\overline{CS}/V_{PP}$ Supply Current	$\overline{CS}/V_{PP}=V_{PP}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{CS}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CSS}	$\overline{CS}/V_{PP}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{CS}/V_{PP}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CS}/V_{PP}$ Program Pulse Width	(Note 3)	95	105	µs
t_{CS}	Data Valid from $\overline{CS}/V_{PP}$			70	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 5ns
Input Pulse Levels .....0.0V to 3.0V
Input Timing Reference Level 1.5V
Output Timing Reference Level 1.5V

Notes:

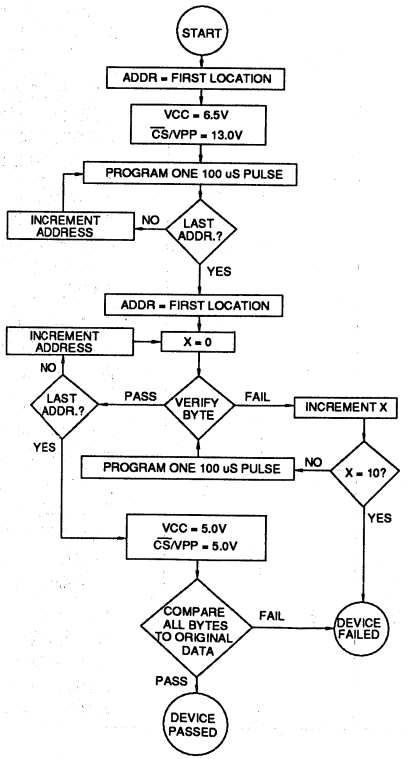
1. V_{CC} must be applied simultaneously or before $\overline{CS}/V_{PP}$ and removed simultaneously or after $\overline{CS}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 27HC641R/2R Integrated Product Identification Code:

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	1	0	0	0	0	10

Rapid Programming Algorithm

A 100µs $\overline{CS}/V_{PP}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{CS}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100µs $\overline{CS}/V_{PP}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{CS}/V_{PP}$ is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
35	45	25	AT27HC641R-35DC AT27HC642R-35DC AT27HC641R-35LC	24DW6 24DW3 28LW	Commercial (0°C to 70°C)
45	45	25	AT27HC641R-45DC AT27HC642R-45DC AT27HC641R-45LC AT27HC641R-45PC AT27HC642R-45PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
45	50	30	AT27HC641R-45DI AT27HC642R-45DI AT27HC641R-45LI AT27HC641R-45PI AT27HC642R-45PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-45DM AT27HC642R-45DM AT27HC641R-45LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-45DM/883 AT27HC642R-45DM/883 AT27HC641R-45LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	45	25	AT27HC641R-55DC AT27HC642R-55DC AT27HC641R-55LC AT27HC641R-55PC AT27HC642R-55PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
55	50	30	AT27HC641R-55DI AT27HC642R-55DI AT27HC641R-55LI AT27HC641R-55PI AT27HC642R-55PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-55DM AT27HC642R-55DM AT27HC641R-55LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-55DM/883 AT27HC642R-55DM/883 AT27HC641R-55LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	45	25	AT27HC641R-70DC AT27HC642R-70DC AT27HC641R-70LC AT27HC641R-70PC AT27HC642R-70PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
70	50	30	AT27HC641R-70DI AT27HC642R-70DI AT27HC641R-70LI AT27HC641R-70PI AT27HC642R-70PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	30	AT27HC641R-70DM AT27HC642R-70DM AT27HC641R-70LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-70DM/883 AT27HC642R-70DM/883 AT27HC641R-70LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	45	25	AT27HC641R-90DC AT27HC642R-90DC AT27HC641R-90LC AT27HC641R-90PC AT27HC642R-90PC	24DW6 24DW3 28LW 24P6 24P3	Commercial (0°C to 70°C)
90	50	30	AT27HC641R-90DI AT27HC642R-90DI AT27HC641R-90LI AT27HC641R-90PI AT27HC642R-90PI	24DW6 24DW3 28LW 24P6 24P3	Industrial (-40°C to 85°C)
			AT27HC641R-90DM AT27HC642R-90DM AT27HC641R-90LM	24DW6 24DW3 28LW	Military (-55°C to 125°C)
			AT27HC641R-90DM/883 AT27HC642R-90DM/883 AT27HC641R-90LM/883	24DW6 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
45	50	30	5962-87515 01 JX 5962-87515 01 KX 5962-87515 01 LX 5962-87515 01 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
55	50	30	5962-87515 02 JX 5962-87515 02 KX 5962-87515 02 LX 5962-87515 02 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
70	50	30	5962-87515 03 JX 5962-87515 03 KX 5962-87515 03 LX 5962-87515 03 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
90	50	30	5962-87515 04 JX 5962-87515 04 KX 5962-87515 04 LX 5962-87515 04 3X	24DW6 24CW 24DW3 28LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24DW6	24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

512K (32K x 16) One Time Programmable (OTP) CMOS PROM

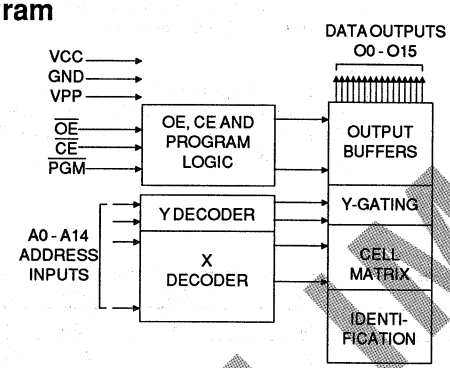
Preliminary

5

Features

- Low Power CMOS Operation
  - 100 µA max. Standby
  - 30 mA max. Active at 5 MHz
- Fast Read Access Time - 150ns
- JEDEC Standard Packages
  - 40-Lead 600 mil OTP Plastic DIP
  - 44-Pad OTP PLCC
- 5V±10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100µs/word (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Block Diagram



Description

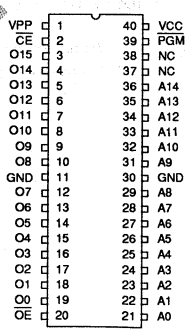
The AT32C16 chip is a low-power, high-performance One Time Programmable (OTP) Read Only Memory (PROM) organized 32K x 16. It requires only one 5V power supply in normal read mode operation. Any word can be accessed in less than 150ns, eliminating the need for speed reducing WAIT states. The by-16 organization makes these parts ideal for high-performance 16 and 32 bit microprocessor systems.

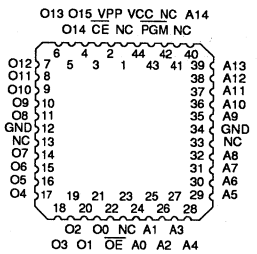
The AT32C16 is ideal for replacing the two 256K EPROMs normally used on personal computer motherboards.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.





Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

Description (Continued)

The AT32C16 comes in a choice of industry standard JEDEC-approved packages including; 40-pin DIP one time programmable (OTP) plastic or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 32K word storage capability, the AT32C16 allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 32C16 have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT32C16			
		-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V			5	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP}=3.8 to V_{CC}+0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$=V_{CC}-0.3 to V_{CC}+1.0V			100	µA
		I_{SB2} (TTL) $\overline{CE}$=2.0 to V_{CC}+1.0V			1	mA
I_{CC}	V_{CC} Active Current	f=5MHz,I_{OUT}=0mA, $\overline{CE}$=V_{IL}	Com.		30	mA
			Ind.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3		V
		I_{OH}=-2.5mA		3.5		V
		I_{OH}=-400µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

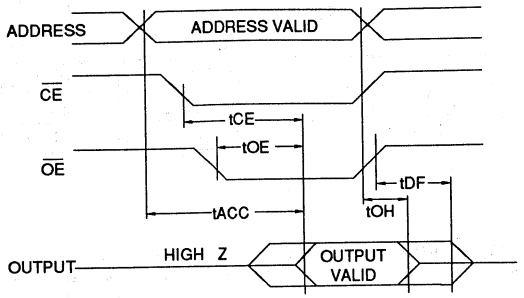
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT32C16								
				-15		-17		-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$=$\overline{OE}$ =V_{IL}	Com.		150		170		200		250	ns
			Ind.				170		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}			150		170		200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}			65		65		75		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}			40		50		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$=$\overline{OE}$ =V_{IL}			0		0		0		0	ns

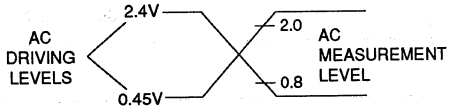
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



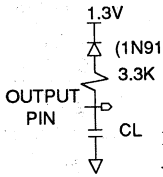
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



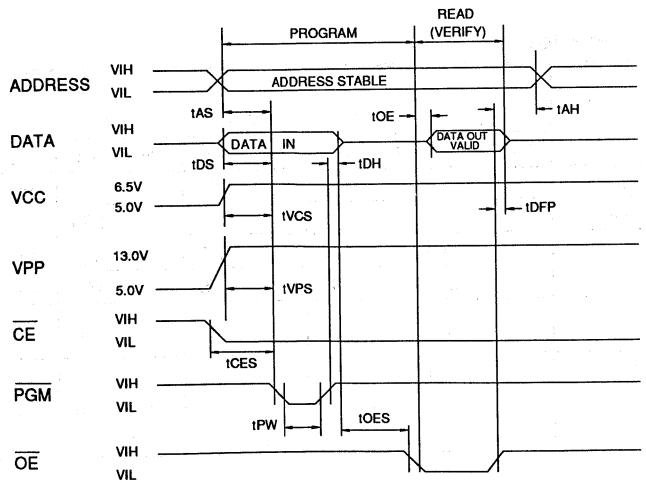
Note: C_L=100pF including jig capacitance.

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT32C16 a 0.1µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, V_{PP}=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels .....0.45V to 2.4V
Input Timing Reference Level .....0.8V to 2.0V
Output Timing Reference Level .....0.8V to 2.0V

Notes:

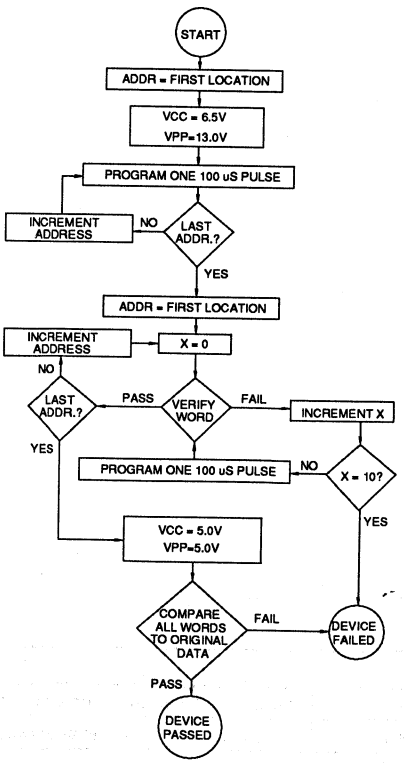
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Atmel's 32C16 Integrated Product Identification Code:

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	1	0	00F2

Rapid Programming Algorithm

A 100µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
170	30	0.1	AT32C16-17JC AT32C16-17PC	44J 40P6	Commercial (0°C to 70°C)
170	40	0.2	AT32C16-17JI AT32C16-17PI	44J 40P6	Industrial (-40°C to 85°C)
200	30	0.1	AT32C16-20JC AT32C16-20PC	44J 40P6	Commercial (0°C to 70°C)
200	40	0.2	AT32C16-20JI AT32C16-20PI	44J 40P6	Industrial (-40°C to 85°C)
250	30	0.1	AT32C16-25JC AT32C16-25PC	44J 40P6	Commercial (0°C to 70°C)
250	40	0.2	AT32C16-25JI AT32C16-25PI	44J 40P6	Industrial (-40°C to 85°C)

Package Type	
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Contents

Section 6

CMOS SRAMs

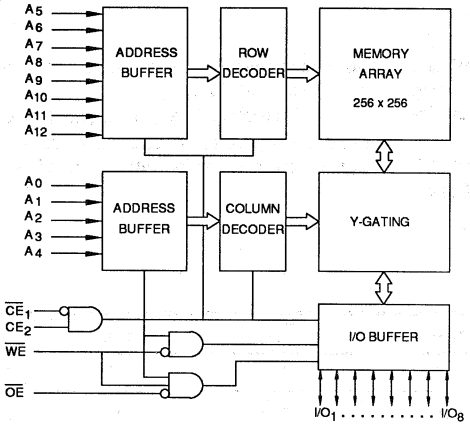
Features

- Fast Read Access Time - 100ns
- Low Power
  - 35mA Maximum (Active)
  - 100µA Maximum (Standby)
- 2V Data Retention
- Fully Static: No Clock Required
- Three Control Inputs ($\overline{CE_1}$, CE_2, and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 5V ± 10% Supply
- 28 Lead Dual In-line and Surface Mount Packages
- JEDEC Pinout
- Commercial and Industrial Temperature Ranges

64K (8K x 8) CMOS SRAM

6

Block Diagram



Description

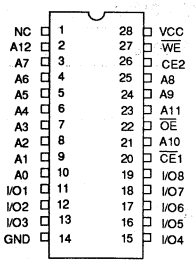
The AT3864L is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L offers access times down to 100ns with power dissipation of under 200mW. When the AT3864L is deselected, the standby current is just 100µA. In addition, the AT3864L offers a data retention capability of only 100µW power dissipation when operated on a 2V power supply.

The AT3864L powers down to the standby mode when deselected ($\overline{CE_1}$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected (CE_1 is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L is completely TTL compatible and requires a single 5V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE_1}$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Absolute Maximum Ratings*

Temperature Under Bias	-40° C to 85° C
Storage Temperature	-55° C to 125° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3V to V_{CC}+0.3V
All Output Voltages with Respect to Ground	-0.3V to V_{CC}+0.3V
Maximum Supply Voltage	+7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 100 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X(1)	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT3864L-10	AT3864L-12	AT3864L-15
Operating Temperature (Case)	Commercial	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Industrial	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%

D.C. and Operating Characteristics

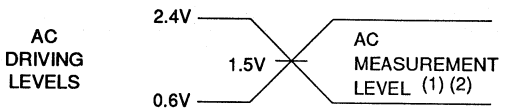
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}=0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V or CE_2 = -0.3V to 0.8V or $\overline{OE}$ = 2.2V to V_{CC} + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2V$ or $\overline{CE_1} \ge V_{CC}$ - 0.2V, $CE_2 \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$ V_{IN} = 0 to V_{CC}		2	100	µA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3V to 0.8V or $\overline{CE_1}$ = 2.2V to V_{CC} +0.3V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3V to 0.8V, CE_2 = 2.2V to V_{CC} + 0.3V, I_{OUT} = 0mA, min cycle		20	35	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2V		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4			V

Pin Capacitance (f=1MHz T=25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5ns.
2. Output load: 1TTL gate + 100pF.

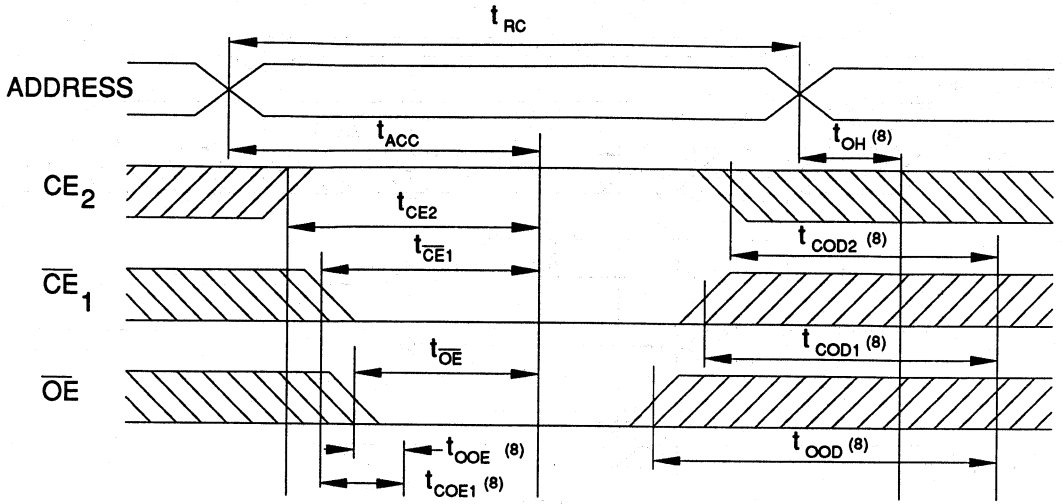
A.C. Characteristics for Read

Symbol	Parameter	AT3864L-10		AT3864L-12		AT3864L-15		UnitS
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		ns
t_{ACC}	Address Access Time		100		120		150	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		100		120		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		50		60		70	ns
t_{OH}	Output Hold Time	15		15		15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		10		10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		5		5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		45		45		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		40		40		50	ns

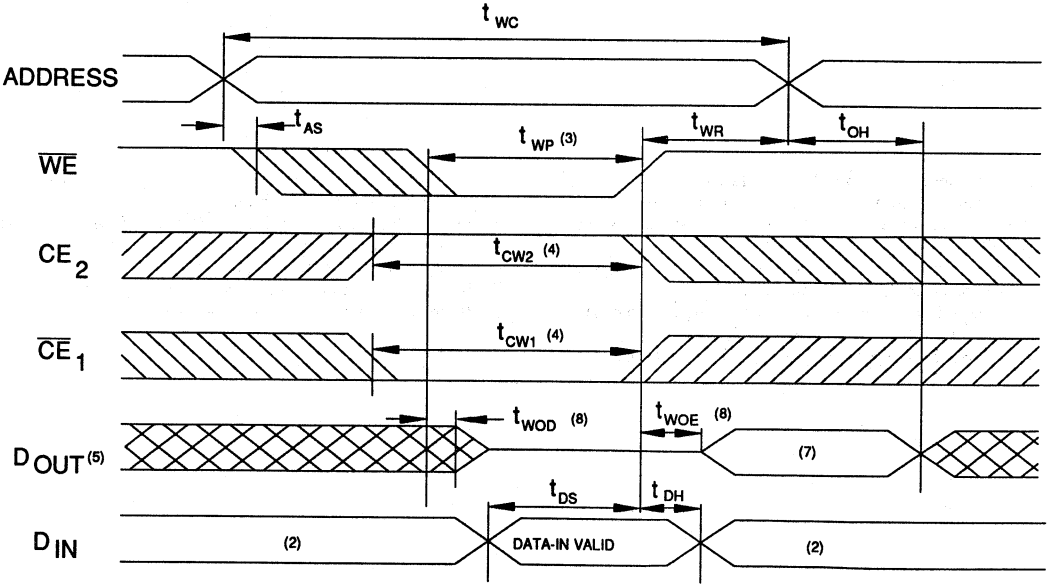
A.C. Characteristics for Write

Symbol	Parameter	AT3864L-10		AT3864L-12		AT3864L-15		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	60		70		90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	80		80		90		ns
t_{WR}	Write Recovery Time	0		0		0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		0		0		ns
t_{DS}	Data Setup Time	40		50		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		0		0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		5		5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		40		40		50	ns

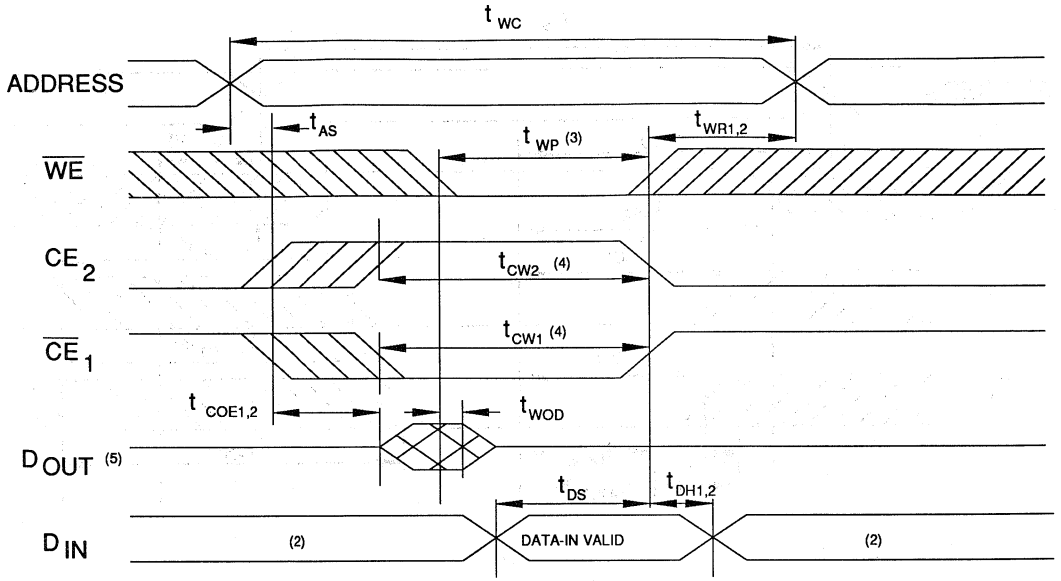
A.C. Waveforms for Read Cycle (1)



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) (6)



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) (6)



Notes:

1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE_1}$, CE_2 and $\overline{WE}$ are all active at the same time.
   A Write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE_1}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$=V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE}_1 \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$ - 0.2V or $CE_2 \leq 0.2V$	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2V$	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V $\overline{CE}_1 \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$-0.2V or $CE_2 \leq 0.2V$		1	50	µA
	I_{CCDR2}	V_{CC} = 3.0V, $CE_2 \leq 0.2V$		1	50	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC}=Read Cycle Time

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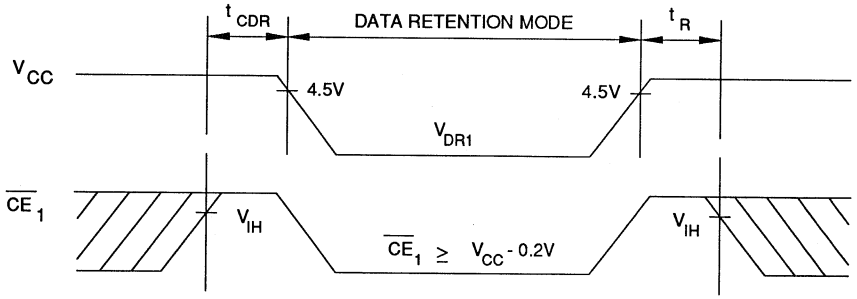
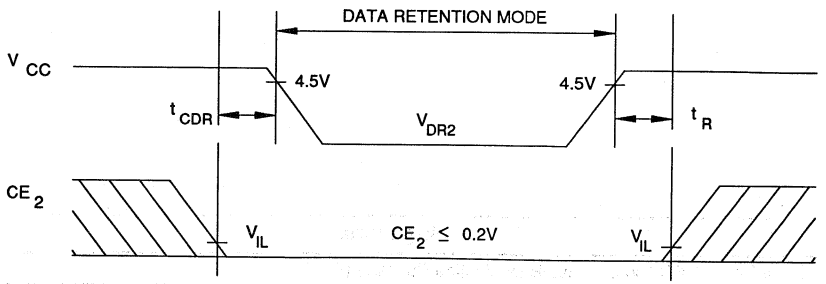
Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	35	0.1	AT3864L-10PC AT3864L-10RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-10PI AT3864L-10RI	28P6 28R	Industrial (-40° to 85°C)
120	35	0.1	AT3864L-12PC AT3864L-12RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-12PI AT3864L-12RI	28P6 28R	Industrial (-40° to 85°C)
150	35	0.1	AT3864L-15PC AT3864L-15RC	28P6 28R	Commercial (0° to 70°C)
			AT3864L-15PI AT3864L-15RI	28P6 28R	Industrial (-40° to 85°C)

Package Type	
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide Plastic Gull Wing Small Outline (SOIC)

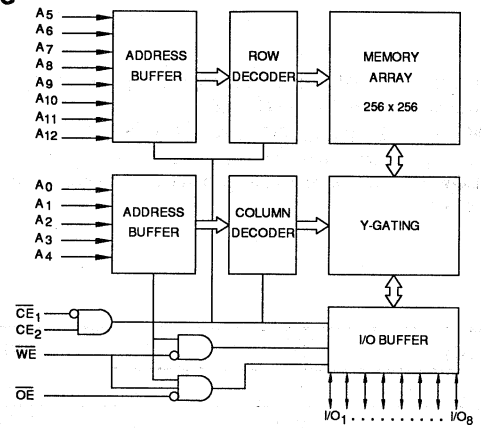
Features

- Fast Read Access Time - 150ns
- Low Power
  - 40mA Maximum (Active)
  - 1mA Maximum (Standby)
- 2V Data Retention
- Fully Static: No Clock Required
- Three Control Inputs ($\overline{CE_1}$, CE_2, and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 5V ± 10% Supply
- 28 Lead Dual In-line
- JEDEC Pinout
- Full Military Temperature Range

64K (8K x 8) CMOS SRAM

6

Block Diagram



Description

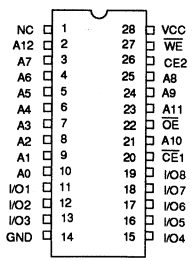
The AT3864L-15DMB is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L-15DMB offers access times down to 150ns with power dissipation of 220mW maximum. When the AT3864L-15DMB is deselected, the standby current is just 1mA. In addition, the AT3864L-15DMB offers a data retention capability of only 800µW power dissipation when operated on a 2V power supply.

The AT3864L-15DMB powers down to the standby mode when deselected ($\overline{CE_1}$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE_1}$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L-15DMB is completely TTL compatible and requires a single 5V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE_1}$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc, GND	Power, Ground
NC	No Connect



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 150° C
Storage Temperature	-65° C to 150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3V to V_{CC}+0.3V
All Output Voltages with Respect to Ground	-0.3V to V_{CC}+0.3V
Maximum Supply Voltage	+7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 800 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X(1)	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

	AT3864L-15
Operating Temperature (Case) Military	-55°C - 125°C
V_{CC} Power Supply	5V±10%

D.C. and Operating Characteristics

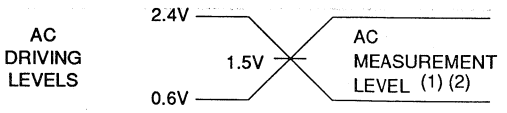
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}=0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V or CE_2 = -0.3V to 0.8V or $\overline{OE}$ = 2.2V to V_{CC} + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2V$ or $\overline{CE_1} \ge V_{CC}$ - 0.2V, $CE_2 \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$ V_{IN} = 0 to V_{CC}			1	mA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3V to 0.8V or $\overline{CE_1}$ = 2.2V to V_{CC} +0.3V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3V to 0.8V, CE_2 = 2.2V to V_{CC} + 0.3V, I_{OUT} = 0mA, min cycle		20	40	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2V		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4			V

Pin Capacitance (f=1MHz T=25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5ns.
2. Output load: 1TTL gate + 100pF.

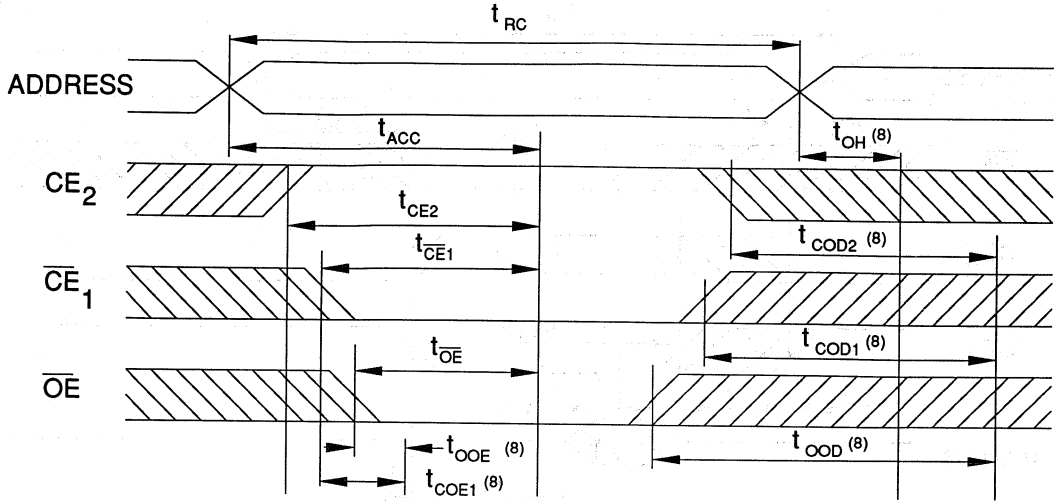
A.C. Characteristics for Read

Symbol	Parameter	AT3864L-15		Units
		Min	Max	
t_{RC}	Read Cycle Time	150		ns
t_{ACC}	Address Access Time		150	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		70	ns
t_{OH}	Output Hold Time	15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		50	ns

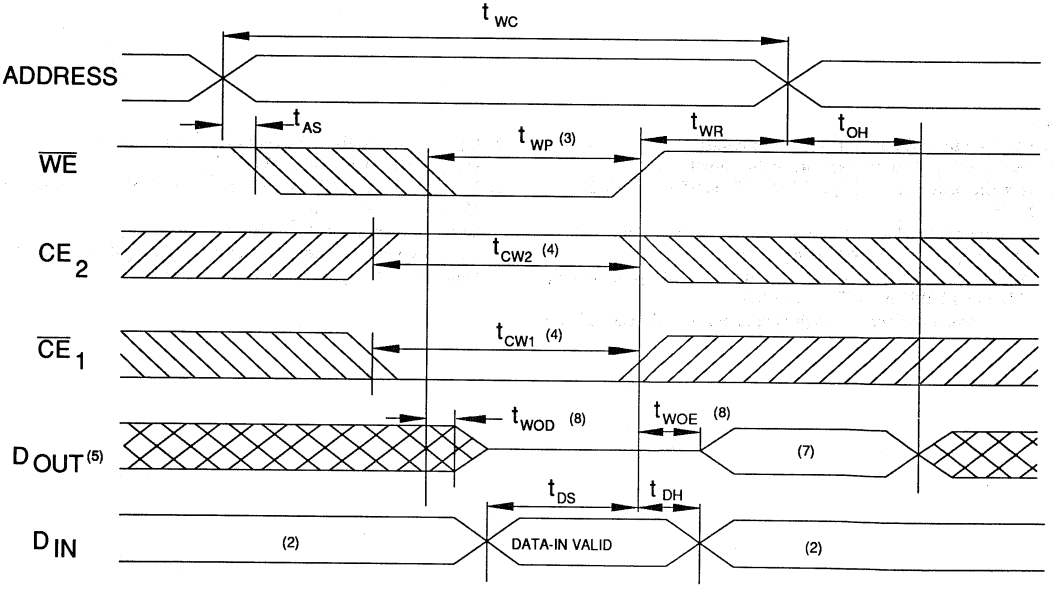
A.C. Characteristics for Write

Symbol	Parameter	AT3864L-15		Units
		Min	Max	
t_{WC}	Write Cycle Time	150		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	90		ns
t_{WR}	Write Recovery Time	0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		50	ns

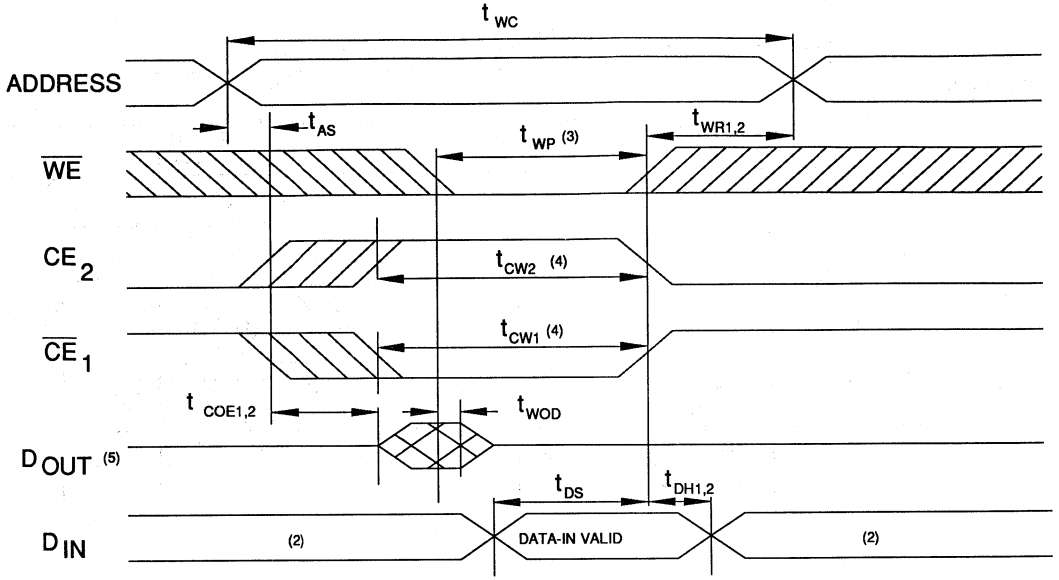
A.C. Waveforms for Read Cycle (1)



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) (6)



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) [6]



Notes:
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW.
   A Write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE_1}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$ is V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE}_1 \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$ - 0.2V or $CE_2 \leq 0.2V$	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2V$	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V $\overline{CE}_1 \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$-0.2V or $CE_2 \leq 0.2V$		1	400	µA
	I_{CCDR2}	V_{CC} = 3.0V, $CE_2 \leq 0.2V$		1	400	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC}=Read Cycle Time

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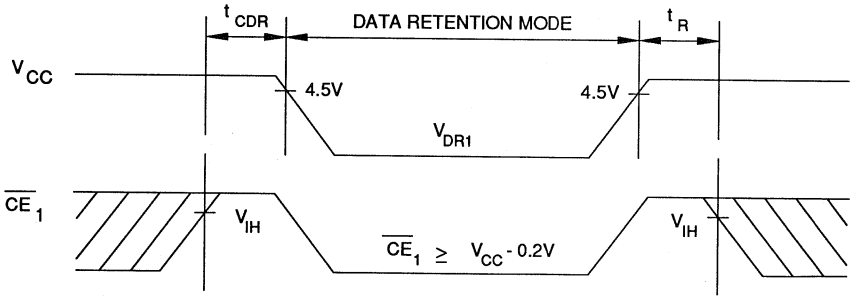
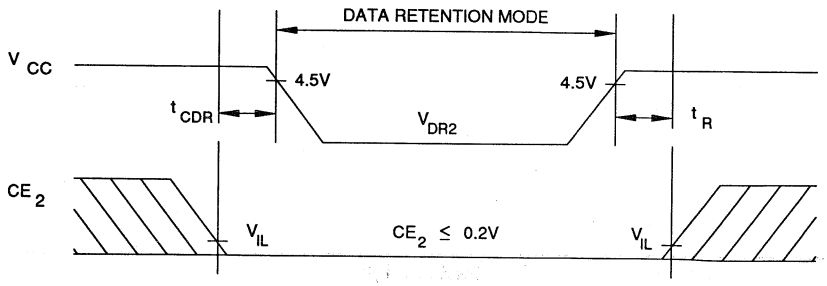
Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	1.0	AT3864L-15DMB	28D6	Military (-55° to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)

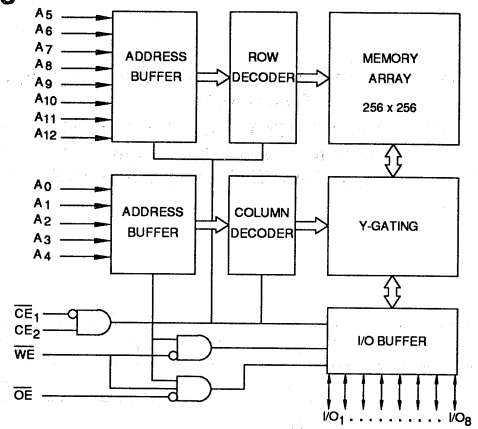
Features

- Fast Read Access Time - 200ns
- Low Power
  - 110mW Maximum (Active) at V_{CC} = 3.0V
  - 100µW Maximum (Standby)
- 2V Data Retention
- Fully Static: No Clock Required
- Three Control Inputs ($\overline{CE}_1$, CE_2, and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 3.0V to 5.5V Supply
- 28 Lead Dual In-line and Surface Mount Packages
- JEDEC Pinout
- Commercial Temperature Range

64K (8K x 8) Low Voltage CMOS SRAM

6

Block Diagram



Description

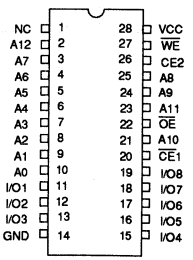
The AT38LV64 is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT38LV64 offers an access time of 200ns with power dissipation of under 110mW at 3 volts. When the AT38LV64 is deselected, the standby current is just 100µA. In addition, the AT38LV64 offers a data retention capability of only 100µW power dissipation when operated on a 2V power supply.

The AT38LV64 powers down to the standby mode when deselected ($\overline{CE}_1$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE}_1$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT38LV64 is completely TTL compatible and requires a single 3V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}_1$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Absolute Maximum Ratings*

Temperature Under Bias	0° C to 70° C
Storage Temperature	-55° C to 125° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3V to V_{CC}+0.3V
All Output Voltages with Respect to Ground	-0.3V to V_{CC}+0.3V
Maximum Supply Voltage	+7.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the 8 bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the 8 bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as 2 volts without impacting data integrity. Power dissipation will be reduced to 100 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X(1)	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT38LV64-20
Operating Temperature (Case)	Commercial	0°C - 70°C
V_{CC} Power Supply		3.0V to 5.5V

D.C. and Operating Characteristics

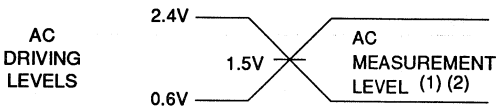
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}=0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2V to V_{CC} + 0.3V or $\overline{CE_2}$ = -0.3V to 0.8V or $\overline{OE}$ = 2.2V to V_{CC} + 0.3V or $\overline{WE}$ = -0.3V to 0.8V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$\overline{CE_2} \le 0.2V$ or $\overline{CE_1} \ge V_{CC}$ - 0.2V, $CE_2 \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$ V_{IN} = 0 to V_{CC}		2	100	µA
I_{SB2}	Standby Current (TTL)	$\overline{CE_2}$ = -0.3V to 0.8V or $\overline{CE_1}$ = 2.2V to V_{CC} +0.3V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3V to 0.8V, CE_2 = 2.2V to V_{CC} + 0.3V, I_{OUT} = 0mA, min cycle		20	35	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2V		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	2.4			V

Pin Capacitance (f=1MHz T=25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5ns.
2. Output load: 1TTL gate + 100pF.

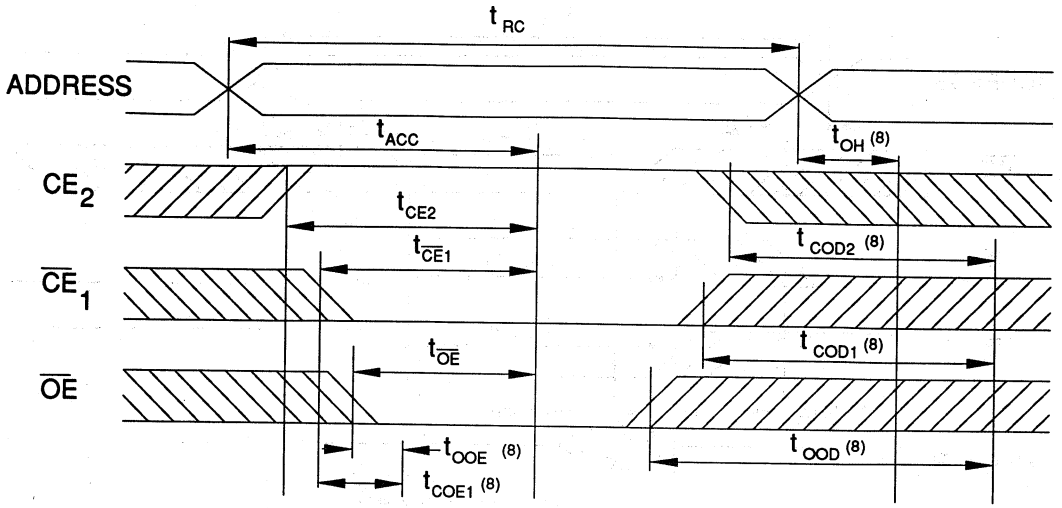
A.C. Characteristics for Read

Symbol	Parameter	AT38LV64-20		UnitS
		Min	Max	
t_{RC}	Read Cycle Time	200		ns
t_{ACC}	Address Access Time		200	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		200	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		80	ns
t_{OH}	Output Hold Time	15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		80	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		80	ns

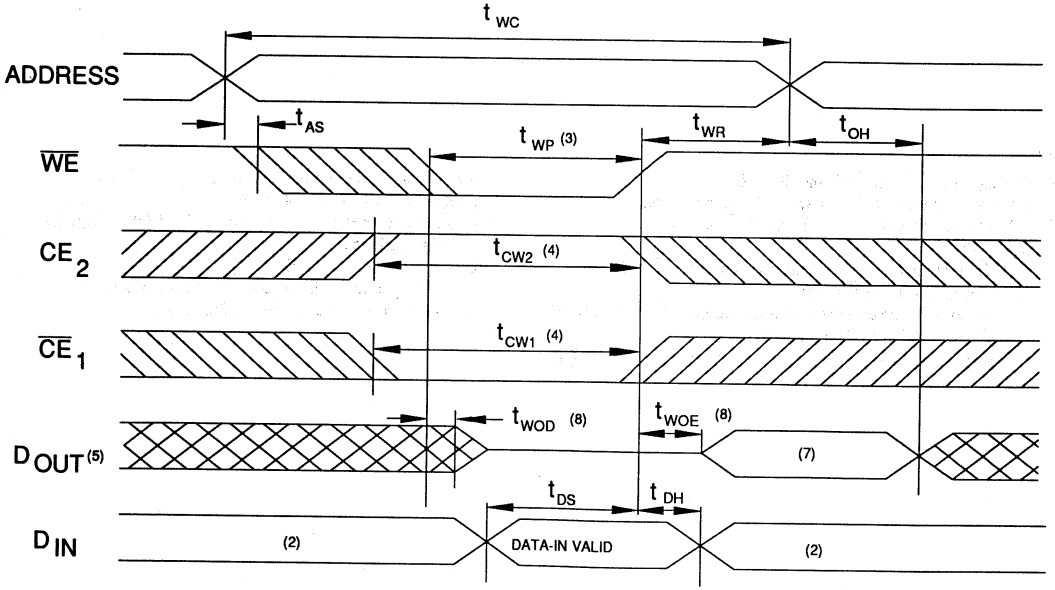
A.C. Characteristics for Write

Symbol	Parameter	AT38LV64-20		Units
		Min	Max	
t_{WC}	Write Cycle Time	200		ns
t_{AS}	Address Setup Time			ns
t_{WP}	Write Pulse Width	100		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	100		ns
t_{WR}	Write Recovery Time	25		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	25		ns
t_{DS}	Data Setup Time	90		ns
t_{DH}	Data Hold Time			ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		80	ns

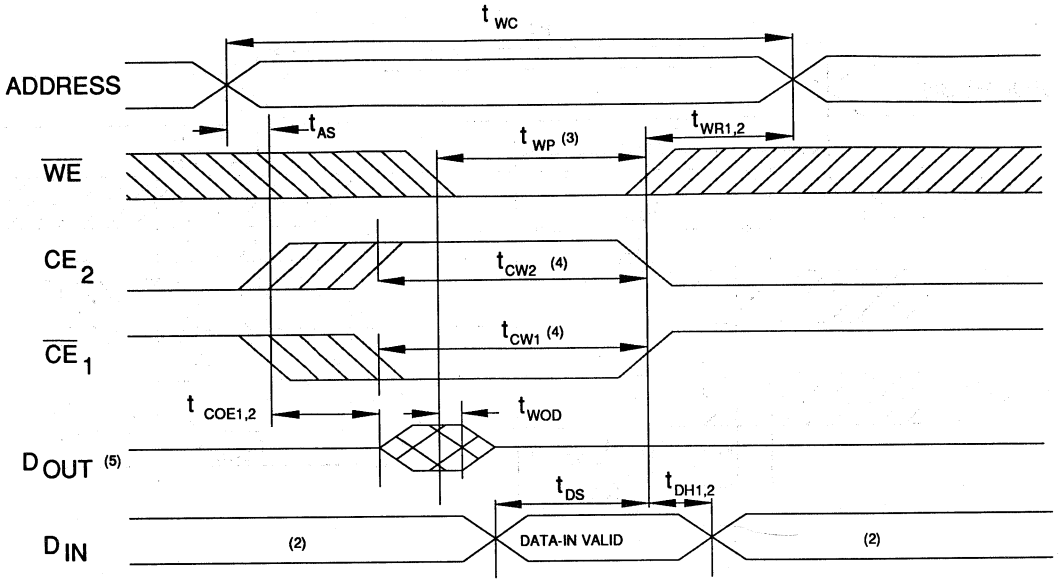
A.C. Waveforms for Read Cycle [1]



A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) [6]



Notes:

1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE_1}$, CE_2 and $\overline{WE}$ are all active at the same time.
   A Write begins at the latest transition among $\overline{CE_1}$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE_1}$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE_1}$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE_1}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$=V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE}_1 \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$ - 0.2V or $CE_2 \leq 0.2V$	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2V$	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0V $\overline{CE}_1 \geq V_{CC}$ - 0.2V $CE_2 \geq V_{CC}$-0.2V or $CE_2 \leq 0.2V$		1	50	µA
	I_{CCDR2}	V_{CC} = 3.0V, $CE_2 \leq 0.2V$		1	50	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC}=Read Cycle Time

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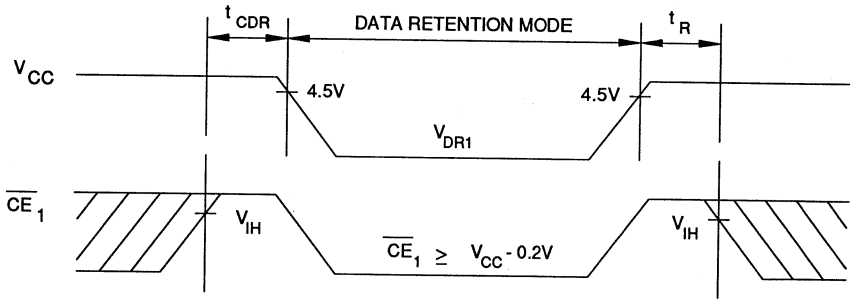
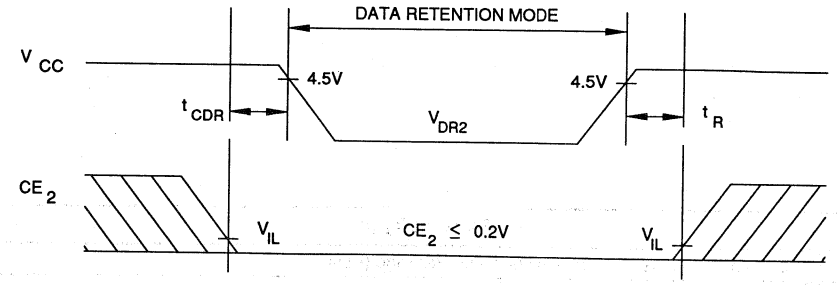
Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE_2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	35	0.1	AT38LV64L-20PC AT38LV64L-20RC	28P6 28R	Commercial (0° to 70°C)

Package Type	
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28R	28 Lead, 0.330" Wide Plastic Gull Wing Small Outline (SOIC)

Contents

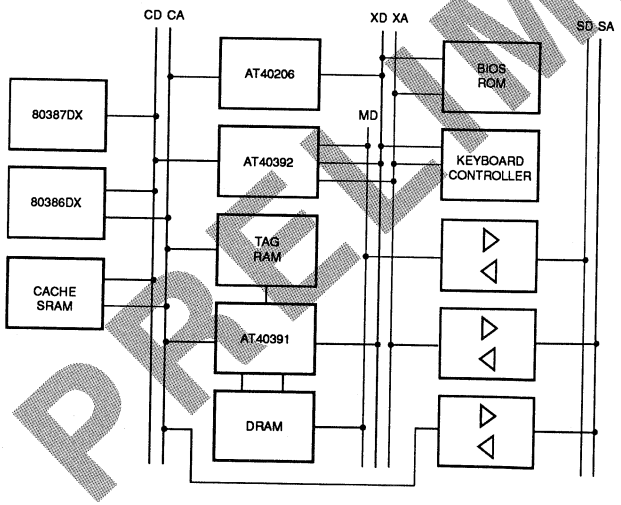
Section 7

CMOS Logic

Features

- Two-Chip PC/AT Compatible Chip Set for 80386DX Based Systems of up to 40 MHz
  - AT40391 System Controller
  - AT40392 Data Buffer Controller
- Two 160-Pin Quad Flatpacks, 1-Micron CMOS Process
- On-Chip Support For Direct-mapped Copy-back Cache
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Size of up to 64MB
- Support for 256K/1M/4M DRAM
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support For Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock
- 0 or 1 Wait State for 16-bit ISA Bus Cycles
- Support for 80387DX and 3167 Numeric Co-processors

Block Diagram



Description

The Atmel AT40391/2 chip set, consisting of the AT40391 and AT40392, is a 100% IBM PC/AT compatible chip set for 80386DX based systems of up to 40 MHz. The high integration and an on-chip copy-back, direct mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 IPC, a very high performance, yet low-cost, 80386DX motherboard can be built with a minimum number of components.

80386DX PC/AT Chip Set

Preliminary

7

Description (continued)

The AT40391 System Controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks: CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a copy-back, direct mapped cache controller and a paged mode DRAM controller. The AT40391 supports cache sizes up to 256 Kbytes (16-byte line size), and platform memory sizes up to 64 Mbytes.

The AT40392 performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40392 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM / EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.

The AT40391/2 PC/AT chip set is compatible with the AT40206 Integrated Peripheral Controller and works with BIOS from AMI, Phoenix, Award and Quadtel.

BIOS may be a registered trademark of IBM.

Ordering Information

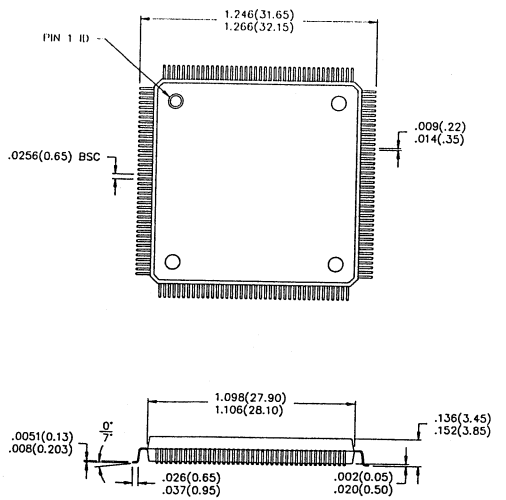
CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5V ± 5%	AT40391-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5V ± 5%	AT40391-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
40	5V ± 5%	AT40391-40 AT40392-40	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)

7

Packaging Information

160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)



Features

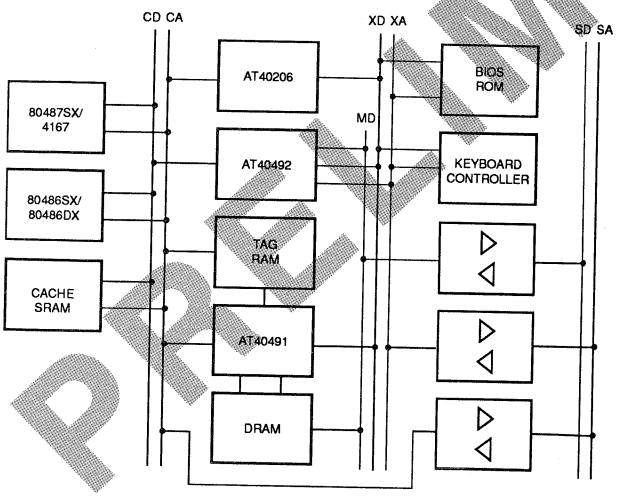
- Two-Chip PC/AT Compatible Chip Set for 80486 Based Systems of up to 33 MHz
  - AT40491 System Controller
  - AT40492 Data Buffer Controller
- Two 160-Pin Quad Flatpacks, 1-Micron CMOS Process
- On-Chip Support For Direct-mapped Copy-back Cache
- Supports 2,1,1,1 and 3,1,1,1 Cache Burst Cycles
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Sizes of up to 64MB
- Support for 1M and 4M DRAMs
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support For Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock Divide
- 0 or 1 Wait States for 16-bit ISA Bus Cycles
- Support for Weitek 4167 Numeric Co-processor

80486SX 80486DX PC/AT Chip Set

Preliminary

7

Block Diagram



Description

The Atmel AT40491/2 chip set, consisting of the AT40491 and AT40492, is a 100% IBM PC/AT compatible chip set for 80486SX and 80486DX based systems of up to 33 MHz. The high integration and an on-chip copy-back, direct mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 IPC, a very high performance, yet low-cost, 80486SX/80486DX motherboard can be built with a minimum number of components.

Description (continued)

The AT40491 System Controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks : CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a copy-back, direct mapped cache controller and a paged mode DRAM controller. The AT40491 support cache sizes up to 512 Kbytes (16-byte line size) and platform memory sizes up to 64 Mbytes.

The AT40492 performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40492 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM / EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.

The AT40491/2 PC/AT chip set is compatible with the AT40206 Integrated Peripheral Controller and works with BIOS from AMI, Phoenix, Award and Quadtel.

BIOS may be a registered trademark of IBM.

Ordering Information

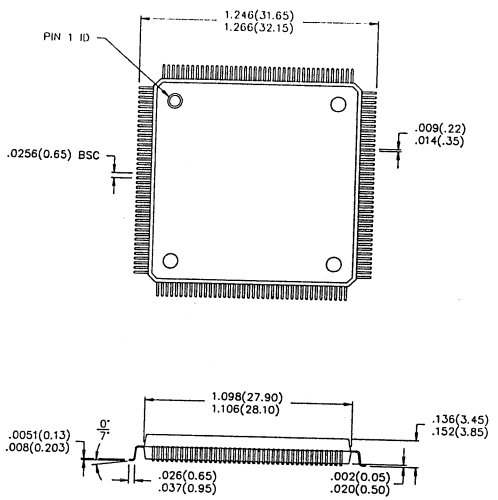
CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5V ± 5%	AT40491-25 AT40492-25	160Q 160Q	Commercial (0°C to 70°C)
33	5V ± 5%	AT40491-33 AT40492-33	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)

7

Packaging Information

160Q, 160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)



Contents

Section 8

CMOS EPLDs

8

Features

- 20-pin Universal EPLD
- Virtually Zero Standby Power
- Functional Replacement for Common 20-Pin Programmable Devices
  - I_{OL} = 24 mA
- High Performance CMOS EPROM Cell Technology
  - Erasable
  - Reconfigurable
  - 100% Testable
- 35 ns Max Propagation Delay (Commercial)
- 40 ns Max Propagation Delay (Industrial)
- Up to 18 Inputs and 8 Input/Output Macrocells
- Programmable Output Polarity
- Power-Up Reset on all Registers
- Register Preload Capability
- Synchronous Preset/Asynchronous Reset
- Security Fuse to Protect Duplication of Proprietary Designs
- Design Support Provided using many Popular Software Development Packages for PLDs
- Available in 300-mil-wide DIP with Quartz Window, Plastic DIP (OTP) or PLCC (OTP)
- Second Source to Signetic's PLC18V8Z/I

Zero-Standby Power 20-Pin EPLD

8

Description

The AT18V8Z is a universal EPLD featuring high performance and virtually zero-standby power for power sensitive applications. It is a reliable, user-configurable substitute for discrete TTL/CMOS logic. While compatible with TTL and HCT logic, the AT18V8Z can also replace HC logic over the V_{CC} range of 4.5 to 5.5 V.

The AT18V8Z is a two-level logic element comprised of 10 inputs, 74 AND gates (product terms) and 8 output Macro cells.

Each output features an "Output Macro Cell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the AT18V8Z is capable of emulating all common 20-pin programmable logic devices to reduce documentation, inventory, and manufacturing costs.

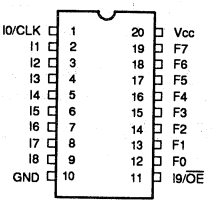
A power-up reset function and a Register Preload function have been incorporated in the AT18V8Z architecture to facilitate state machine design and testing.

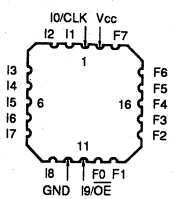
With a standby current of less than 100 µA and active power consumption of 1.5 mA/MHz, the AT18V8Z is ideally suited for power sensitive applications in battery operated/backed portable instruments and computers.

The AT18V8Z is also processed to industrial requirements for operation over an extended temperature range of -40°C to +85°C and supply voltage of 4.5 V to 5.5 V.

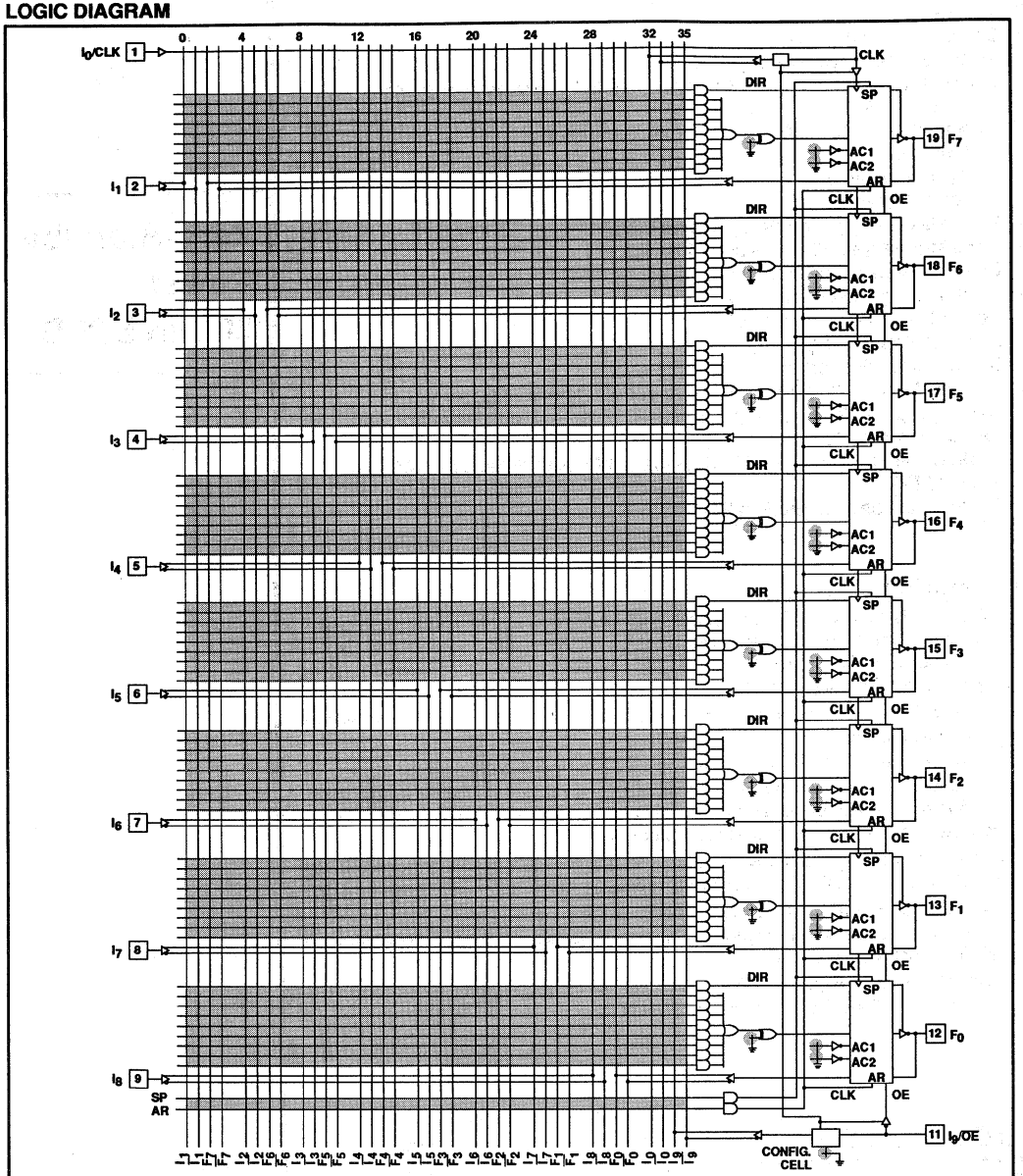
Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply





LOGIC DIAGRAM



NOTES:
In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

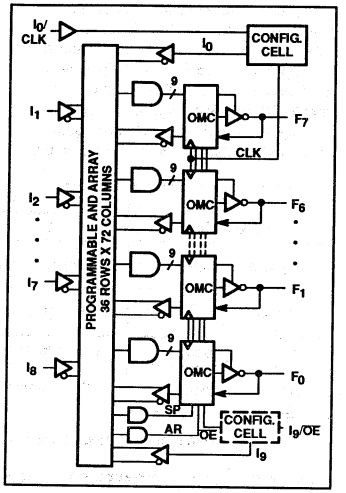
Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and OE functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
Denotes a programmable cell location.

PAL DEVICE TO PLC18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

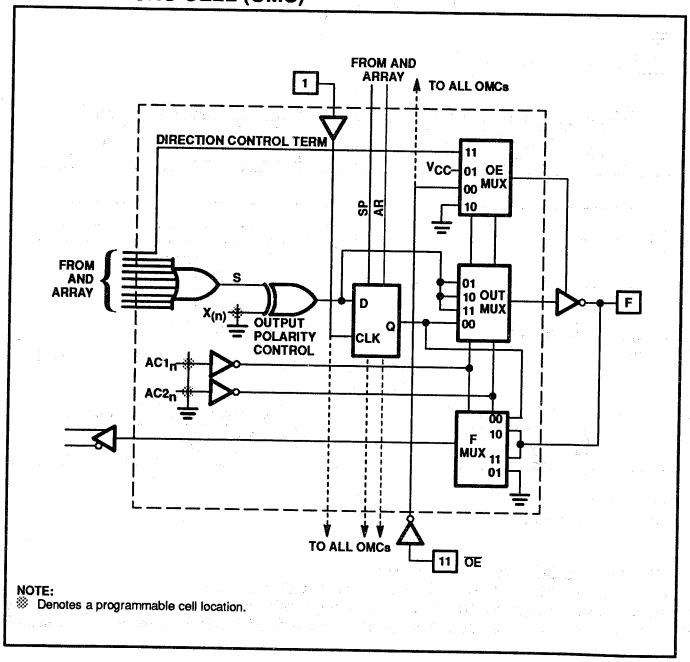
PIN NO.	PLC 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	I_9/$\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Atmel state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Atmel to functionally test the devices prior to shipment to the customer. Additionally, this allows Atmel to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

FUNCTIONAL DIAGRAM



OUTPUT MACRO CELL (OMC)



NOTE:
※ Denotes a programmable cell location.

THE OUTPUT MACRO CELL (OMC)

The PLC18V8Z series devices have 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The PLC18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

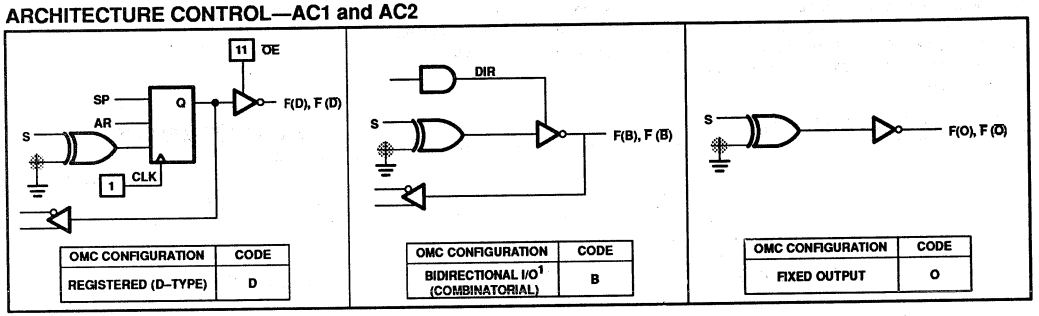
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

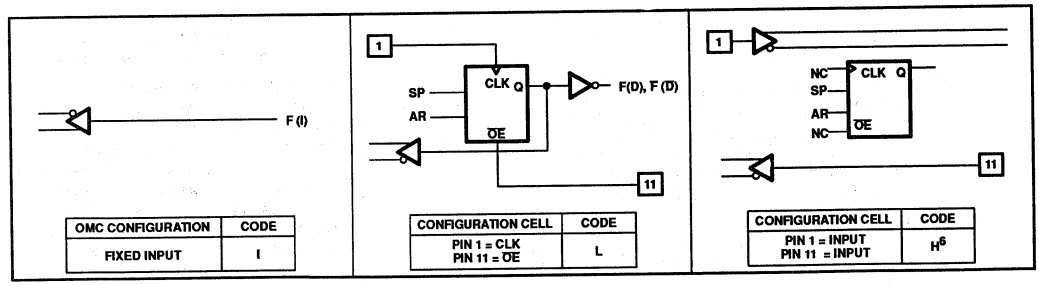
ARCHITECTURE CONTROL—AC1 and AC2



OMC CONFIGURATION	CODE
REGISTERED (D–TYPE)	D

OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B

OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I

CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L

CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H[6]

NOTE:
A factory shipped unprogrammed device is configured such that:
1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{CC}	Operating supply voltage	4.5 to 5.5 (Industrial) 4.75 to 5.25 (Commercial)	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	–40 to +85 (Industrial) 0 to +75 (Commercial)	°C
T_{stg}	Storage temperature range	–65 to +150	°C

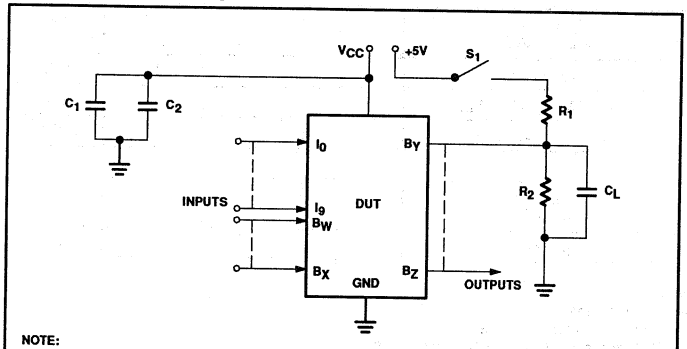
NOTE:

1. Stresses above those listed may cause malfuncion or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

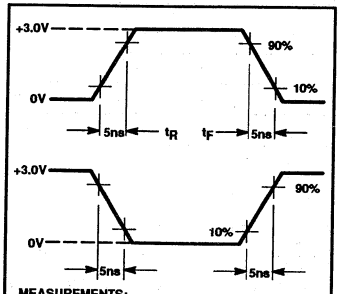
TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

8

DC ELECTRICAL CHARACTERISTICS

Commercial = 0°C ≤ T_{AMB} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V;
Industrial = –40°C ≤ T_{amb} ≤ +85°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 20µA V_{CC} = MIN, I_{OL} = 24mA			0.100 0.500	V V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –3.2mA V_{CC} = MIN, I_{OH} = –20µA	2.4 V_{CC} – 0.1V			V V
Input current						
I_{IL}	Low[7]	V_{IN} = GND			–10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi–Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 –10	µA µA
I_{OS}	Short-circuit[3]	V_{OUT} = GND			–130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = MAX, V_{IN} = 0 or V_{CC}[8]			100	µA
I_{CC}/f	V_{CC} supply current (Active)[4]	V_{CC} = MAX (CMOS inputs)[5, 6]			1.5	mA/MHz
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all outputs switching.
5. ΔI_{CC}/TTL input = 2mA.
6. ΔI_{CC} vs frequency (registered configuration) = 2mA/MHz.
7. I_{IL} for Pin 1 (I_0/CLK) is ± 10µA with V_{IN} = 0.4V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

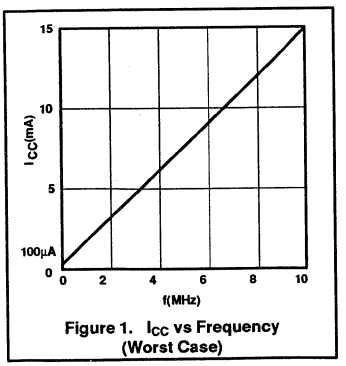


Figure 1. I_{CC} vs Frequency (Worst Case)

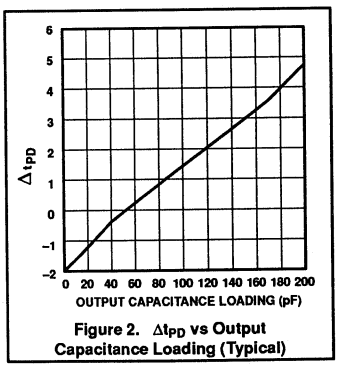


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

Commercial = $0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$;
Industrial = $-40°C \le T_{amb} \le +85°C$, $4.5V \le V_{CC} \le 5.5V$; $R_2 = 390\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]		PLC18V8Z35 (Commercial)		PLC18V8ZI (Industrial)		UNIT
				R_1 (Ω)	C_L (pF)	MIN	MAX	MIN	MAX	
Pulse width										
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	200	50	47		57		ns
t_{CKH}	Clock width High	CLK +	CLK –	200	50	20		25		ns
t_{CKL}	Clock width Low	CLK –	CLK +	200	50	20		25		ns
t_{ARW}	Async reset pulse width	I ±, F±	I ∓, F ∓			35		40		ns
Hold time										
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	25		30		ns
Propagation delay										
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		35		40	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		22		27	ns
t_{OE1}[3]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		35		40	ns
t_{OD1}[2]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		35		40	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	OE –	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		30	ns
t_{OE2}[3]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		25		30	ns
t_{ARD}	Async reset delay	I ±, F±	F +				35		40	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +			25		30		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +			25		30		ns
t_{PPR}	Power-up reset	V_{CC} +	F +				35		40	ns
Frequency of operation										
f_{MAX}	Maximum frequency	$1/(t_{IS} + t_{CKO})$		200	50		21		18	MHz

NOTES:

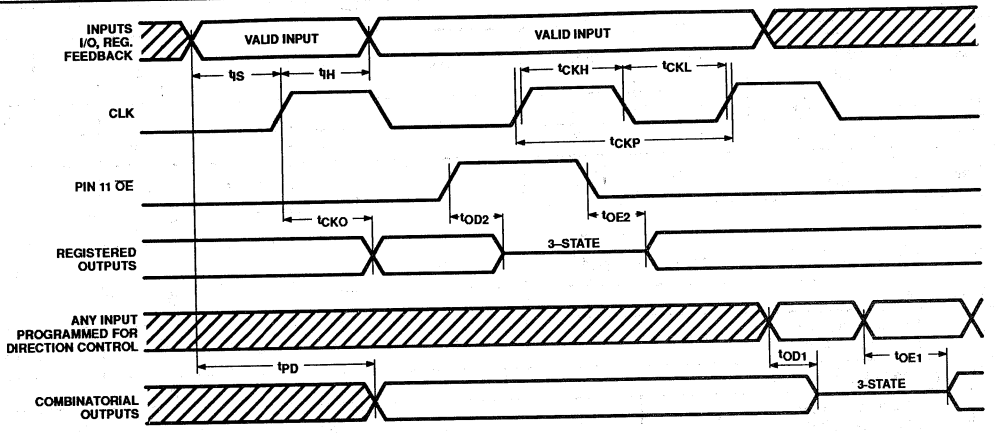
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

8

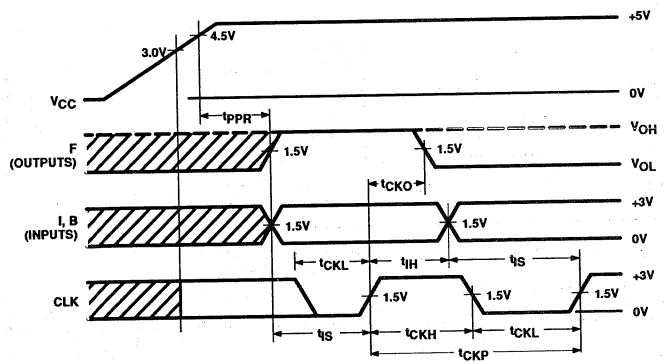
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC18V8Z. All internal registers will reset to Active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

TIMING DIAGRAMS



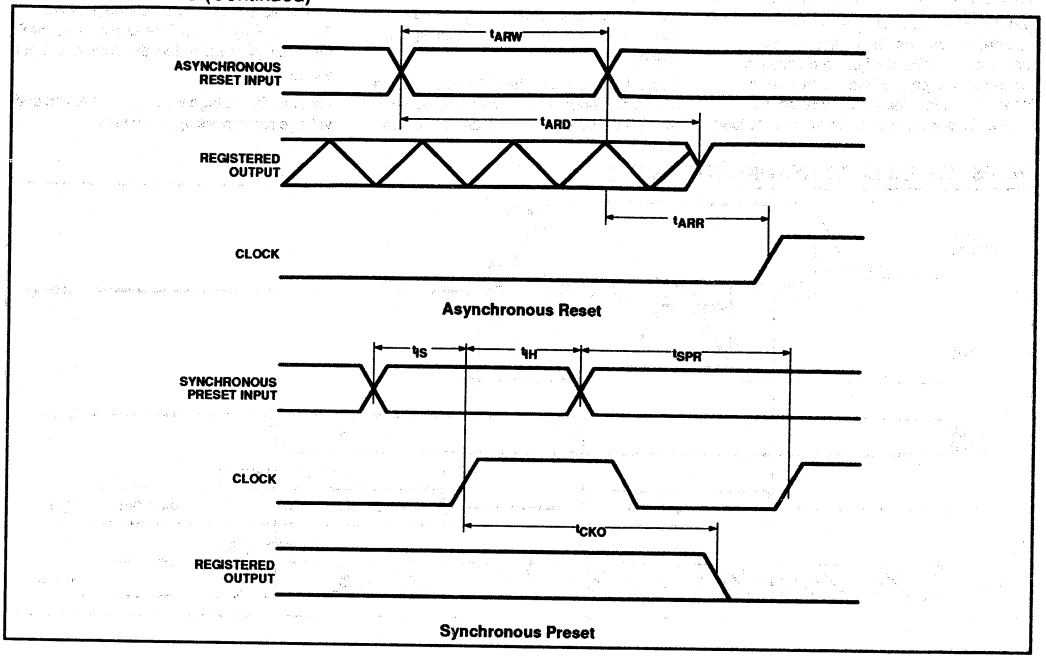
Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

TIMING DIAGRAMS (Continued)



8

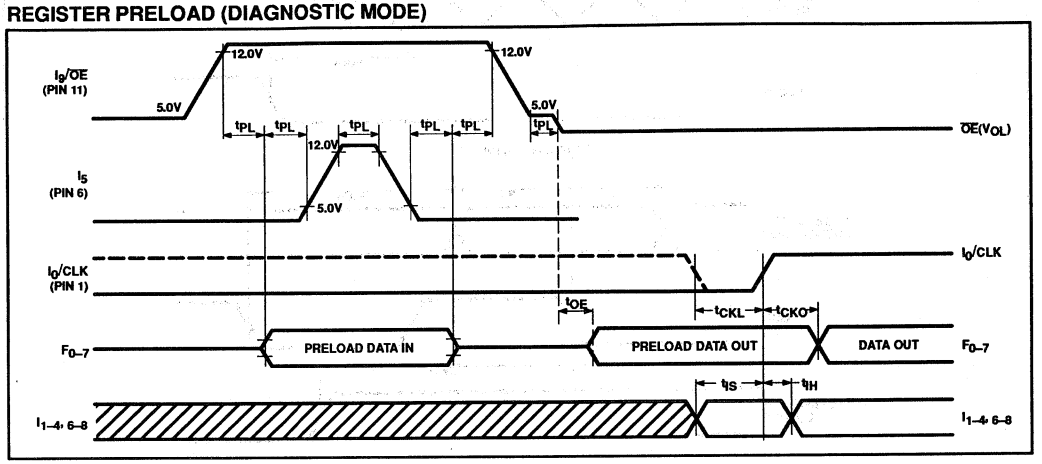
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10µsec.

REGISTER PRELOAD (DIAGNOSTIC MODE)



LOGIC PROGRAMMING

The PLC18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics AMAZE, SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLC18V8Z architecture.

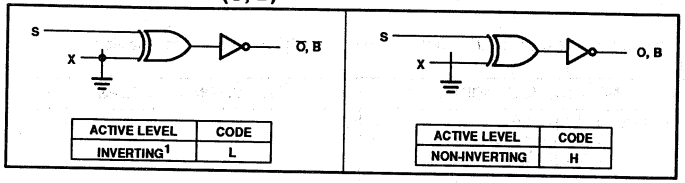
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by AMAZE and SLICE only. Both AMAZE and SLICE design packages are available, free of charge, to qualified users.

With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

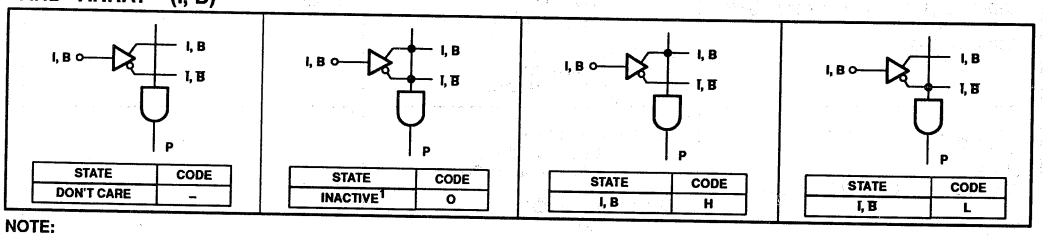
OUTPUT POLARITY – (O, B)



ACTIVE LEVEL	CODE
INVERTING[1]	L

ACTIVE LEVEL	CODE
NON-INVERTING	H

"AND" ARRAY – (I, B)



STATE	CODE
DON'T CARE	–

STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B	H

STATE	CODE
I, $\bar{B}$	L

NOTE:
1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

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ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical PLC18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

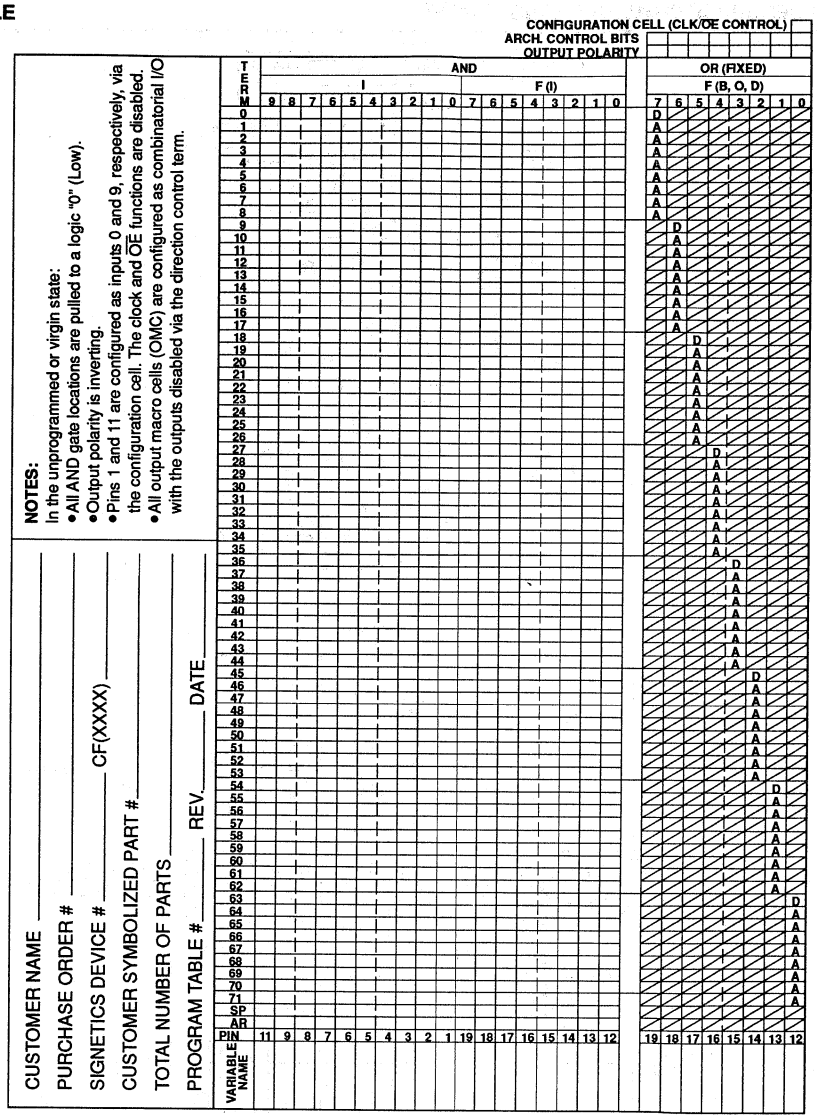
PROGRAMMING

The PLC18V8Z35/I is programmable on conventional programmers for 20-pin PAL devices. Refer to the following charts for qualified manufacturers of programmers and software tools:

PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073–9746 (800)247–5700	System 29B, LogicPak™ 303A–011A; V09 (DIL) 303A–011B; V04 (PLCC) UNISITE 40/48 V2.6 (DIL) Chipsite (PLCC) – V2.8 MODEL 60 360A001 (DIL) 360A006 (PLCC)	86/4F
STAG MICROSYSTEMS, INC. 1600 WYATT DRIVE SUITE 3 SANTA CLARA, CALIFORNIA 95054 (408)988–1118	ZL30/30A PROGRAMMER REV. 30A34 (DIL) 30A001 Adaptor (PLCC) PPZ PROGRAMMER TBA	12/205

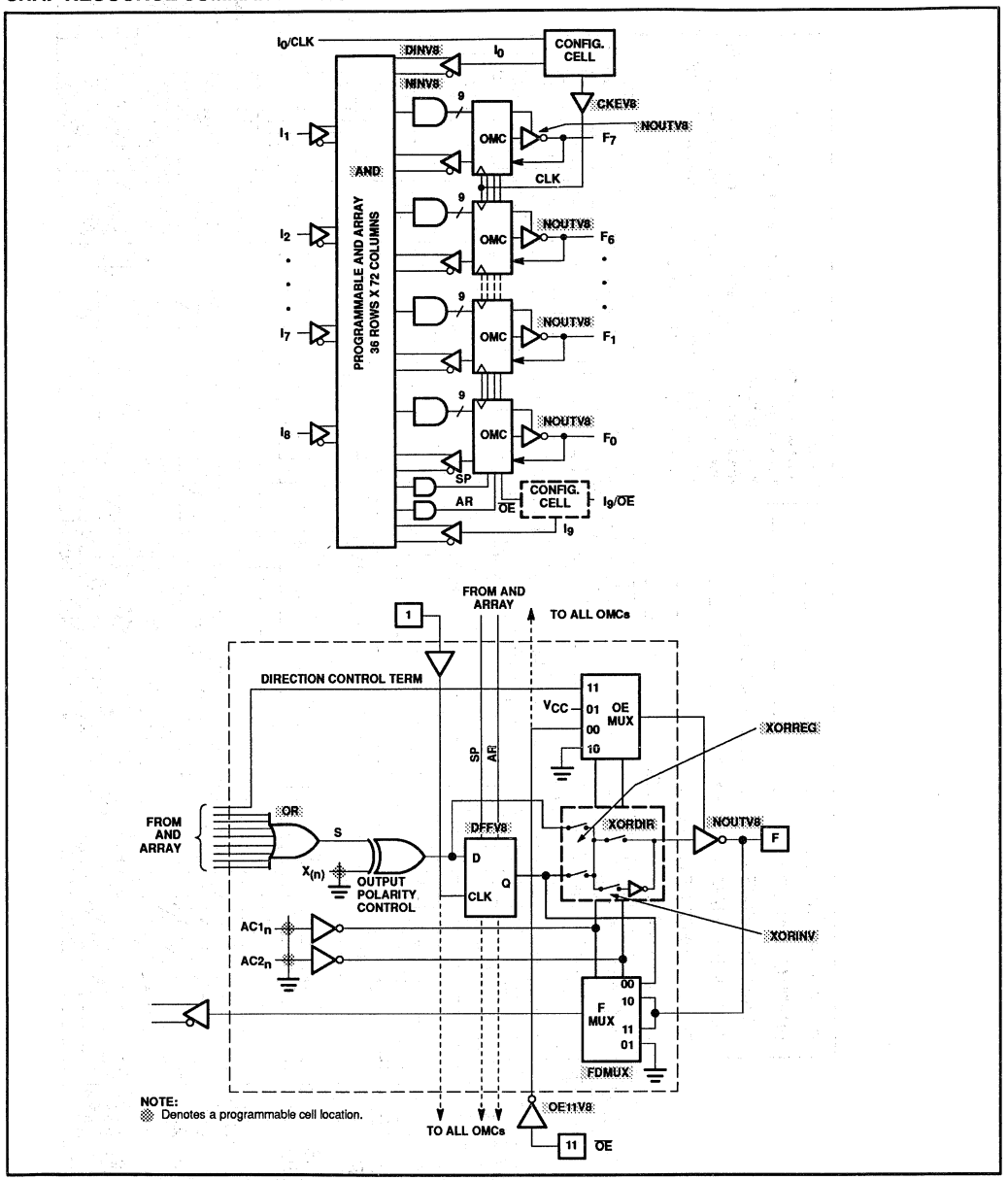
SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
SIGNETICS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088–3409 (408)991–2000	SNAP REV. 1.6 AND LATER SLICE REV. 1.0 AND LATER AMAZE SOFTWARE REV. 1.8 AND LATER
DATA I/O 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073–9746 (800)247–5700	ABEL™ SOFTWARE
LOGICAL DEVICES, INC. 1201 NORTHWEST 65TH PLACE FORT LAUDERDALE, FLORIDA 33309 (800)331–7766	CUPL™ SOFTWARE

PROGRAM TABLE



* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "–" IS NOT ALLOWED.

SNAP RESOURCE SUMMARY DESIGNATIONS



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
35	25	22	AT18V8Z-35DC AT18V8Z-35JC AT18V8Z-35PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
40	30	27	AT18V8Z-40DI AT18V8Z-40JI AT18V8Z-40PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)

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Package Type	
20DW3	20 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
20J	20 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
20P3	20 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)

Features

- **High Speed Programmable Logic Device**
  - **15 ns Max Propagation Delay**
  - **5V ±10% Operation**
- **Low Power CMOS Operation**

Speed	"L"	-15,-20	All
Temp	C/M	C/M	Others
Icc(mA)	12/15	90/100	55

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages**

High Speed UV Erasable Programmable Logic Device

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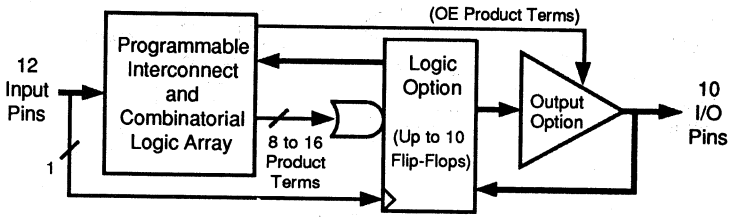
Logic Diagram



Description

The AT22V10 and AT22V10L are CMOS high performance Erasable Programmable Logic Devices (EPLDs). Speeds down to 15 ns and power dissipation as low as 12 mA are offered. All speed ranges are specified over the full 5V ±10% range. All pins offer a low ±10 µA leakage.

The AT22V10L provides the optimum low power CMOS EPLD solution, with low DC power (8mA typical) and full CMOS output levels. The AT22V10L significantly reduces total system power and enhances system reliability.

Full CMOS output levels help reduce power in many other system components.

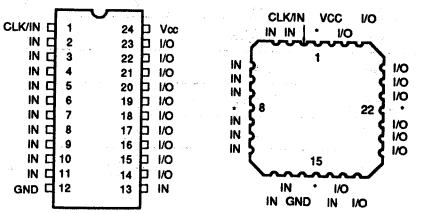
The AT22V10 and AT22V10L incorporate a variable product term architecture. Each output is allocated from 8 to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply



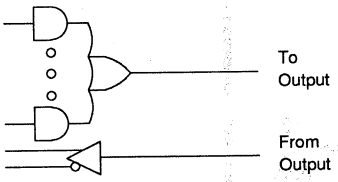
Absolute Maximum Ratings*

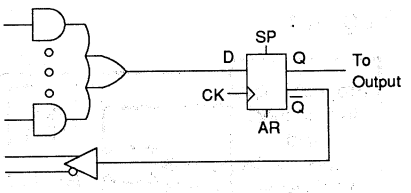
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W-sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

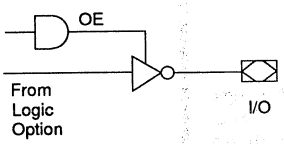
Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

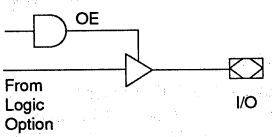
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22V10/L -15, -20, -25, -35	Industrial AT22V10/L -15, -20, -25, -35	Military AT22V10/L -15, -20, -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5V±10%	5V±10%	5V±10%

Operating Modes

Mode	24 DIP Pin / 28 JLCC Pin	1 / 2	5 / 6	8 / 10	13 / 16	I/O's	Vcc(24) / Vcc(28)
"EPLD"		X (1)	X	X	X	I/O	5V
Program		V_{PP}	X / V_H (2)	X	V_{PP}	D_{IN}	6V
PGM Verify		V_{PP}	X/V_H	X	V_{IL}	D_{OUT}	6V
PGM Inhibit		V_{PP}	X/V_H	X	V_{IH}	High Z	6V
Preload		X	X	V_H	X	D_{IN}	5V

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V				10	µA
I_{CC}	Power Supply Current	V_{CC}=MAX, V_{IN}=GND, Outputs Open	AT22V10-15,-20	Com.		90	mA
				Ind., Mil.		100	mA
			AT22V10-25,-35(2)			55	mA
			AT22V10L(2)	Com.		12	mA
				Ind., Mil.		15	mA
I_{CC2}	Clocked Power Supply Current	f=1MHz, V_{CC}=MAX, Outputs Open	AT22V10L(2)	Com.		15	mA
				Ind., Mil.		20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V				-90	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OL}=16mA	Com.,Ind.		0.5	V
			I_{OL}=12mA	Mil.		0.5	V
			I_{OL}=24mA	Com.		0.8	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH}=-100µA		V_{CC}-0.3		V
			I_{OH}=-4.0mA		2.4		V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. See I_{CC} vs. Frequency curves in the back of this data sheet.

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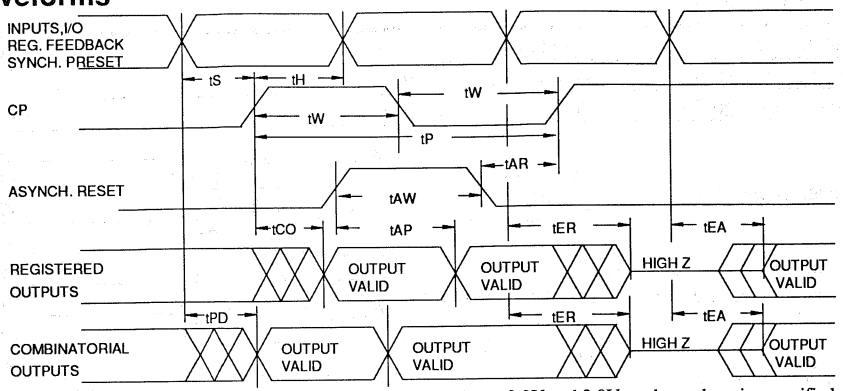
A.C. Characteristics, Commercial and Industrial

Symbol	Parameter	AT22V10-15			AT22V10/L-20			AT22V10/L-25			AT22V10/L-35			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	35	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	35	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	35	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	12	0	10	15	0	12	20	ns
t_S	Input or Feedback Setup Time	10	8		12	8		15	12		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback 1/(ts+tco)			50.0			41.6			33.3			25.0	MHz
	Internal Feedback 1/(ts + tcf)			80.0			50.0			40.0			28.5	MHz
	No Feedback 1/(tp)			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

A.C. Waveforms [1]

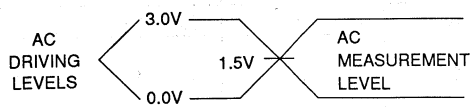


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics, Military

Symbol	Parameter	AT22V10-15			AT22V10/L-20			AT22V10/L-25			AT22V10/L-30			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	30	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	30	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	15	0	10	15	0	12	20	ns
t_{SF}	Feedback Setup Time	10	8		12	10		15	12		18	15		ns
t_S	Input Setup Time	10	8		17	14		18	15		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			31.2			30.3			25.0	MHz
	Internal Feedback $1/(t_S + t_{CF})$			80.0			50.0			40.0			30.0	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

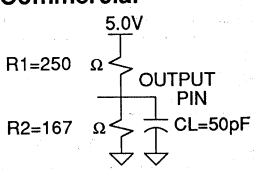
Input Test Waveforms and Measurement Levels



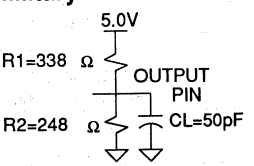
tR, tF < 5ns (10% to 90%)

Output Test Loads:

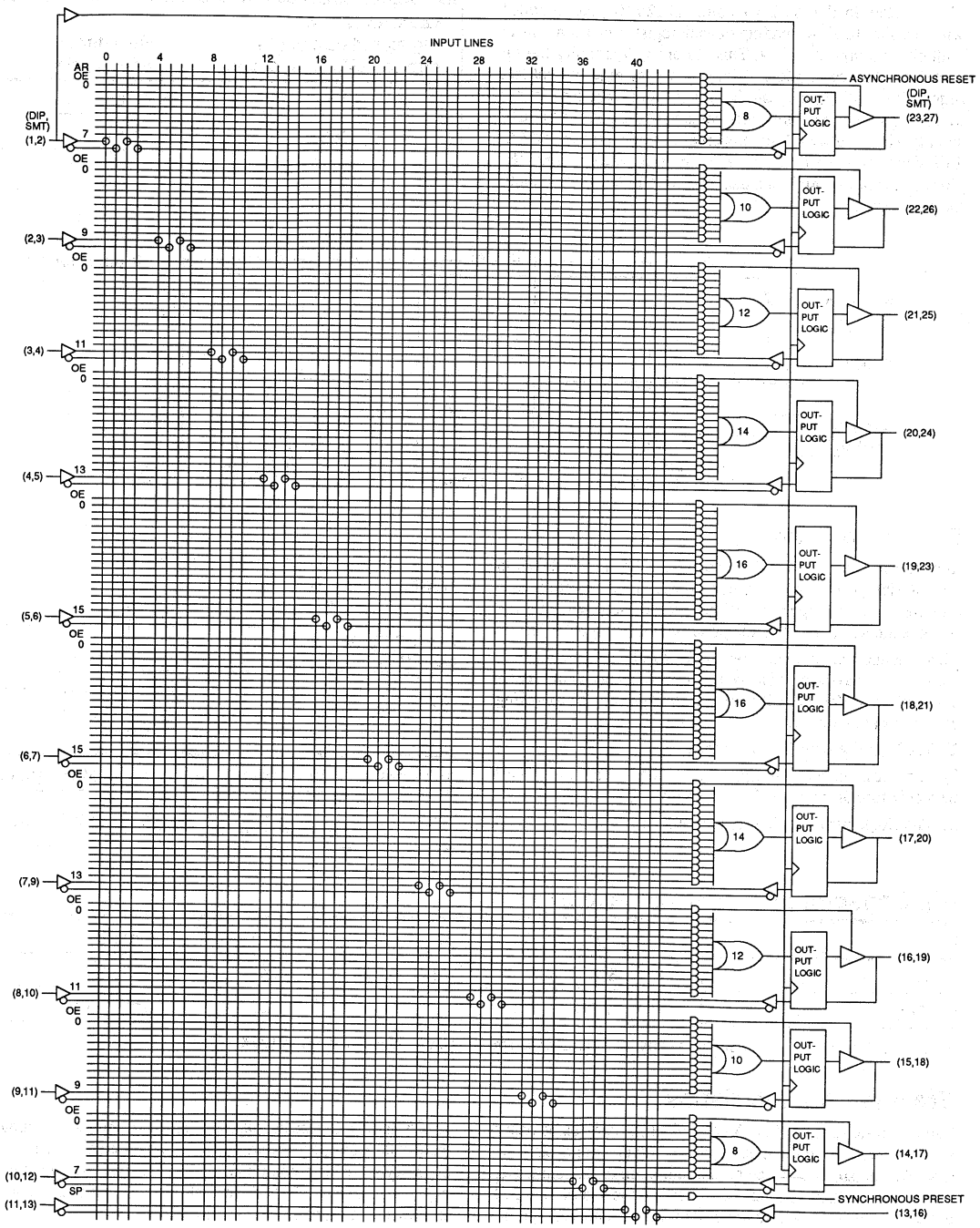
Commercial



Military



Functional Logic Diagram AT22V10/L



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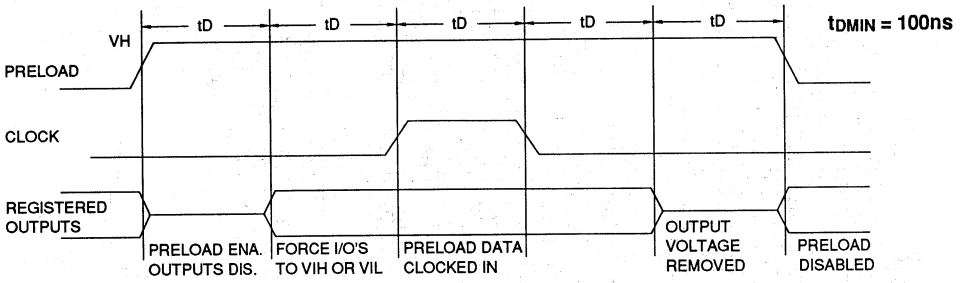
Preload of Registered Outputs

The registers in the AT22V10 and AT22V10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The PRELOAD state is entered by placing an 11V to 14V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the 10 registers.

Level forced on registered output pin during PRELOAD cycle.	Register state After Cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

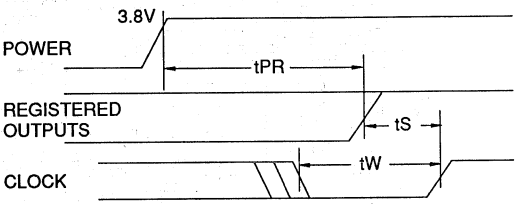
The registers in the AT22V10 and AT22V10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

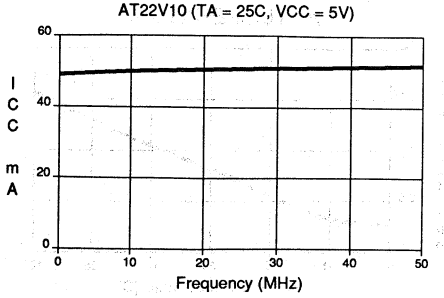
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10 or AT22V10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

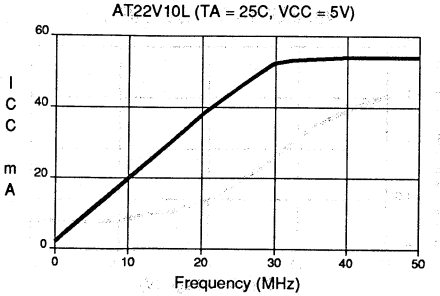
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10 (TA = 25C, VCC = 5V)

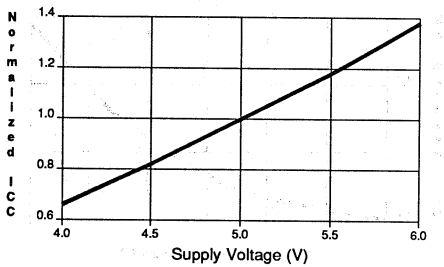


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10L (TA = 25C, VCC = 5V)

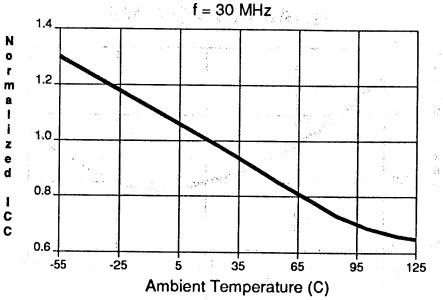


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

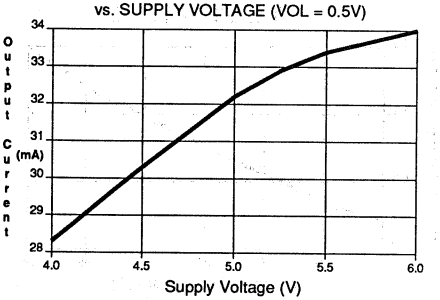


NORMALIZED ICC vs. AMBIENT TEMP.

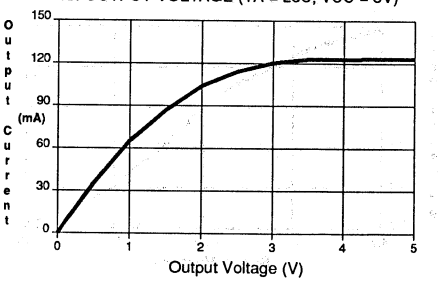
f = 30 MHz



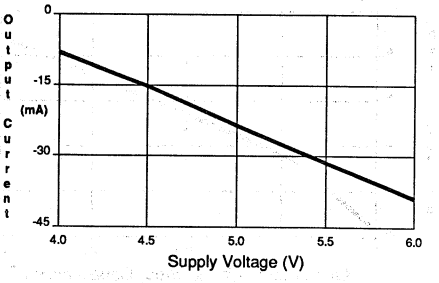
OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE (VOL = 0.5V)



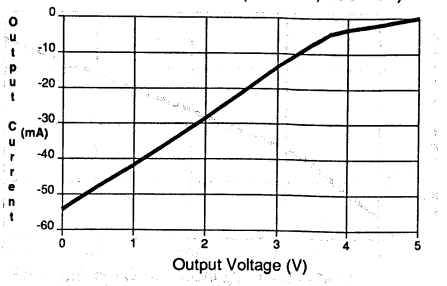
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE (VOH = 2.4V)



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



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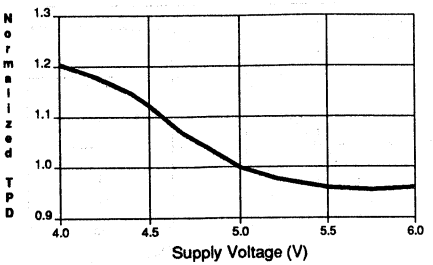
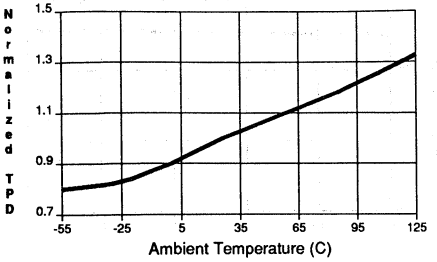
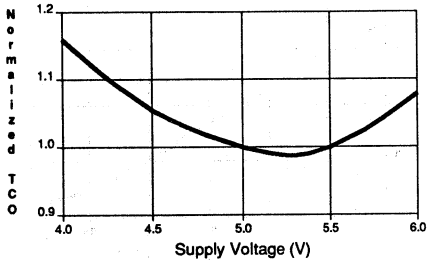
NORMALIZED TPD
vs. SUPPLY VOLTAGE



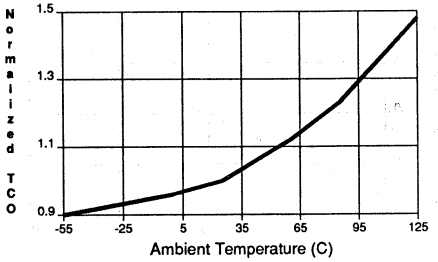
NORMALIZED TPD
vs. TEMPERATURE



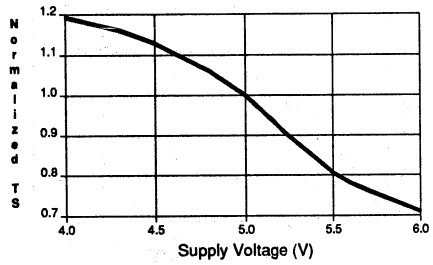
NORMALIZED TCO
vs. SUPPLY VOLTAGE



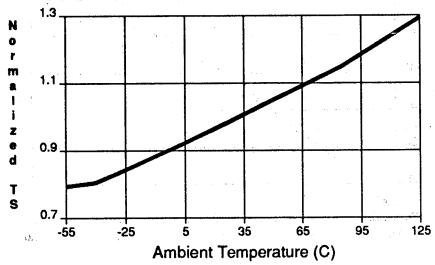
NORMALIZED TCO
vs. TEMPERATURE



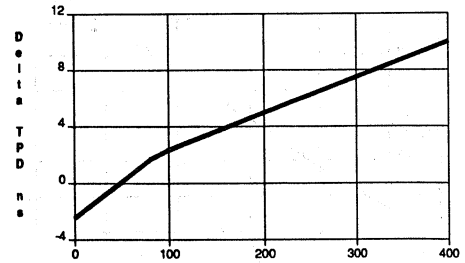
NORMALIZED TS
vs. SUPPLY VOLTAGE



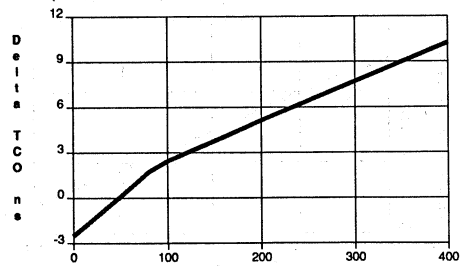
NORMALIZED TS
vs. TEMPERATURE



DELTA TPD vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	10	AT22V10-15DC AT22V10-15FC AT22V10-15GC AT22V10-15JC AT22V10-15KC AT22V10-15LC AT22V10-15NC AT22V10-15PC AT22V10-15YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-15DI AT22V10-15FI AT22V10-15GI AT22V10-15JI AT22V10-15KI AT22V10-15LI AT22V10-15NI AT22V10-15PI AT22V10-15YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			AT22V10-15DM AT22V10-15FM AT22V10-15GM AT22V10-15KM AT22V10-15LM AT22V10-15NM AT22V10-15YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10-15DM/883 AT22V10-15FM/883 AT22V10-15GM/883 AT22V10-15KM/883 AT22V10-15LM/883 AT22V10-15NM/883 AT22V10-15YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	12	15	AT22V10-20DC AT22V10-20FC AT22V10-20GC AT22V10-20JC AT22V10-20KC AT22V10-20LC AT22V10-20NC AT22V10-20PC AT22V10-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-20DI AT22V10-20FI AT22V10-20GI AT22V10-20JI AT22V10-20KI AT22V10-20LI AT22V10-20NI AT22V10-20PI AT22V10-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	17	15	AT22V10-20DM AT22V10-20FM AT22V10-20GM AT22V10-20KM AT22V10-20LM AT22V10-20NM AT22V10-20YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10-20DM/883 AT22V10-20FM/883 AT22V10-20GM/883 AT22V10-20KM/883 AT22V10-20LM/883 AT22V10-20NM/883 AT22V10-20YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10-25DC AT22V10-25FC AT22V10-25GC AT22V10-25JC AT22V10-25KC AT22V10-25LC AT22V10-25NC AT22V10-25PC AT22V10-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-25DI AT22V10-25FI AT22V10-25GI AT22V10-25JI AT22V10-25KI AT22V10-25LI AT22V10-25NI AT22V10-25PI AT22V10-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
25	18	15	AT22V10-25DM AT22V10-25FM AT22V10-25GM AT22V10-25KM AT22V10-25LM AT22V10-25NM AT22V10-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10-25DM/883 AT22V10-25FM/883 AT22V10-25GM/883 AT22V10-25KM/883 AT22V10-25LM/883 AT22V10-25NM/883 AT22V10-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
30	20	20	AT22V10-30DM AT22V10-30FM AT22V10-30GM AT22V10-30KM AT22V10-30LM AT22V10-30NM AT22V10-30YM	24DW3 24C 28D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10-30DM/883 AT22V10-30FM/883 AT22V10-30GM/883 AT22V10-30KM/883 AT22V10-30LM/883 AT22V10-30NM/883 AT22V10-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	25	25	AT22V10-35DC AT22V10-35FC AT22V10-35GC AT22V10-35JC AT22V10-35KC AT22V10-35LC AT22V10-35NC AT22V10-35PC AT22V10-35YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10-35DI AT22V10-35FI AT22V10-35GI AT22V10-35JI AT22V10-35KI AT22V10-35LI AT22V10-35NI AT22V10-35PI AT22V10-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	17	15	5962-87539 04 LX 5962-87539 04 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-87539 01 KX 5962-87539 01 LX 5962-87539 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-87539 02 KX 5962-87539 02 LX 5962-87539 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-87539 03 KX 5962-87539 03 LX 5962-87539 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-88670 04 KX 5962-88670 04 LX 5962-88670 04 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	18	15	5962-88670 01 KX 5962-88670 01 LX 5962-88670 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-88670 02 KX 5962-88670 02 LX 5962-88670 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-88670 03 KX 5962-88670 03 LX 5962-88670 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	12	15	AT22V10L-20DC AT22V10L-20FC AT22V10L-20GC AT22V10L-20JC AT22V10L-20KC AT22V10L-20LC AT22V10L-20NC AT22V10L-20PC AT22V10L-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10L-20DI AT22V10L-20FI AT22V10L-20GI AT22V10L-20JI AT22V10L-20KI AT22V10L-20LI AT22V10L-20NI AT22V10L-20PI AT22V10L-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
20	17	15	AT22V10L-20DM AT22V10L-20FM AT22V10L-20GM AT22V10L-20KM AT22V10L-20LM AT22V10L-20NM AT22V10L-20YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10L-20DM/883 AT22V10L-20FM/883 AT22V10L-20GM/883 AT22V10L-20KM/883 AT22V10L-20LM/883 AT22V10L-20NM/883 AT22V10L-20YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10L-25DC AT22V10L-25FC AT22V10L-25GC AT22V10L-25JC AT22V10L-25KC AT22V10L-25LC AT22V10L-25NC AT22V10L-25PC AT22V10L-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			AT22V10L-25DI AT22V10L-25FI AT22V10L-25GI AT22V10L-25JI AT22V10L-25KI AT22V10L-25LI AT22V10L-25NI AT22V10L-25PI AT22V10L-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)

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Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	18	15	AT22V10L-25DM AT22V10L-25FM AT22V10L-25GM AT22V10L-25KM AT22V10L-25LM AT22V10L-25NM AT22V10L-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10L-25DM/883 AT22V10L-25FM/883 AT22V10L-25GM/883 AT22V10L-25KM/883 AT22V10L-25LM/883 AT22V10L-25NM/883 AT22V10L-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	AT22V10L-30DM AT22V10L-30FM AT22V10L-30GM AT22V10L-30KM AT22V10L-30LM AT22V10L-30NM AT22V10L-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			AT22V10L-30DM/883 AT22V10L-30FM/883 AT22V10L-30GM/883 AT22V10L-30KM/883 AT22V10L-30LM/883 AT22V10L-30NM/883 AT22V10L-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	25	25	AT22V10L-35DC AT22V10L-35FC AT22V10L-35GC AT22V10L-35JC AT22V10L-35KC AT22V10L-35LC AT22V10L-35NC AT22V10L-35PC AT22V10L-35YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
35	25	15	AT22V10L-35DI AT22V10L-35FI AT22V10L-35GI AT22V10L-35JI AT22V10L-35KI AT22V10L-35LI AT22V10L-35NI AT22V10L-35PI AT22V10L-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	17	15	5962-88724 04 KX 5962-88724 04 LX 5962-88724 04 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88724 01 KX 5962-88724 01 LX 5962-88724 01 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-88724 02 KX 5962-88724 02 LX 5962-88724 02 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-88724 03 KX 5962-88724 03 LX 5962-88724 03 3X	24CW 24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-89755 01 KX 5962-89755 01 LX 5962-89755 01 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	20	20	5962-89755 02 KX 5962-89755 02 LX 5962-89755 02 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	30	25	5962-89755 03 KX 5962-89755 03 LX 5962-89755 03 3X	24C 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

8

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

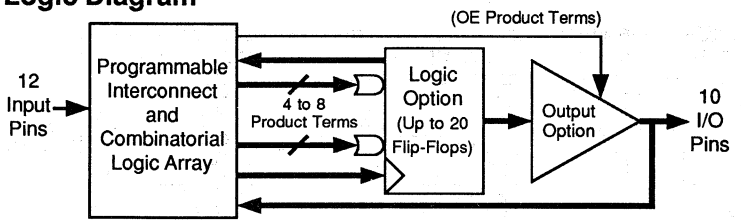
Features

- **Third Generation Programmable Logic Structure**
  High Density Replacement for Discrete Logic
- **High Speed - Plus a New Low Power Version**
- **Increased Logic Flexibility**
  42 Inputs and 20 SUM terms
- **Flexible Output Logic**
  20 Flip-Flops - 10 Extra
  All Can Be Individually Buried or 10 Output Directly
  Each has Individual Asynchronous Reset or Clock Terms
- **Multiple Feedback Paths Provide for Buried State Machines**
  and I/O Bus Compatibility
- **Proven and Reliable High Speed CMOS EPROM Process**
  2000V ESD Protection
  200 mA Latchup Immunity
- **Reprogrammable - Tested 100% for Programmability**
- **24 pin, 300 mil Dual-In-line and 28 Lead Surface Mount Packages**

High Density UV Erasable Programmable Logic Device

8

Logic Diagram



Description

The ATV750/L is 100% more powerful than most other programmable logic devices in 24 pin packages. Increased Product terms, SUM Terms, and Flip-Flops translate into more usable gates.

Each of the ATV750's 22 logic pins can be used as an input. Ten of these can be used as input, output, or bi-directional I/O pins. All 20 Flip-Flops can be fed back into the array independently. This flexibility allows burying all of the SUM terms and Flip-Flops.

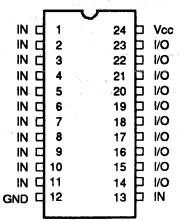
There are 171 Product Terms available. A variable format is used to assign between 4 and 8 Product Terms per Sum Term. There are 2 Sum Terms per output, providing added flexibility. Much more logic can be replaced by this one 24 pin device.

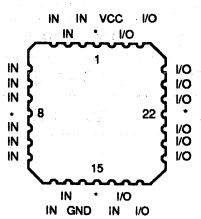
The ATV750/L has more flip-flops available than other EPLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. One product term provides a global synchronous Preset. Register Preload simplifies testing. The device has an internal power up clear function.

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply





Absolute Maximum Ratings*

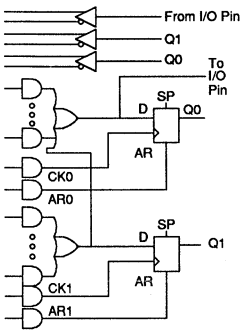
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W-sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

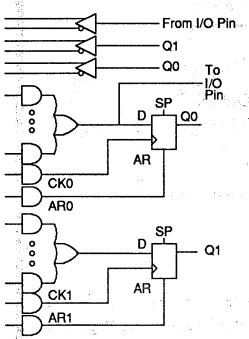
Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Logic Options

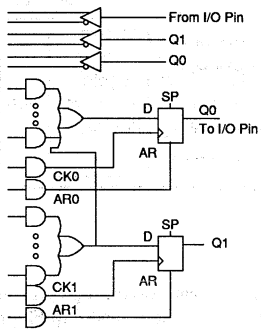
Combined Terms



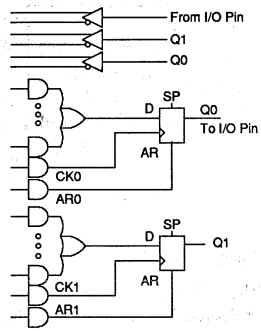
Separate Terms



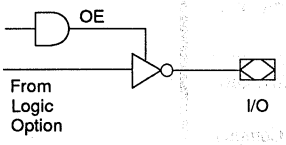
Combined Terms

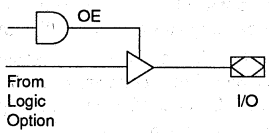


Separate Terms



Output Options





D.C. and A.C. Operating Conditions

		ATV750-20	ATV750/L-25	ATV750/L-30	ATV750/L-35	ATV750/L-40
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V				10	µA
I_{CC}	Power Supply Current	VCC=MAX, V_{IN}=GND, Outputs Open	ATV750	Com.		120	mA
				Ind.,Mil.		140	mA
			ATV750L	Com.		12	mA
				Ind.,Mil.		15	mA
I_{CC2} (2)	Clocked Power Supply Current	f=1MHz, VCC=MAX, Outputs Open	ATV750L	Com.		15	mA
				Ind.,Mil.		20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V				-90	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OL}=12mA Com.,Ind.			0.5	V
			I_{OL}=8mA Mil.			0.5	V
			I_{OL}=24mA, Com.			1.0	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH}=-100µA		V_{CC}-0.3		V
			I_{OH}=-4.0mA		2.4		V

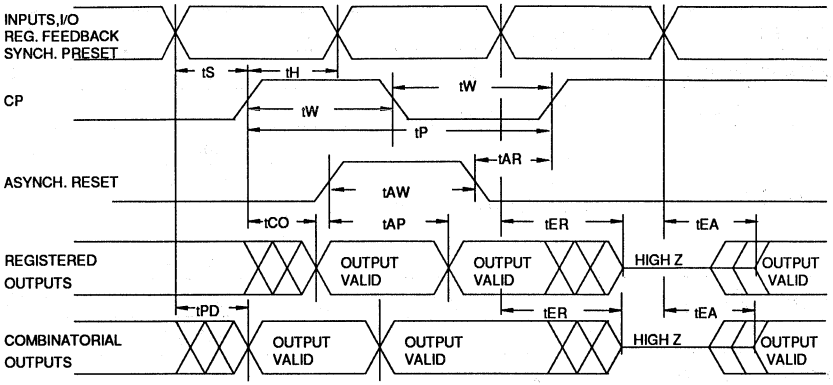
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Outputs not loaded.

Operating Modes

Mode	24 DIP Pin	1	5	8	11	13	I/O's	Vcc(24)
	28 JLCC Pin	2	6	10	13	16	I/O's	Vcc(28)
"EPLD"		X (1)	X	X	X	X	I/O	5V
Program		V_{PP}	X/V_H (2)	X	X/V_H	V_{PP}	D_{IN}	6V
PGM Verify		V_{PP}	X/V_H	X	X/V_H	V_{IL}	D_{OUT}	5V
PGM Inhibit		V_{PP}	X/V_H	X	X/V_H	V_{IH}	High Z	5-6V
Preload #1		X	X	V_H	X	V_{IL}	D_{IN}	5V
Preload #2		X	X	V_H	X	V_{IH}	D_{IN}	5V

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics

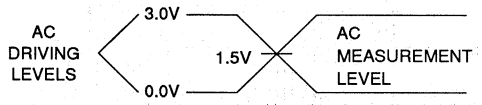
Symbol	Parameter	ATV750-30 Min	ATV750-30 Max	ATV750-35 Min	ATV750-35 Max	ATV750-40 Min	ATV750-40 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40	ns
t_{EA}	Input to Output Enable		30		35		40	ns
t_{ER}	Input to Output Disable		30		35		40	ns
t_{CO}	Clock to Output	5	25	10	30	10	35	ns
t_{CF}	Clock to Feedback	5	10	10	12	10	15	ns
t_S	Input Setup Time	15		18		20		ns
t_H	Hold Time	5		10		15		ns
t_P	Clock Period	25		30		35		ns
t_W	Clock Width	12		15		17		ns
F_{MAX}	Maximum Frequency		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	30		35		40		ns
t_{AR}	Asynchronous Reset Recovery Time	30		35		40		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40	ns
t_{SP}	Setup Time, Synchronous Preset	15		18		20		ns

A.C. Characteristics

Symbol	Parameter	ATV750-20 Min	ATV750-20 Max	ATV750/L-25 Min	ATV750/L-25 Max	ATV750L-30 Min	ATV750L-30 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		20		25		30	ns
t_{EA}	Input to Output Enable		20		25		30	ns
t_{ER}	Input to Output Disable		20		25		30	ns
t_{CO}	Clock to Output		20		22	5	25	ns
t_{CF}	Clock to Feedback	5	10	5	10	5	10	ns
t_S	Input Setup Time	10		12		15		ns
t_{SF}	Feedback Setup Time	5		7		15		ns
t_H	Hold Time	5		5		5		ns
t_P	Clock Period	18		22		25		ns
t_W	Clock Width	8		10		12		ns
F_{MAX}	Maximum Frequency		55		45		40	MHz
t_{AW}	Asynchronous Reset Width	15		20		30		ns
t_{AR}	Asynchronous Reset Recovery Time	15		20		30		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		20		25		30	ns
t_{SP}	Setup Time, Synchronous Preset	12		15		15		ns

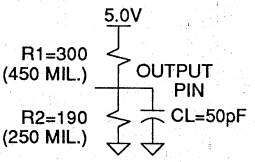
8

Input Test Waveforms and Measurement Levels

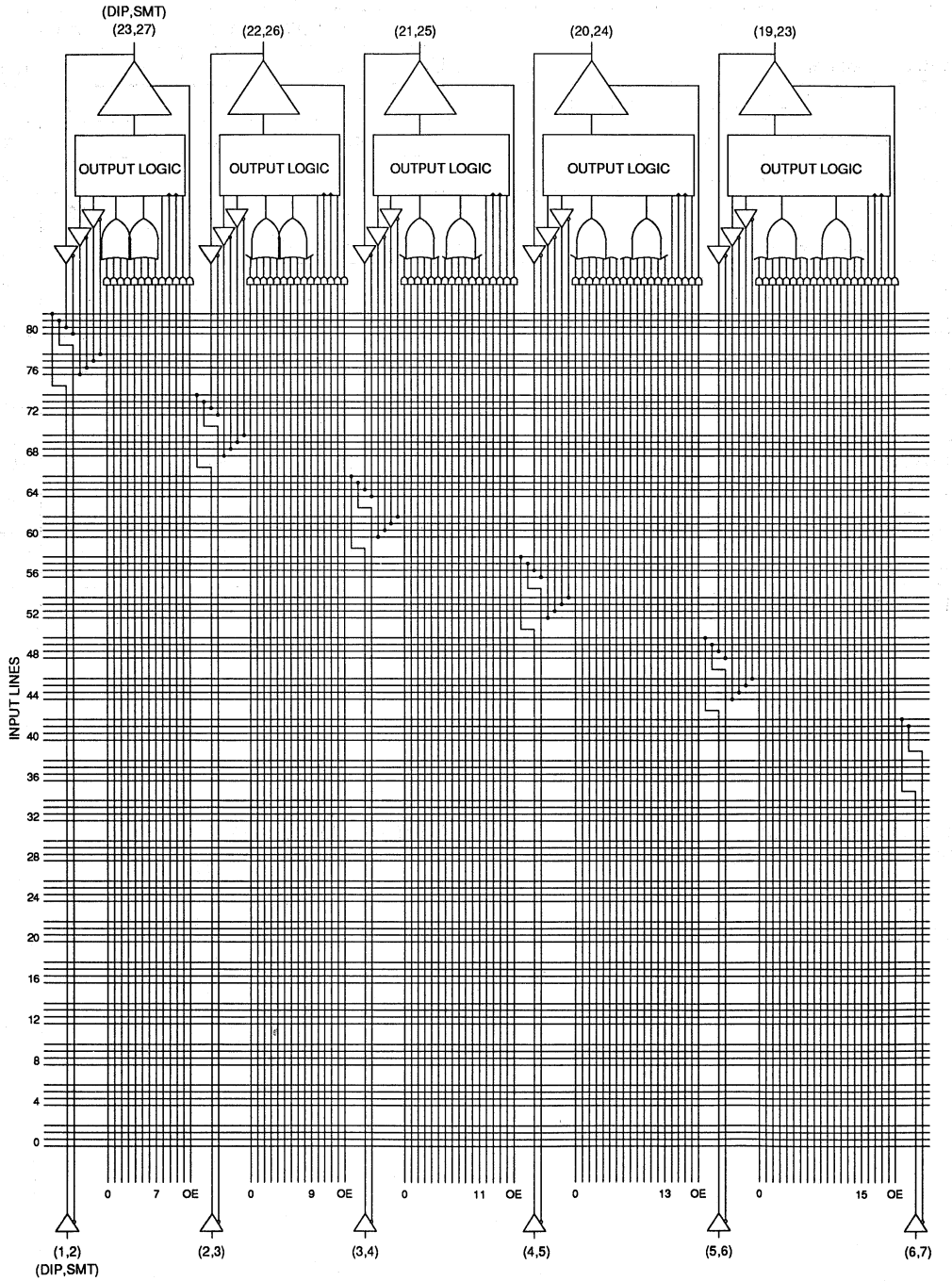


tR, tF < 5ns (10% to 90%)

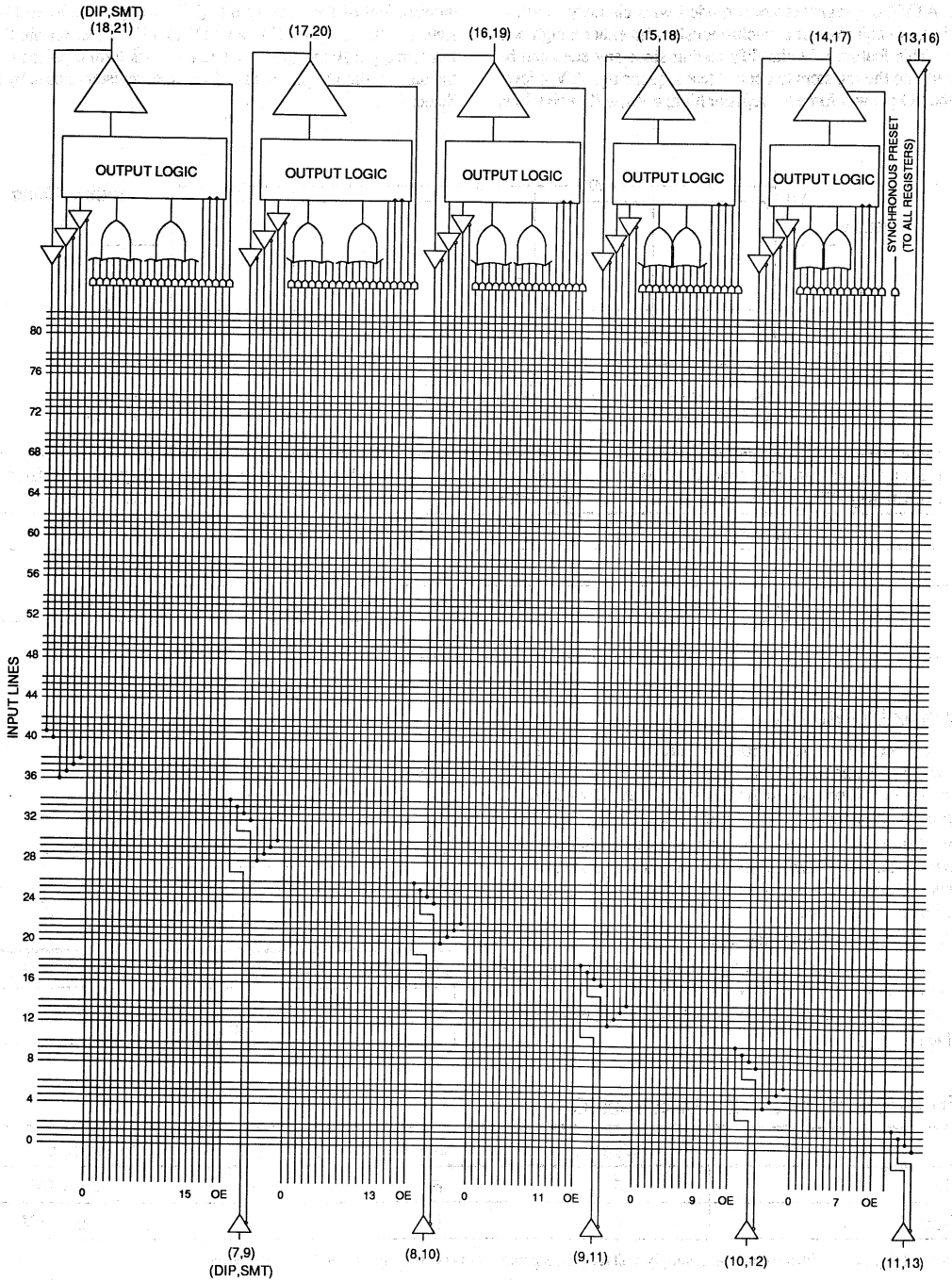
Output Test Load



Functional Logic Diagram ATV750, Upper Half



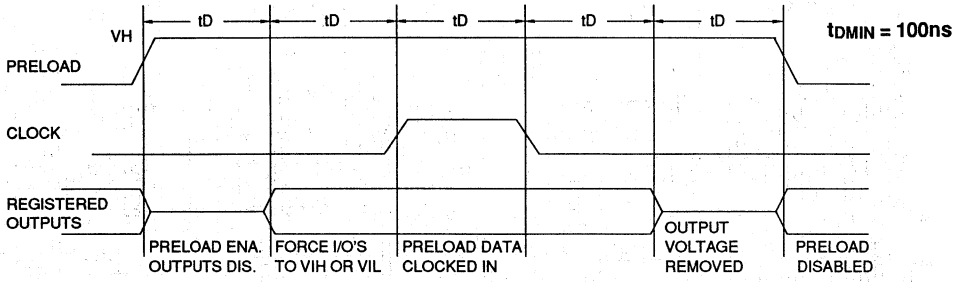
Functional Logic Diagram ATV750, Lower Half



8

Preload of Registered Outputs

The ATV750's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (S0) setting. The PRELOAD state is entered by placing an 11V to 14V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock term is pulsed high, the data on the I/O pin is placed into the register chosen by the Select Pin.



Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #1 state after cycle	Register #2 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power Up Reset

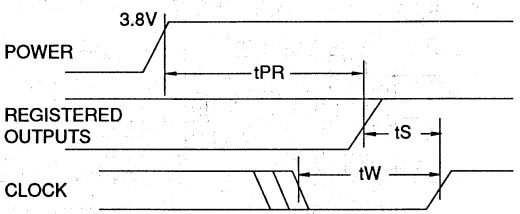
The registers in the ATV750/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Using The ATV750's Many Advanced Features

The ATV750's flexibility puts more usable gates in 24 pins than other EPLDs. The ATV750/L starts with an architecture similar to the popular AT22V10, and adds several features:

- Asynchronous Clocks -
  Each of the Flip-Flops in the ATV750/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV750/L clock period matches that of similar synchronous devices.
- A Full Bank of 10 More Registers -
  The ATV750/L provides two Flip-Flops for each Output Macrocell - a total of 20. Each register has its own clock and reset product terms, as well as its own SUM term.
- Independent I/O Pin and Feedback Paths -
  Each I/O pin on the ATV750/L has a dedicated input path. Each of the 20 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.
- Combinable Sum Terms -
  Each Output Macrocell's 2 SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 16 product terms per Output or Flip-Flop. This architecture increases the number of usable gates available.

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV750/L is available from the following sources:

Data I/O / Futurenet Corp.	- ABEL 2.1, 3.0, and above
Logical Devices	- CUPL 2.15B, and above

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750/L. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 Flip-Flops. Both Master and Slave halves of the Flip-Flops are reset when the input signals received combine so as to force the internal resets high.

8

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750/L fuse patterns. Once programmed, the output buffers will remain in a high impedance state during verify.

The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

The entire memory array of an ATV750/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

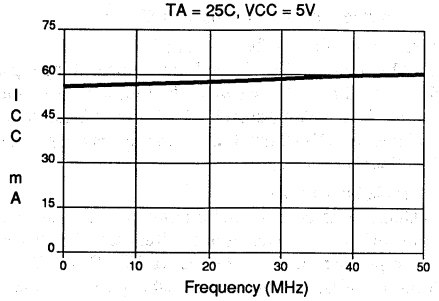
Atmel CMOS EPLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.5 micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64k to 1 megabit devices.

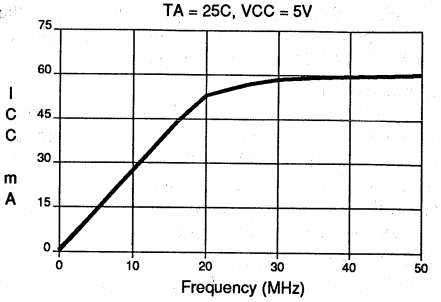
V750 ICC vs FREQUENCY

TA = 25C, VCC = 5V



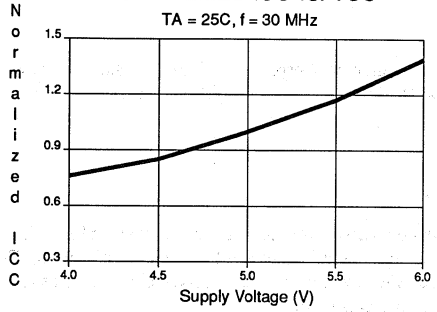
V750L ICC vs FREQUENCY

TA = 25C, VCC = 5V



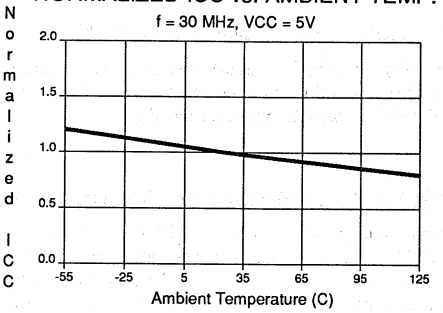
NORMALIZED ICC vs. VCC

TA = 25C, f = 30 MHz



NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz, VCC = 5V



Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	18	55	ATV750-20DC ATV750-20FC ATV750-20GC ATV750-20JC ATV750-20KC ATV750-20LC ATV750-20NC ATV750-20PC ATV750-20YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-20DI ATV750-20FI ATV750-20GI ATV750-20JI ATV750-20KI ATV750-20LI ATV750-20NI ATV750-20PI ATV750-20YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-20DM ATV750-20FM ATV750-20GM ATV750-20KM ATV750-20LM ATV750-20NM ATV750-20YM	24DW3 24C 28D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-20DM/883 ATV750-20FM/883 ATV750-20GM/883 ATV750-20KM/883 ATV750-20LM/883 ATV750-20NM/883 ATV750-20YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	ATV750-25DC ATV750-25FC ATV750-25GC ATV750-25JC ATV750-25KC ATV750-25LC ATV750-25NC ATV750-25PC ATV750-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-25DI ATV750-25FI ATV750-25GI ATV750-25JI ATV750-25KI ATV750-25LI ATV750-25NI ATV750-25PI ATV750-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)

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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750-25DM ATV750-25FM ATV750-25GM ATV750-25KM ATV750-25LM ATV750-25NM ATV750-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-25DM/883 ATV750-25FM/883 ATV750-25GM/883 ATV750-25KM/883 ATV750-25LM/883 ATV750-25NM/883 ATV750-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	25	40	ATV750-30DC ATV750-30FC ATV750-30GC ATV750-30JC ATV750-30KC ATV750-30LC ATV750-30NC ATV750-30PC ATV750-30YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-30DI ATV750-30FI ATV750-30GI ATV750-30JI ATV750-30KI ATV750-30LI ATV750-30NI ATV750-30PI ATV750-30YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-30DM ATV750-30FM ATV750-30GM ATV750-30KM ATV750-30LM ATV750-30NM ATV750-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-30DM/883 ATV750-30FM/883 ATV750-30GM/883 ATV750-30KM/883 ATV750-30LM/883 ATV750-30NM/883 ATV750-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
35	30	33	ATV750-35DC ATV750-35FC ATV750-35GC ATV750-35JC ATV750-35KC ATV750-35LC ATV750-35NC ATV750-35PC ATV750-35YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Commercial (0°C to 70°C)
			ATV750-35DI ATV750-35FI ATV750-35GI ATV750-35JI ATV750-35KI ATV750-35LI ATV750-35NI ATV750-35PI ATV750-35YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-35DM ATV750-35FM ATV750-35GM ATV750-35KM ATV750-35LM ATV750-35NM ATV750-35YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750-35DM/883 ATV750-35FM/883 ATV750-35GM/883 ATV750-35KM/883 ATV750-35LM/883 ATV750-35NM/883 ATV750-35YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	35	28	ATV750-40DI ATV750-40FI ATV750-40GI ATV750-40JI ATV750-40KI ATV750-40LI ATV750-40NI ATV750-40PI ATV750-40YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750-40DM ATV750-40FM ATV750-40GM ATV750-40KM ATV750-40LM ATV750-40NM ATV750-40YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)

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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
40	35	28	ATV750-40DM/883 ATV750-40FM/883 ATV750-40GM/883 ATV750-40KM/883 ATV750-40LM/883 ATV750-40NM/883 ATV750-40YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	30	33	5962-88726 02 LX 5962-88726 02 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
40	35	28	5962-88726 01 LX 5962-88726 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750L-25DC ATV750L-25FC ATV750L-25GC ATV750L-25JC ATV750L-25KC ATV750L-25LC ATV750L-25NC ATV750L-25PC ATV750L-25YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24P3	Commercial (0°C to 70°C)
			ATV750L-25DI ATV750L-25FI ATV750L-25GI ATV750L-25JI ATV750L-25KI ATV750L-25LI ATV750L-25NI ATV750L-25PI ATV750L-25YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)
			ATV750L-25DM ATV750L-25FM ATV750L-25GM ATV750L-25KM ATV750L-25LM ATV750L-25NM ATV750L-25YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750L-25DM/883 ATV750L-25FM/883 ATV750L-25GM/883 ATV750L-25KM/883 ATV750L-25LM/883 ATV750L-25NM/883 ATV750L-25YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	25	40	ATV750L-30DC ATV750L-30FC ATV750L-30GC ATV750L-30JC ATV750L-30KC ATV750L-30LC ATV750L-30NC ATV750L-30PC ATV750L-30YC	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24P3	Commercial (0°C to 70°C)
			ATV750L-30DI ATV750L-30FI ATV750L-30GI ATV750L-30JI ATV750L-30KI ATV750L-30LI ATV750L-30NI ATV750L-30PI ATV750L-30YI	24DW3 24C 24D3 28J 28KW 28LW 28L 24P3 24CW	Industrial (-40°C to 85°C)

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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	25	40	ATV750L-30DM ATV750L-30FM ATV750L-30GM ATV750L-30KM ATV750L-30LM ATV750L-30NM ATV750L-30YM	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military (-55°C to 125°C)
			ATV750L-30DM/883 ATV750L-30FM/883 ATV750L-30GM/883 ATV750L-30KM/883 ATV750L-30LM/883 ATV750L-30NM/883 ATV750L-30YM/883	24DW3 24C 24D3 28KW 28LW 28L 24CW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24C	24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28KW	28 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)
24CW	24 Lead, Windowed, Ceramic Flat Package (Cerpack)

Using the ATV750 with ABEL™ and CUPL™

Typical applications for first and second generation PLDs include address decoding and counting. Here is an example using the ATV750, a third generation PLD, to implement a more complex counter. The following pages show example input listings for ABEL™ and CUPL™.

The first listing is for ABEL™ 3.0. The second listing is for CUPL™ 2.15b.

This design uses all twenty flip-flops of the ATV750 to build a 20-bit synchronous / asynchronous counter. With COUNT high and COUNT10, PRESET, RESET, Q1SEL, and OE low, a 1 MHz signal on the CLK pin will produce roughly a 1 Hz signal on pin 23.

The unique architecture of the macrocell gives the ATV750 its versatility and also increases gate utilization. Each of the twenty registers has its Q and $\overline{Q}$ feeding back to the array.

The Output Registers (Q0's) can be addressed directly (by the pin names in ABEL™; in CUPL™ define PINNODES 35 through 44). However, to access the Buried Registers (Q1's), the corresponding nodes have to be named (nodes 26 through 35 in ABEL™, PINNODEs 25 through 34 in CUPL™). They are called B14, B15,...B24 to show the correspondence with their Q0 counterparts. Any valid identifier can be used as a node name.

The ATV750 provides a global synchronous Preset which is accessible through the node definition or by extension. Each of the twenty flip-flops has its own clock, reset and sum term (not like a second generation PLD that allows only one clock and one reset for all registers). Use the '.CK' extension in conjunction with the named registers to define the equations for the clock inputs for all the registers. Use the '.RE' command following the named registers to define the reset terms.

The ATV750 gives the user a total of eight choices to configure each output. The operators ':=' and '=' inform ABEL™ the output is registered or combinatorial, respectively. In CUPL™, use of the .Q extension defines a registered output. Use the '!' operator to define an active low output; active high output is assumed by default. Another convenient method is to use the 'ISTYPE' statement (ABEL™ only) to define the outputs as high/low and registered / combinatorial. (Note: the ATV22V10 is defined the same way.)

The ATV750 has an advanced feature that lets the user combine or separate the sum terms in each macrocell. By default, the terms are combined. In CUPL™ and ABEL™, using the buried register automatically splits the sum terms.

'Sets' (ABEL™) or 'fields' (CUPL™) are often defined for ease of referencing a group of signals or constants. In this particular example, 'OUTS' is a collection of outputs used in the OE definition. "Out" is a reserved word in CUPL, and "Ouch" was used instead.

When PRESET and COUNT are asserted and the Clk pin goes high, all registers, even the asynchronously clocked ones, will go to the 'one' state. This is because as each flip-flop goes high, it forces the clock of the next flip-flop high, rippling the preset condition throughout the entire bank. To reset the output registers and the buried registers, simply have RESET high and vary !Q1SEL accordingly.

The O registers pair with the corresponding B registers to form ten 2-bit synchronous counters. These are clocked by the preceding pair's output, thus forming a 20-bit counter. The last product term for the 'O' logic changes this device into a 10-bit counter with the output register mimicking the B registers. This provides observability, and a handy test mode. Test vectors take full advantage of ABEL™'s and CUPL™'s ability to simulate the device before programming. This feature can save hours

High Density UV Erasable Programmable Logic Device

Application Brief

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of testing and enable the user to make the necessary changes in seconds without ever leaving his or her PC. Therefore, it is highly recommended to take the time to write a comprehensive set of test vectors; this will reduce the time spent on the test bench.

ABEL™ is a trademark of DATA I/O Corporation
CUPL™ is a trademark of Logical Devices, Inc.

ABEL™ Example

```
module EX3
title '20 Bit Counter for Atmel's ATV750
EX375   device    'P750';
Clk                             pin     1;
COUNT,COUNT10,PRESETpin         2, 3, 4;
RESET, Q1SEL , OE               pin     5, 11, 13;
O14,O15,O16,O17,O18             pin     14,15,16,17,18;
O19,O20,O21,O22,O23             pin     19,20,21,22,23;
B14,B15,B16,B17,B18             node    26,27,28,29,30;
B19,B20,B21,B22,B23             node    31,32,33,34,35;
"       Nodes           Description
"       26..35          Q1 for pins 14 to 23
"Sets
OUTS=[O23,O22,O21,O20,O19,O18,O17,O16,O15,O14];
H,L,Z,C,X = 1,0,.Z.,.C.,.X.;
Equations
O14.RE          =       O14.Q & RESET & !Q1SEL;
B14.RE          =       B14 & RESET & Q1SEL;
O15.RE          =       O15.Q & RESET & !Q1SEL;
B15.RE          =       B15 & RESET & Q1SEL;
O16.RE          =       O16.Q & RESET & !Q1SEL;
B16.RE          =       B16 & RESET & Q1SEL;
O17.RE          =       O17.Q & RESET & !Q1SEL;
B17.RE          =       B17 & RESET & Q1SEL;
O18.RE          =       O18.Q & RESET & !Q1SEL;
B18.RE          =       B18 & RESET & Q1SEL;
O19.RE          =       O19.Q & RESET & !Q1SEL;
B19.RE          =       B19 & RESET & Q1SEL;
O20.RE          =       O20.Q & RESET & !Q1SEL;
B20.RE          =       B20 & RESET & Q1SEL;
O21.RE          =       O21.Q & RESET & !Q1SEL;
B21.RE          =       B21 & RESET & Q1SEL;
O22.RE          =       O22.Q & RESET & !Q1SEL;
B22.RE          =       B22 & RESET & Q1SEL;
O23.RE          =       O23.Q & RESET & !Q1SEL;
B23.RE          =       B23 & RESET & Q1SEL;
O14.C           =       Clk & COUNT;
B14.CK          =       Clk & COUNT; "Synchronous
O15.CK          =       O14.Q & COUNT;
B15.CK          =       O14.Q & COUNT; "Asynchronous
O16.CK          =       O15.Q & COUNT;
B16.CK          =       O15.Q & COUNT;
O17.CK          =       O16.Q & COUNT;
B17.CK          =       O16.Q & COUNT;
O18.CK          =       O17.Q & COUNT;
B18.CK          =       O17.Q & COUNT;
O19.CK          =       O18.Q & COUNT;
B19.CK          =       O18.Q & COUNT;
O20.CK          =       O19.Q & COUNT;
B20.CK          =       O19.Q & COUNT;
O21.CK          =       O20.Q & COUNT;
B21.CK          =       O20.Q & COUNT;
O22.CK          =       O21.Q & COUNT;
B22.CK          =       O21.Q & COUNT;
O23.CK          =       O22.Q & COUNT;
B23.CK          =       O22.Q & COUNT;
B14             :=      !B14;
!O14            :=      !O14.Q &  B14 & !COUNT10
                #       O14.Q & !B14 & !COUNT10
                #       !B14 & COUNT10;
B15             :=      !B15;
!O15            :=      !O15.Q & B15 & !COUNT10
                #       O15.Q & !B15 & !COUNT10
                #       !B15 & COUNT10;
B16             :=      !B16;
!O16            :=      !O16.Q & B16 & !COUNT10
                #       O16.Q & !B16 & !COUNT10
                #       !B16 & COUNT10;
B17             :=      !B17;
!O17            :=      !O17.Q & B17 & !COUNT10
                #       O17.Q & !B17 & !COUNT10
                #       !B17 & COUNT10;
B18             :=      !B18;
!O18            :=      !O18.Q & B18 & !COUNT10
                #       O18.Q & !B18 & !COUNT10
                #       !B18 & COUNT10;
B19             :=      !B19;
!O19            :=      !O19.Q &  B19 & !COUNT10
                #       O19.Q & !B19 & !COUNT10
                #       !B19 & COUNT10;
B20             :=      !B20;
!O20            :=      !O20.Q & B20 & !COUNT10
                #       O20.Q & !B20 & !COUNT10
                #       !B20 & COUNT10;
B21             :=      !B21;
!O21            :=      !O21.Q & B21 & !COUNT10
                #       O21.Q & !B21 & !COUNT10
                #       !B21 & COUNT10;
B22             :=      !B22;
!O22            :=      !O22.Q & B22 & !COUNT10
                #       O22.Q & !B22 & !COUNT10
                #       !B22 & COUNT10;
B23             :=      !B23;
!O23            :=      !O23.Q & B23 & !COUNT10
                 #      O23.Q & !B23 & !COUNT10
                #       !B23 & COUNT10;
O23.PR          =       PRESET;
ENABLE OUTS     =       !OE;
End
```

CUPL™ Example

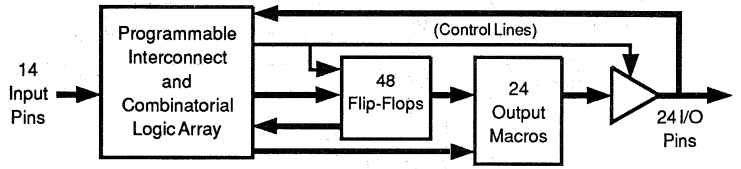
```
Name            EX75;
Company Atmel;
Device          V750;
/*****************************************/
/** Allowable Target Device Types : V750      */
/*****************************************/
/**Inputs **/
PIN [1..4]=     [Clk,COUNT,COUNT10,PRESET];
PIN [5,11,13]   =       RESET,Q1SEL,OE;
/**Outputs**/
PIN [14..23]    =       [Q14..Q23];     /* Pin Outputs*/
/*The easiest way to access the buried nodes in CUPL*/
/*Refer to the I/O pins by their pin names, and the */
/* Q0 and Q1 outputs by their pinnode names   */
PINNODE [25..34] =      [B14..B23]; /* Q1 nodes*/
field BEES      =       [B23..B14];     /*Q1 field*/
field Ohi       =       [O23..O19];     /*output hi field*/
field Olo       =       [O18..O14];     /*output low field*/
field Ouch      =       [O23..O14];     /*outputfield*/
/** Logic Equations **/
/*  The Asynch. Reset terms use the .AR extension*/
Q14.AR          =       Q14 &  RESET & !Q1SEL;
B14.AR          =       B14 &  RESET & Q1SEL;
Q15.AR          =       Q15 &  RESET & !Q1SEL;
B15.AR          =       B15 &  RESET & Q1SEL;
Q16.AR          =       Q16 &  RESET & !Q1SEL;
B16.AR          =       B16 &  RESET & Q1SEL;
Q17.AR          =       Q17 &  RESET & !Q1SEL;
B17.AR          =       B17 &  RESET & Q1SEL;
Q18.AR          =       Q18 &  RESET & !Q1SEL;
B18.AR          =       B18 &  RESET & Q1SEL;
Q19.AR          =       Q19 &  RESET & !Q1SEL;
B19.AR          =       B19 &  RESET & Q1SEL;
Q20.AR          =       Q20 &  RESET & !Q1SEL;
B20.AR          =       B20 &  RESET & Q1SEL;
Q21.AR          =       Q21 &  RESET & !Q1SEL;
B21.AR          =       B21 &  RESET & Q1SEL;
Q22.AR          =       Q22 &  RESET & !Q1SEL;
B22.AR          =       B22 &  RESET & Q1SEL;
Q23.AR          =       Q23 &  RESET & !Q1SEL;
B23.AR          =       B23 &  RESET & Q1SEL;
/* The Clock lines are accessed with the .CK extension*/
Q14.CK          =       Clk & COUNT;
B14.CK          =       Clk & COUNT; /* Synchronous */
Q15.CK          =       Q14 & COUNT;
B15.CK          =       Q14 & COUNT; /* Asynchronous*/
Q16.CK          =       Q15 & COUNT;
B16.CK          =       Q15 & COUNT;
Q17.CK          =       Q16 & COUNT;
B17.CK          =       Q16 & COUNT;
Q18.CK          =       Q17 & COUNT;
B18.CK          =       Q17 & COUNT;
Q19.CK          =       Q18 & COUNT;
B19.CK          =       Q18 & COUNT;
Q20.CK          =       Q19 & COUNT;
B20.CK          =       Q19 & COUNT;
Q21.CK          =       Q20 & COUNT;
B21.CK          =       Q20 & COUNT;
Q22.CK          =       Q21 & COUNT;
B22.CK          =       Q21 & COUNT;
Q23.CK          =       Q22 & COUNT;
B23.CK          =       Q22 & COUNT;
B14.D           =       !B14;
Q14.D           =       !Q14 &  B14 & !COUNT10
                #       Q14 & !B14 & !COUNT10
                #       !B14 & COUNT10;
/* Equations for both the B and the Q automatically     */
/*tells CUPL to set the 'split' SUM term's architecture bit.*/
B15.D           =       !B15;
Q15.D           =       !Q15 & B15 & !COUNT10
                #       Q15 & !B15 & !COUNT10
                #       !B15 & COUNT10;
B16.D           =       !B16;
Q16.D           =       !Q16 & B16 & !COUNT10
                #       Q16 & !B16 & !COUNT10
                #       !B16 & COUNT10;
B17.D           =       !B17;
Q17.D           =       !Q17 & B17 & !COUNT10
                #       Q17 & !B17 & !COUNT10
                #       !B17 & COUNT10;
B18.D           =       !B18;
Q18.D           =       !Q18 & B18 & !COUNT10
                #       Q18 & !B18 & !COUNT10
                #       !B18 & COUNT10;
B19.D           =       !B19;
Q19.D           =       !Q19 & B19 & !COUNT10
                #       Q19 & !B19 & !COUNT10
                #       !B19 & COUNT10;
B20.D           =       !B20;
Q20.D           =       !Q20 & B20 & !COUNT10
                #       Q20 & !B20 & !COUNT10
                #       !B20 & COUNT10;
B21.D           =       !B21;
Q21.D           =       !Q21 & B21 & !COUNT10
                #       Q21 & !B21 & !COUNT10
                #       !B21 & COUNT10;
B22.D           =       !B22;
Q22.D           =       !Q22 &  B22 & !COUNT10
                #       Q22 & !B22 & !COUNT10
                #       !B22 & COUNT10;
B23.D           =       !B23;
Q23.D           =       !Q23 & B23 & !COUNT10
                #       Q23 & !B23 & !COUNT10
                #       !B23 & COUNT10;
/*Only one synch preset equation is required    */
O23.SP  =       PRESET;
/*Use the .OE extension for the OE product term*/
O14.oe          =       !OE ;   O19.oe  =       !OE ;
O15.oe          =       !OE ;   O20.oe  =       !OE ;
O16.oe          =       !OE ;   O21.oe  =       !OE ;
O17.oe          =       !OE ;   O22.oe  =       !OE ;
O18.oe          =       !OE ;   O23.oe  =       !OE ;
```

High Density UV Erasable Programmable Logic Device

Features

- **Third Generation Programmable Logic Structure**
  - **Easily Achieves Gate Utilization Factors of 80 Percent**
- **Increased Logic Flexibility**
  - **86 Inputs and 72 Sum Terms**
- **Flexible Output Macrocell**
  - **48 Flip-Flops - 2 per Macrocell**
  - **3 Sum Terms - Can Be OR'ed and Shared**
- **High Speed**
- **Low Power - Less than 0.5mA Typical (ATV2500L)**
- **Multiple Feedback Paths Provide For Buried State Machines and I/O Bus Compatibility**
- **Asynchronous Clocks and Resets**
  - **Multiple Synchronous Presets - 1 per 4 or 8 Flip-Flops**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **40 pin Dual-In-line and 44 Lead Surface Mount Packages**

Block Diagram



Description

The ATV2500H/L is the most powerful programmable logic device available in a 40 pin package. Increased Product terms, Sum Terms, and Flip-Flops translate into many more usable gates. High gate utilization is easily obtainable.

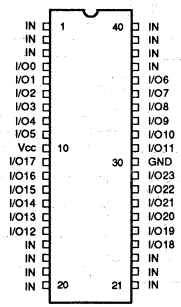
The ATV2500H/L is organized around a global bus. All pin and feedback terms are always available to every Logic Cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 Flip-Flops.

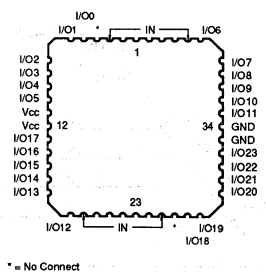
There are 416 Product Terms available. Four Product Terms are input to each Sum Term. The 3 Sum terms per Logic Cell can be combined to provide up to 12 Product Terms, Combinatorial and Registered. Independent of output configuration, the 2 Flip-Flops are always usable, and always have at least 4 Product Term inputs.

Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. Eight product terms provide local Synchronous Presets, divided up into banks of 4 and 8 Flip-Flops. Register Preload and buried register observability simplify testing. The device has an internal power up clear function.

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O,0,2,4..	"Even" I/O Buffers
I/O,1,3,5..	"Odd" I/O Buffers
*	No Internal Connection
VCC	+5V Supply





* = No Connect

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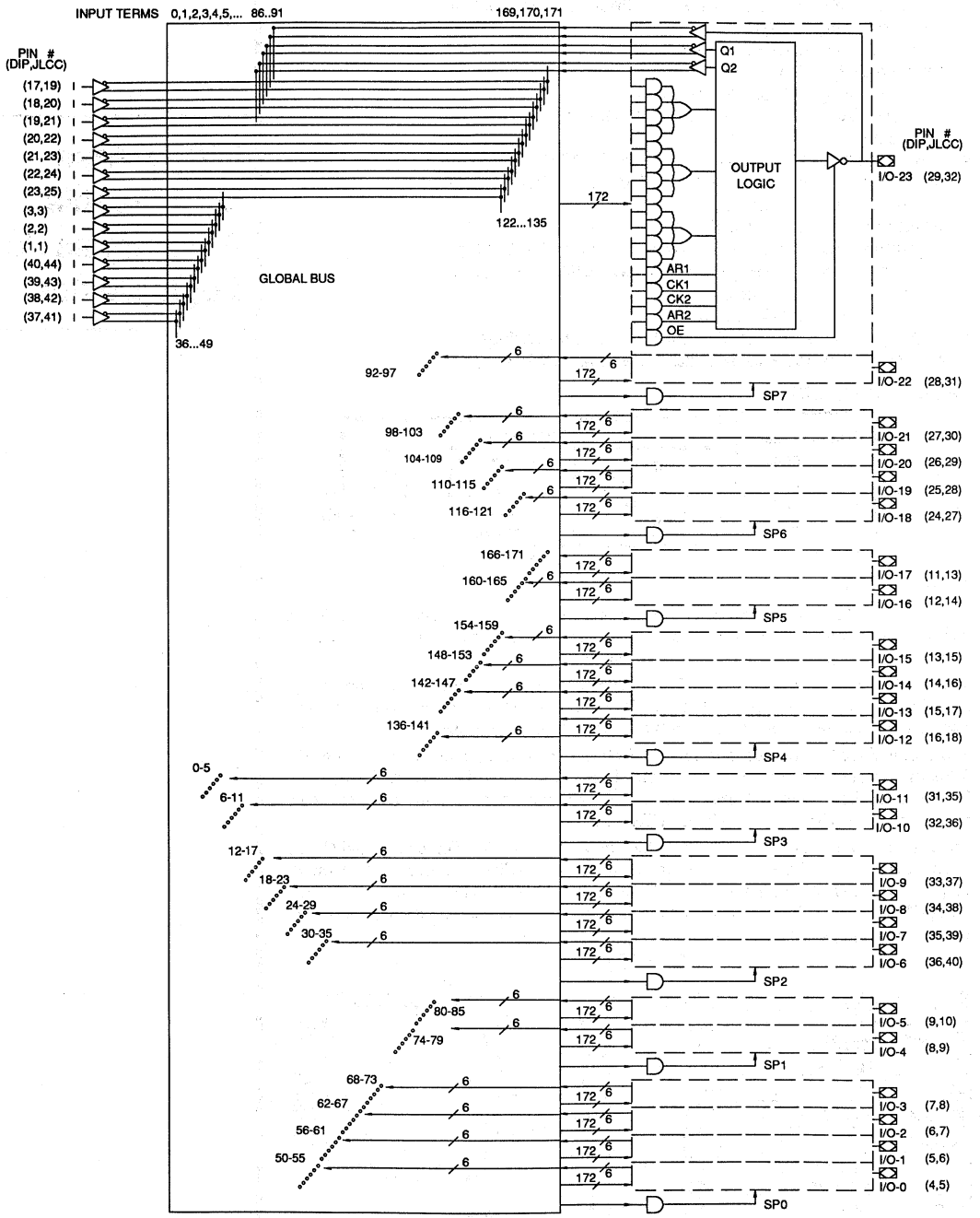
Functional Logic Diagram ATV2500H/L



Functional Logic Diagram Description

The ATV2500H/L Functional Logic Diagram describes the interconnections between the input, feedback pins and Logic Cells. All interconnections are routed through the Global Bus.

The ATV2500H/L is a straightforward and uniform EPLD. The 24 Macrocells are numbered 0 through 23. Each Macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per Flip-Flop, and an Output Enable. The top 12 product terms are grouped into 3 sum terms, which are used as shown in the Macrocell diagrams.

Eight Synchronous Preset terms are distributed in a 2/4 pattern. The first four Macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two Macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each Macrocell provides 6 inputs to the global bus: (left to right) Flip-Flop Q2 true and false, Flip-Flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the Global Bus are the six numbers in the bus diagram next to each Macrocell.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W·sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

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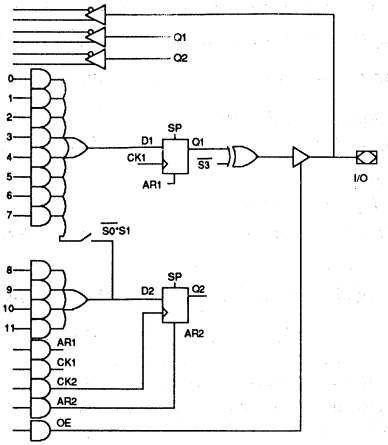
Operating Modes

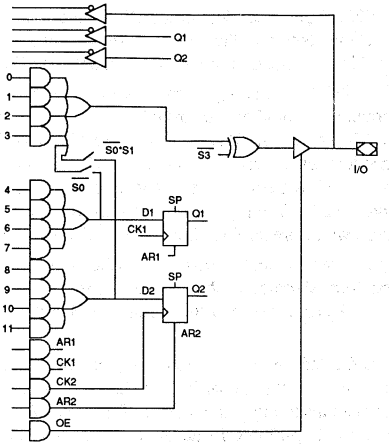
	40 DIP PIN	21	2	38	23	20	V_{CC}(10)	Odd	Even
Mode	44 JLCC PIN	23	2	42	25	22	V_{CC}(11,12)	I/O's	I/O's
"EPLD"		X(1)	X	X	X	X	5V	I/O	I/O
Program		V_{PP}	X	X	X	V_H (2)	6V	D_{IN}	N.C.
PGM Verify		V_{PP}	X	X	X	V_{IL}	6V	D_{OUT}	V_{OH}
PGM Inhibit		V_{PP}	X	X	X	V_{IH}	6V	High Z	High Z
Preload Q1		⎍	X	V_H	V_{IL}/V_{IH}	V_{IL}	5V	D_{IN}(Even/Odd)	V_{IH}
Preload Q2		⎍	X	V_H	V_{IL}/V_{IH}	V_{IH}	5V	D_{IN}(Even/Odd)	V_{IH}
Observe Q2		X	V_H	X	X	X	5V	D_{OUT}	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

Output Logic, Registered [1]



Output Logic, Combinatorial [1]



Note: 1. These diagrams shows equivalent logic functions, not necessarily the actual circuit implementation.

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
0	0	0	8	4	Registered (Q1)
0	1	0	12	4[1]	Registered (Q1)

Note: 1. These 4 terms are shared with D1.

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
1	0	0	4[1]	4	Combinatorial (8 Terms)
1	0	1	4	4	Combinatorial (4 Terms)
1	1	0	4[1]	4[1]	Combinatorial (12 Terms)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

S3	Output Configuration
0	Active Low
1	Active High

D.C. and A.C. Operating Conditions

		ATV2500H-25	ATV2500H/L-30	ATV2500H/L-35	ATV2500L-40	ATV2500L-45
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V					10	µA
I_{CC}	Power Supply Current	V_{CC}=MAX, V_{IN}=GND or V_{CC} Outputs Open	ATV2500L	Com.		0.5	5	mA
				Ind.,Mil.		0.5	10	mA
			ATV2500H	Com.		80	160	mA
				Ind.,Mil.		80	180	mA
I_{CC2}	Clocked Power Supply Current (ATV2500L)	f=1MHz,V_{CC}=MAX Outputs Open		Com.		10	15	mA
				Ind.,Mil.		10	20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V					-90	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN}=V_{IH} or V_{IL}, I_{OL}=8mA Com,Ind;6mA Mil.					0.5	V
V_{OH}	Output High Voltage	I_{OH}=-100µA			V_{CC}-0.3			V
		I_{OH}=-4.0mA			2.4			V

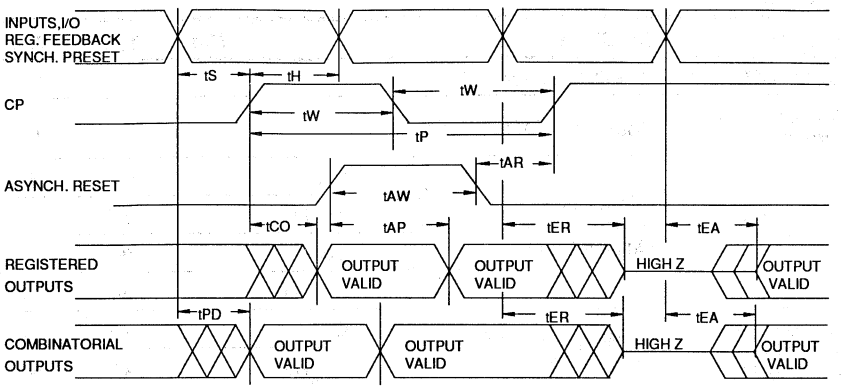
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

Pin Capacitance (f=1MHz T=25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics for the ATV2500L

Symbol	Parameter	ATV2500L-30		ATV2500L-35		ATV2500L-40		ATV2500L-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40		45	ns
t_{EA}	Input to Output Enable		30		35		40		45	ns
t_{ER}	Input to Output Disable		30		35		40		45	ns
t_{CO}	Clock to Output	5	30	5	35	5	40	5	45	ns
t_{CF}	Clock to Feedback	10	20	15	20	15	22	15	25	ns
t_{SI1}	Input Setup Time, Output Register	20		22		25		30		ns
t_{SI2}	Input Setup Time, Buried Register[1]	5		5		5		5		ns
t_{SF}	Feedback Setup Time	10		15		18		20		ns
t_{H1}	Hold Time, Output Register	10		15		15		15		ns
t_{H2}	Hold Time, Buried Register[1]	5		5		5		5		ns
t_W	Clock Width	12		15		17		20		ns
t_P	Clock Period	30		35		40		45		ns
F_{MAX}	Maximum Frequency (1/t_P)		33		28		25		22	MHz
t_{AW}	Asynchronous Reset Width	18		20		22		25		ns
t_{AR}	Asynchronous Reset Recovery Time	18		20		22		25		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40		45	ns

Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

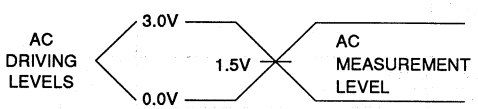
A.C. Characteristics for the ATV2500H

Symbol	Parameter	ATV2500H-25		ATV2500H-30		ATV2500H-35		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		25		30		35	ns
t_{EA}	Input to Output Enable		25		30		35	ns
t_{ER}	Input to Output Disable		25		30		35	ns
t_{CO}	Clock to Output	10	25	12	30	15	35	ns
t_{CF}	Clock to Feedback	10	18	12	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	10		12		15		ns
t_{SI2}	Input Setup Time, Buried Register(1)	5		5		5		ns
t_{SF}	Feedback Setup Time	7		10		15		ns
t_{H1}	Hold Time	5		5		5		ns
t_W	Clock Width	10		12		15		ns
t_P	Clock Period	25		30		35		ns
F_{MAX}	Maximum Frequency (1/t_P)		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	15		18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		30		35	ns

Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

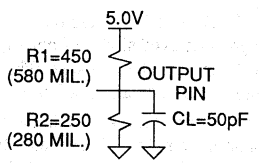
8

Input Test Waveforms and Measurement Levels



tR, tF < 5ns (10% to 90%)

Output Test Load

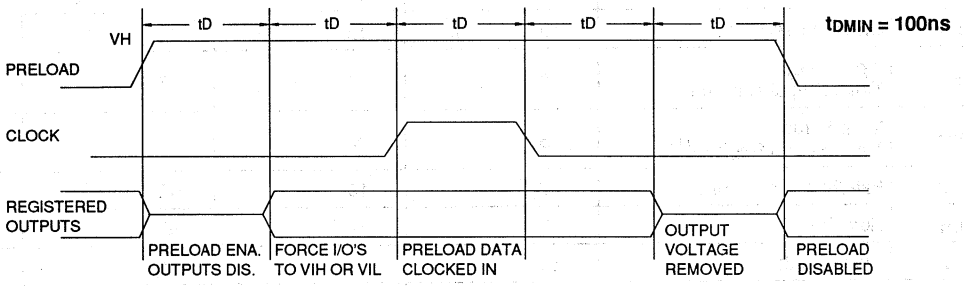


Preload and Observability of Registered Outputs

The ATV2500H/L's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the Odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 11V to 14V signal on pin 38 on the DIP and pin 42 on the SMP. When the clock term is pulsed high, (pin 21 on the DIP, pin 23 on the SMP) the data on the I/O pins is placed into the 12 registers chosen by the Q Select and Even/Odd Select Pins.

Register 2 Observability Mode is entered by placing an 11V to 14V signal on pin 2 (DIP or SMP). In this mode, the contents of the Buried Register bank will appear on the associated outputs when the OE control signals are active.



Level forced on Odd I/O pin during PRELOAD cycle.	Q Select Pin State	Even/ Odd Select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power Up Reset

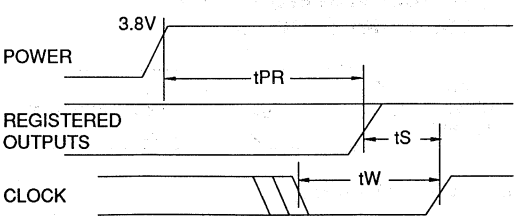
The registers in the ATV2500H/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV2500H/L fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS EPLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.25 micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64k to 1024k bit devices.

Using The ATV2500's Many Advanced Features

The ATV2500H/L's flexibility puts more usable gates in 40 pins than other EPLDs. Some of the ATV2500H/L's key features are:

- Asynchronous Clocks -

Each of the Flip-Flops in the ATV2500H/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV2500H/L clock period matches that of similar synchronous devices.

- A Total of 48 Registers -

The ATV2500H/L provides two Flip-Flops for each Output Macrocell - a total of 48. Each register has its own clock and reset product terms, as well as its own SUM term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500/H has a dedicated input path. Each of the 48 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.

- 3 Sum Terms per Macrocell -

The ATV2500H/L Macrocell can be configured with one Sum term feeding the output, and still have 2 Sum terms feeding the Flip-Flops. This is the simplest method for interfacing with an I/O bus, and no Flip-Flops need be sacrificed.

- Combinable Sum Terms -

Each Output Macrocell's 3 SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 12 product terms per Output or Flip-Flop. When the Registered Output configuration is chosen, 8 terms are automatically available to D1. The 4 terms feeding D2 can also be shared with D1, giving it a total of 12. In the combinatorial mode, 4, 8, or 12 terms can feed the output, with the middle 4 still driving D1 and the bottom 4 still driving D2.

8

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV2500H/L is currently available from the following sources:

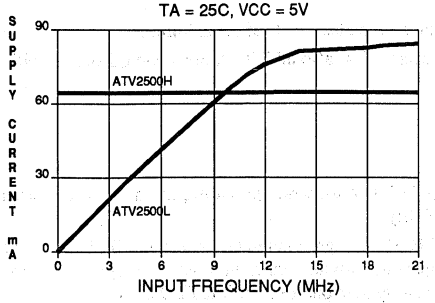
Data I/O / Futurenet Corp.	- ABEL™ 4.0 and above
Logical Devices	- CUPL 3.0 and above
Atmel Corp.	-Atmel-ABEL-4

Erasure Characteristics

The entire memory array of an ATV2500H/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

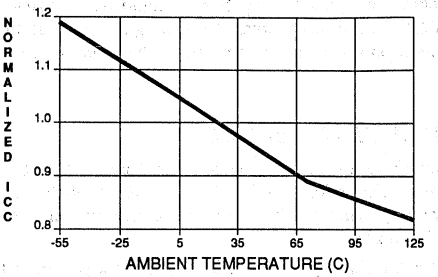
SUPPLY CURRENT vs. INPUT FREQUENCY

TA = 25C, VCC = 5V



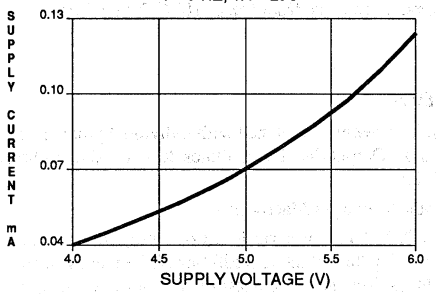
NORMALIZED ICC vs. AMBIENT TEMP.

f = 20 MHz, VCC = 5V



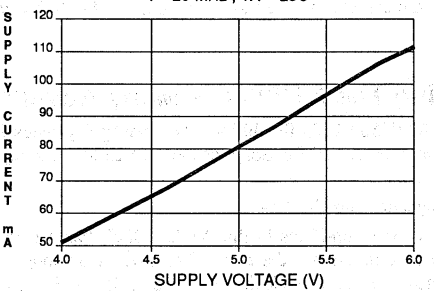
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 0 HZ, TA = 25C



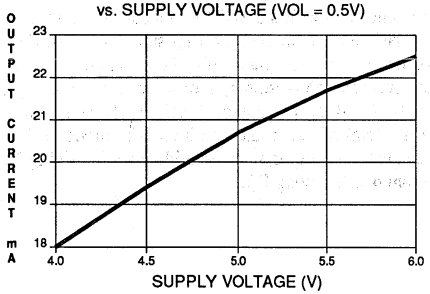
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 20 MHz , TA = 25C



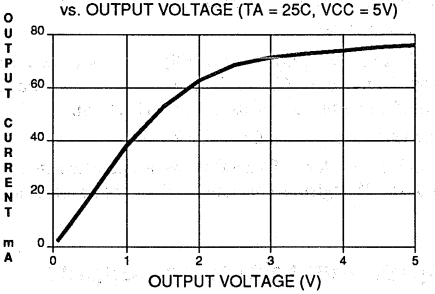
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



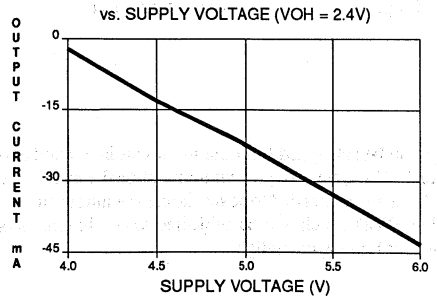
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



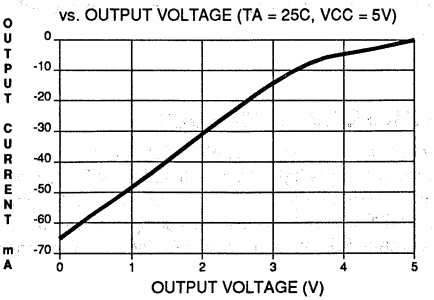
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

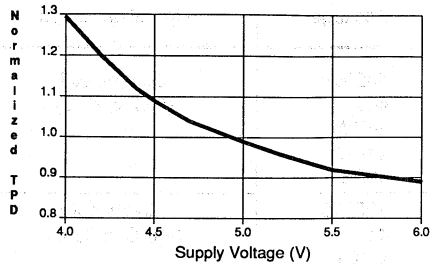


OUTPUT SOURCE CURRENT

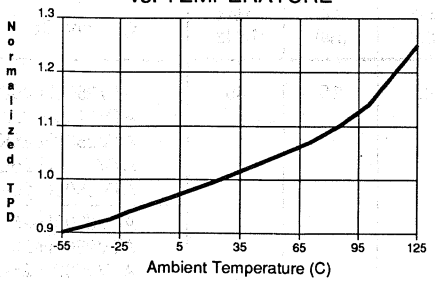
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



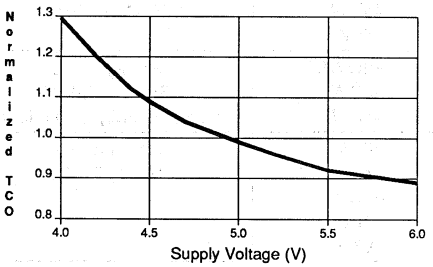
NORMALIZED TPD
vs. SUPPLY VOLTAGE



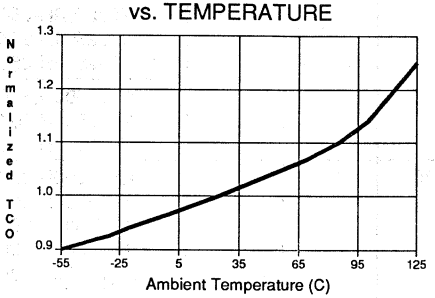
NORMALIZED TPD
vs. TEMPERATURE



NORMALIZED TCO
vs. SUPPLY VOLTAGE

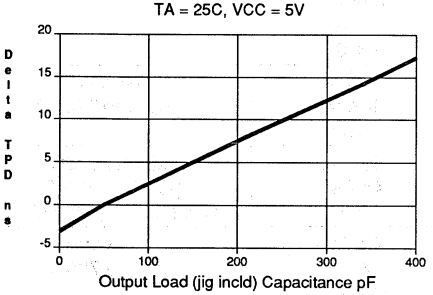


NORMALIZED TCO
vs. TEMPERATURE



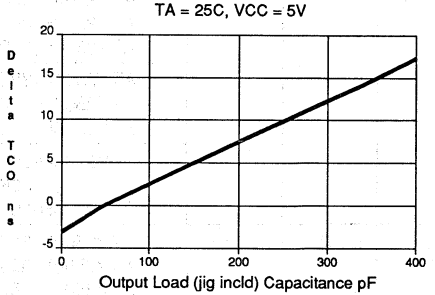
DELTA TPD vs. OUTPUT LOADING

TA = 25C, VCC = 5V



DELTA TCO vs. OUTPUT LOADING

TA = 25C, VCC = 5V



8

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	25	40	ATV2500H-25DC ATV2500H-25JC ATV2500H-25KC ATV2500H-25LC ATV2500H-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-25DI ATV2500H-25JI ATV2500H-25KI ATV2500H-25LI ATV2500H-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-25DM ATV2500H-25KM ATV2500H-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-25DM/883 ATV2500H-25KM/883 ATV2500H-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	ATV2500H-30DC ATV2500H-30JC ATV2500H-30KC ATV2500H-30LC ATV2500H-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-30DI ATV2500H-30JI ATV2500H-30KI ATV2500H-30LI ATV2500H-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-30DM ATV2500H-30KM ATV2500H-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-30DM/883 ATV2500H-30KM/883 ATV2500H-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500H-35DC ATV2500H-35JC ATV2500H-35KC ATV2500H-35LC ATV2500H-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-35DI ATV2500H-35JI ATV2500H-35KI ATV2500H-35LI ATV2500H-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-35DM ATV2500H-35KM ATV2500H-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
35	35	28	ATV2500H-35DM/883 ATV2500H-35KM/883 ATV2500H-35LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	30	33	ATV2500L-30DC ATV2500L-30JC ATV2500L-30KC ATV2500L-30LC ATV2500L-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
35	35	28	ATV2500L-35DC ATV2500L-35JC ATV2500L-35KC ATV2500L-35LC ATV2500L-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-35DI ATV2500L-35JI ATV2500L-35KI ATV2500L-35LI ATV2500L-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-35DM ATV2500L-35KM ATV2500L-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-35DM/883 ATV2500L-35KM/883 ATV2500L-35LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
40	40	25	ATV2500L-40DC ATV2500L-40JC ATV2500L-40KC ATV2500L-40LC ATV2500L-40PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-40DI ATV2500L-40JI ATV2500L-40KI ATV2500L-40LI ATV2500L-40PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-40DM ATV2500L-40KM ATV2500L-40LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-40DM/883 ATV2500L-40KM/883 ATV2500L-40LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
45	45	22	ATV2500L-45DI ATV2500L-45JI ATV2500L-45KI ATV2500L-45LI ATV2500L-45PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
45	45	22	ATV2500L-45DM ATV2500L-45KM ATV2500L-45LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-45DM/883 ATV2500L-45KM/883 ATV2500L-45LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

8

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Using the ATV2500 with ABEL™ and CUPL™

The following two examples show example headers to use when designing the ATV2500 with ABEL™ or CUPL™.

For ABEL™, the node numbers shown may be assigned any legal ABEL™ label. The fuse numbers for combining the product terms are included.

For CUPL™, the pinnodes shown may be assigned any legal CUPL™ label. Combining the product terms is handled automatically.

ABEL™ Example

```
module _NODE2500
title 'Addressing 48 Registers in V2500
NODE2500 device 'P2500';
        @message 'Use P2500PC device file.';
        @message 'for ABEL on a PC/Clone';
"Inputs
I1,I2,I3                                pin     1,2,3;
I17,I18,I19,I20,I21,I22,I23             pin     17,18,19,20,21,22,23;
I37,I38,I39,I40                         pin     37,38,39,40;
"I/Os
O4,O5,O6,O7,O8,O9                       pin     4,5,6,7,8,9;
O11,O12,O13,O14,O15,O16                 pin     11,12,13,14,15,16;
O24,O25,O26,O27,O28,O29                 pin     24,25,26,27,28,29;
O31,O32,O33,O34,O35,O36                 pin     31,32,33,34,35,36;

"Q2 Registers
"Node Name          Node    Number          Pin Associated With:
B4,B5,B6            node    41,42,43;       " pin 4 to pin 6
B7,B8,B9            node    44,45,46;       " pin 7 to pin 9
B11,B12,B13         node    47,48,49;       " pin 11 to pin 13
B14,B15,B16         node    50,51,52;       " pin 14 to pin 16
B24,B25,B26         node    53,54,55;       " pin 24 to pin 26
B27,B28,B29         node    56,57,58;       " pin 27 to pin 29
B31,B32,B33         node    59,60,61;       " pin 31 to pin 33
B34,B35,B36         node    62,63,64;       " pin 34 to pin 36
"Q1 Registers
"Node Name          Node    Number          Pin Associated With:
Q4,Q5,Q6            node    217,218,219;    " pin 4 to pin 6
Q7,Q8,Q9            node    220,221,222;    " pin 7 to pin 9
Q11,Q12,Q13         node    223,224,225;    " pin 11 to pin 13
Q14,Q15,Q16         node    226,227,228;    " pin 14 to pin 16
Q24,Q25,Q26         node    229,230,231;    " pin 24 to pin 26
Q27,Q28,Q29         node    232,233,234;    " pin 27 to pin 29
Q31,Q32,Q33         node    235,236,237;    " pin 31 to pin 33
Q34,Q35,Q36         node    238,239,240;    " pin 34 to pin 36
```

CUPL™ Example

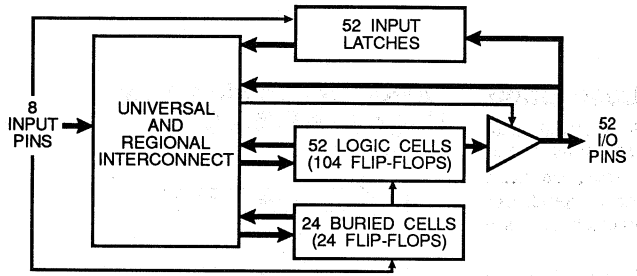
```
Name        NODE2500
Partno      00;
Date        11/21/88;
Revision    00;
Designer    J. Yu
Company     Atmel;
Assembly    None;
Location    None;
Device      V2500;
/*****************************************/
/** Allowable Target Device Types : V2500      **/
/*****************************************/
/** Inputs **/
/* This is a handy way to name a set of pins */
PIN [1..3]    =    [I1..I3];
PIN [17..23]  =    [I17..I23];
PIN [37..40]  =    [I37..I40];
/**  I/Os    **/
PIN [4..9]    =    [O4..O9];
PIN [11..16]  =    [O11..O16];
PIN [24..29]  =    [O24..O29];
PIN [31..36]  =    [O31..O36];
/** Declarations and Intermediate Variable Definitions */
/* Q2 nodes                              Pin assoc. with:*/
PINNODE [41..46]  = [B4..B9];      /*PIN 4 to 9*/
PINNODE [47..52]  = [B11..B16];    /*PIN 11 to 16*/
PINNODE [53..58]  = [B24..B29];    /*PIN 24 to 29*/
PINNODE [59..64]  = [B31..B36];    /*PIN 31 to 36*/
/* Q1 nodes                              Pin assoc. with:*/
PINNODE [65..70]  = [Q4..Q9];      /*PIN 4 to 9*/
PINNODE [71..76]  = [Q11..Q16];    /*PIN 11 to 16*/
PINNODE [77..82]  = [Q24..Q29];    /*PIN 24 to 29*/
PINNODE [83..88]  = [Q31..Q36];    /*PIN 31 to 36*/
etc.
```

Features

- **Advanced Programmable Logic Device - High Gate Utilization**
- **Flexible Interconnect Architecture - Universal Routing**
- **Flexible Logic Cells - 128 Flip-Flops and 52 Latches**
- **Multiple Flip-Flop Types - Synchronous or Asynchronous Registers**
- **High Speed - 50 MHz Operation**
- **Complete Third Party Software Support**
  - **No Placement, Routing or Layout Software Required**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **Commercial, Industrial and Military Temperature Grades**

High Density UV Erasable Programmable Logic Device

Block Diagram



Description

The Atmel V5000 is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

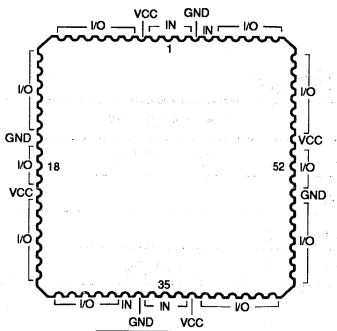
The ATV5000 has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

All 128 registers are configurable as D or T types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard, off-the-shelf third party software tools and programmers support the ATV5000. This minimizes start-up investment and improves product support.

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic and Clock Inputs
Pins 2,32,36,66	Input/Register Clocks 1-4
Pins 1,34,35,68	Input/Latch Clocks 1-4
I/O	Bidirectional Buffers
VCC	+5V Supply



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V[1]
Programming Voltage with Respect to Ground	-2.0V to +14.0V[1]
Integrated UV Erase Dose	7258 W-sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

Functional Logic Diagram Description

There are 52 identical Input/Ouput logic cells and 24 identical buried logic cells in the ATV5000. Each I/O cell has 2 flip-flops, up to 3 sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least 4 Product Term inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The ATV5000 has 4 identical quadrants (see Figure 2). The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The 8 input-only pins are available in all 4 regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 1). The I/O Logic Cells contain 3 sum terms, 2 flip-flops, and an I/O buffer.

The Buried Logic Cells each contain 1 Flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

Quadrant Functional Logic Diagram ATV5000

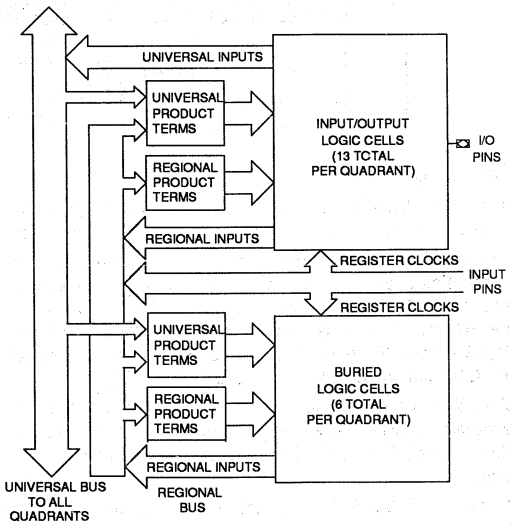


Figure 1

D.C. and A.C. Operating Range

		ATV5000-25	ATV5000/L-30	ATV5000/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V±10%	5V±10%	5V±10%

ATV5000 Block Diagram

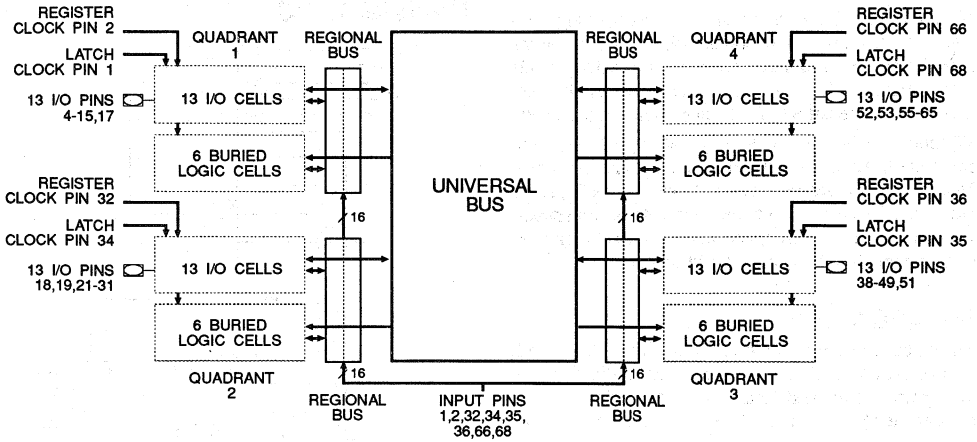


Figure 2

Quadrant Logic Diagram and Description

The ATV5000 has: 4 identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The Universal Bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The 8 input-only pins are available in every Regional Bus.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 3). The I/O Logic Cells (Figures 7, 8, 9) contain 3 sum terms, 2 flip-flops, and an I/O buffer. Sum term B has 5 product terms - 2 universal and 3 regional. Sum terms A and C each have 4 product terms - 1 universal and 3 regional. Flip-flop Q1 has global Asynchronous Preset, Reset, and Clock product terms. Flip-flop Q2 has universal Asynchronous Reset and Clock terms and a regional Asynchronous Preset term. There is 1 universal product term for the I/O pin Output Enable.

The Buried Logic Cells (Figure 4) each contain 1 flip-flop. The sum term has 1 universal product term and 4 regional product terms for a total of 5. The flip-flop has universal Asynchronous Preset, Reset, and Clock terms. In addition, in each buried logic cell the sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip flop inputs) and the 8 dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

Quadrant Clock Pin Assignments

Quadrant Number	Register Clock Pin	Latch Clock Pin
1	2	1
2	32	34
3	36	35
4	66	68

Quadrant Structure

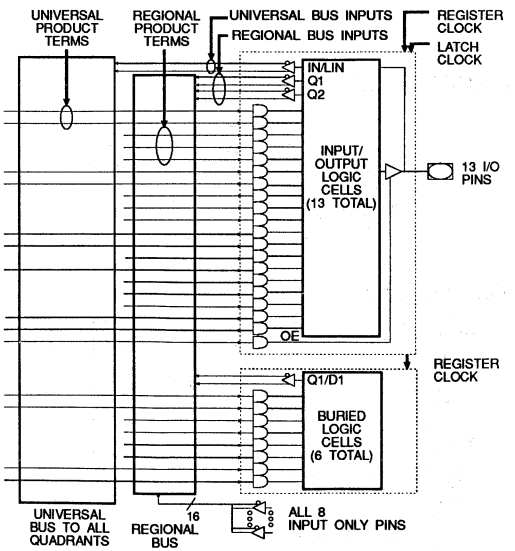


Figure 3

Logic Cell Options

The ATV5000 Logic Cells contain most of the chip's logic options. The standard Logic Cell contains 2 flip-flops, 3 sum terms and 3 array inputs. The 3 sum terms can be combined to provide sum term options of 4, 5, 9, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The ATV5000 retains the ATV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 8). A new feature, unique to the ATV5000, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 7). This high speed logic expansion term increases the devices flexibility and gate utilization.

Buried Logic Cells

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with 5 product terms, a flip-flop, and individual preset, clear, and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

Buried Logic Cells

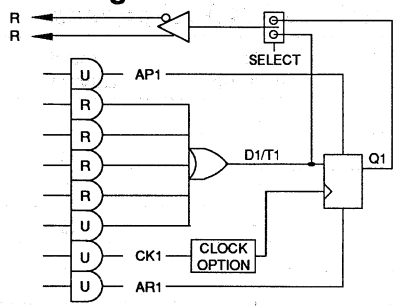


Figure 4

Clock Option

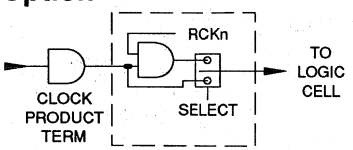


Figure 5

I/O Pin Logic

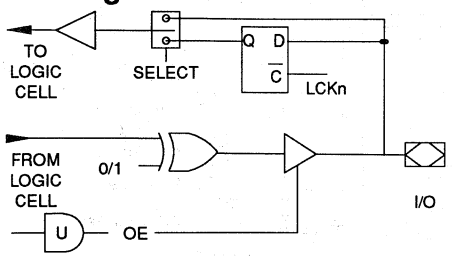


Figure 6

Logic Cell with Buried Sum Term and Register to I/O Cell

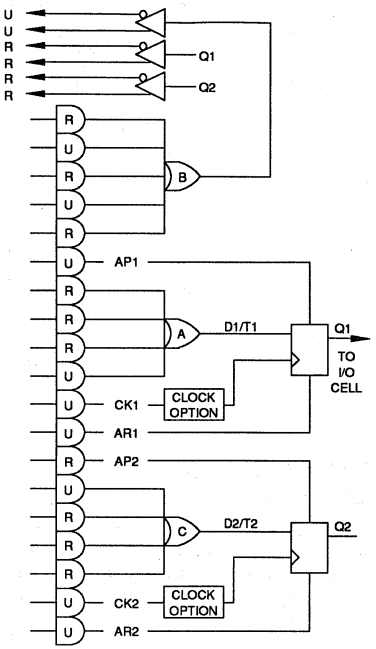


Figure 7

Flip-Flop Clock Options

Each register may be connected to its regional clock to provide fast clock to output timing (see Figure 5). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O Pin Latches

Each I/O pin of the ATV5000 has an input latch which can be individually enabled or disabled (see Figure 6). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is low, and data is captured on the clock's rising edge.

Flip-Flop Types

Each flip-flop in the ATV5000 may be configured as either a T or D type flip-flop. A T type flip-flop can also easily be configured into a JK or SR flip-flop.

Logic Cell, 2 Buried Registers, Combinatorial to I/O Cell

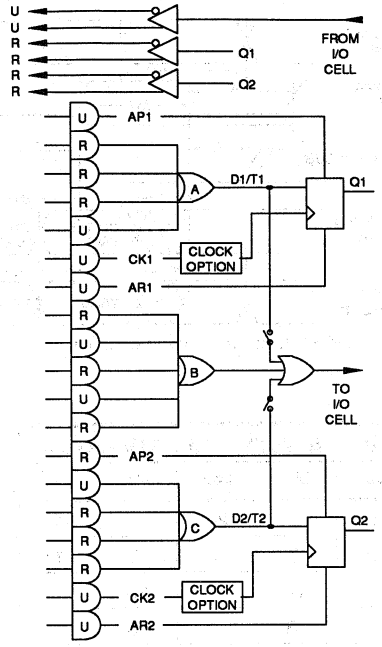


Figure 8

Logic Cell with Combinable Sum Terms, Register to I/O Cell

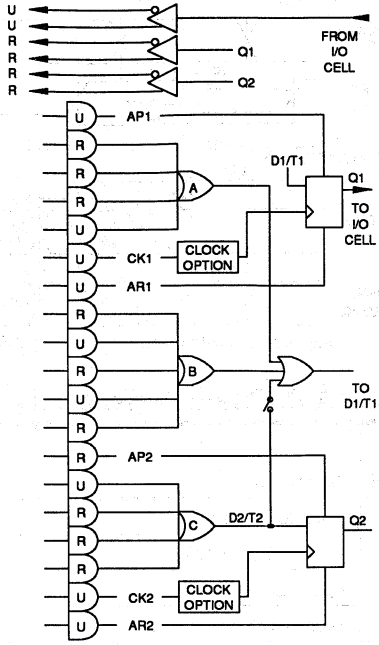


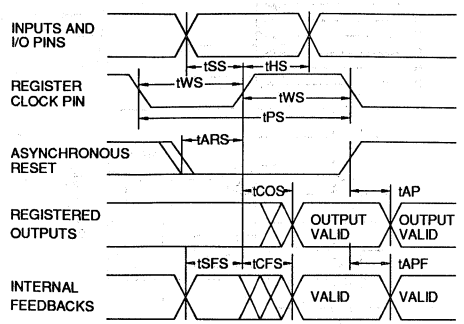
Figure 9

D.C. Characteristics

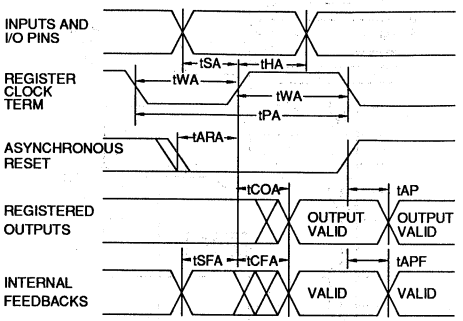
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+1V				10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC}+0.1V				10	µA
I_{CC}	Power Supply Current ATV5000	V_{CC}=MAX, V_{IN}=GND or V_{CC} Outputs Open	Com.		200	350	mA
			Ind.,Mil.		200	400	mA
I_{CC}	Power Supply Current ATV5000L	V_{CC}=MAX, V_{IN}=GND or V_{CC} Outputs Open	Com.		20	40	mA
			Ind.,Mil.		20	50	mA
I_{CC2}	Clocked Power Supply Current, ATV5000L Only	f=1MHz,V_{CC}=MAX Outputs Open	Com.		30	50	mA
			Ind.,Mil.		30	60	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V				-90	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN}=V_{IH} or V_{IL}, I_{OL}=8mA Com,Ind; 6mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH}=-100µA		V_{CC}-0.3			V
		I_{OH}=-4.0mA		2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.

A.C. Waveforms [1] Input Pin Clock



A.C. Waveforms [1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{COS}	Clock to Output		15		20		25	ns
t_{CFS}	Clock to Feedback	0	9	0	12	0	15	ns
t_{SIS}	Input Setup Time[1]	16		17		20		ns
t_{SFS}	Feedback Setup Time[1]	11		13		15		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	10		12		15		ns
t_{PS}	Clock Period	20		25		30		ns
F_{MAXS}	Maximum Frequency ($1/t_{PS}$)		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		30		ns

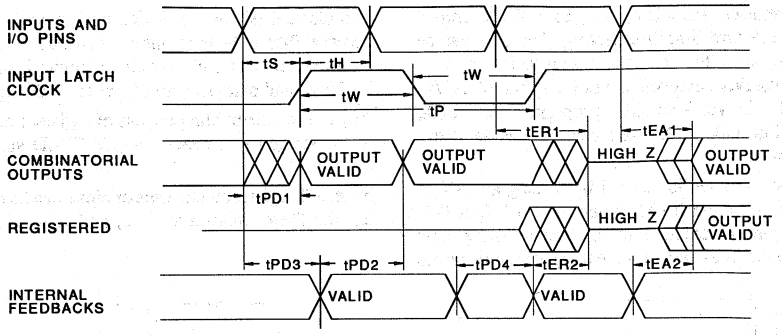
Note: 1. Add 3ns for Universal Product Terms.

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{COA}	Clock to Output		25		30		35	ns
t_{CFA}	Clock to Feedback	7	20	10	25	12	27	ns
t_{SIA}	Input Setup Time[1]	10		12		15		ns
t_{SFA}	Feedback Setup Time[1]	5		8		13		ns
t_{HA}	Hold Time	8		10		12		ns
t_{WA}	Clock Width	12		15		15		ns
t_{PA}	Clock Period	25		33		40		ns
F_{MAXA}	Maximum Frequency ($1/t_{PA}$)		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Note: 1. Add 3ns for Universal Product Terms.

A.C. Waveforms [1]



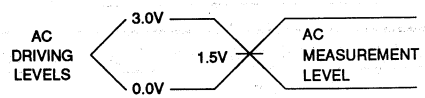
Notes: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{PD1}	Input to Non-Registered Output[1]		25		30		35	ns
t_{PD2}	Feedback to Non-Registered Output[1]		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback[1]		20		25		30	ns
t_{PD4}	Feedback to Non-Registered Feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Clock Width	10		12		12		ns
t_P	Clock Period	20		25		30		ns
F_{MAX}	Maximum Frequency (1/t_P)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		20		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		25		30		35	ns

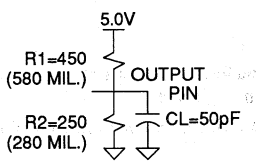
Note: 1. Add 3ns for Universal Product Terms.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5ns (10% to 90%)

Output Test Load



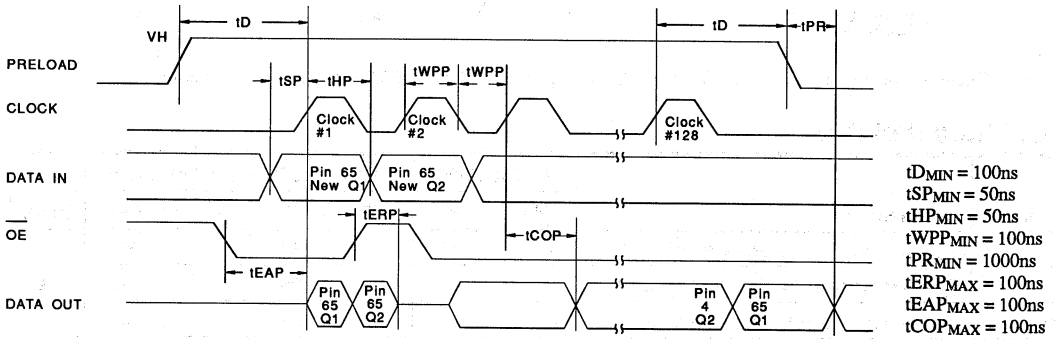
Preload and Observability of Registers

The ATV5000's registers include circuity to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD/OBSERVE state is entered by placing an 11V to 14V signal on pin 68 on the JLCC. When the clock (pin 1) is pulsed high, data (pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, OE (pin 66) can be held high and data out (pin 65) will remain high impedance.

Any user contemplating the use of register preload/obervability is encouraged to contact Atmel's EPLD applications department.

Note: All register clock terms or pins must be low prior to entering the Preload/Observe state, and low prior to leaving the



tD_{MIN} = 100ns
tSP_{MIN} = 50ns
tHP_{MIN} = 50ns
$tWPP_{MIN}$ = 100ns
tPR_{MIN} = 1000ns
$tERP_{MAX}$ = 100ns
$tEAP_{MAX}$ = 100ns
$tCOP_{MAX}$ = 100ns

Preload / Observe Register Scan Order

Quadrant	Pin																			
Quadrant 1	Pin	4			5			6			•••			15			17			
	D_{IN}	→ Q2	→ Q1	→ B23	→ Q2	→ Q1	→ Q2	→ Q1	•••	B18	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 2)					
Quadrant 2	Pin	18			19			21			22		•••			31				
(Quadrant 1)→		Q2	→ Q1	→ Q2	→ Q1	→ B17	→ Q2	→ Q1	→ Q2	→ Q1	•••	B12	→ Q2	→ Q1	→ (Quadrant 3)					
Quadrant 3	Pin	38			39			40			•••			49			51			
(Quadrant 2)→		Q2	→ Q1	→ B11	→ Q2	→ Q1	→ Q2	→ Q1	•••	B6	→ Q2	→ Q1	→ Q2	→ Q1	→ (Quadrant 4)					
Quadrant 4	Pin	52			53			55			56		•••			65				
(Quadrant 3)→		Q2	→ Q1	→ Q2	→ Q1	→ B5	→ Q2	→ Q1	→ Q2	→ Q1	•••	B0	→ Q2	→ Q1	→ D_{OUT}					

Power Up Reset

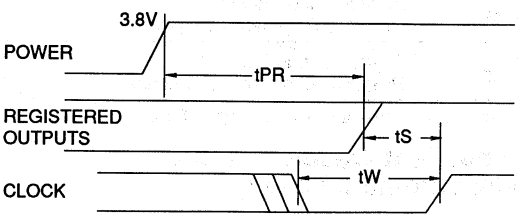
The registers in the ATV5000 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

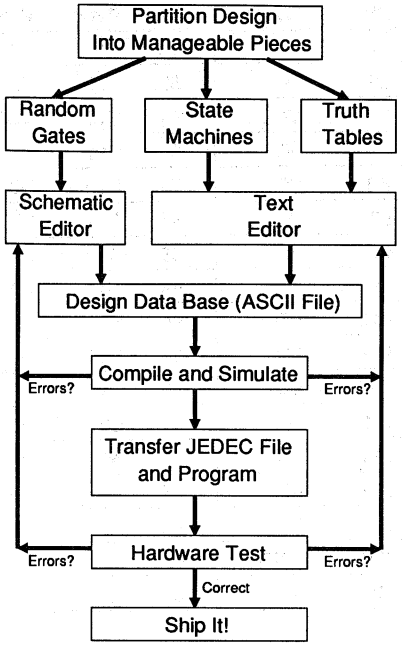
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Design Flow Diagram



Using The ATV5000

The ATV5000's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), and ISDATA (LOGiC™).

The first step in designing a device as complex as the ATV5000 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5000. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the ATV5000 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the ATV5000, and frees the designer from being required to learn all of the features of a complex device such as the ATV5000. For further information on fitters for the ATV5000, contact Atmel's EPLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an EPLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go—all in a matter of hours.

ABEL™ is a trademark of Data I/O Corporation.
CUPL™ is a trademark of Logical Devices.
LOGiC™ is a trademark of ISDATA.

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Operating Modes

	68 Lead LCC Pin								
Mode	1	2	36	34	68	66	Vcc (3,20,37,54)	I/O's	I/O Pin 65
"EPLD"	X (1)	X	X	X	X	X	5V	I/O	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}	ADD
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}	ADD
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	High Z	High Z
Preload/Observe	⎍	D_{IN}	X	X	V_H (2)	$\overline{OE}$	5V	High Z	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

ATV5000 PLCC/PGA Pin Assignments

PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name	PLCC Pin #	PGA Pin #	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	IN	19	F1	I/O	36	L6	IN	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	IN	49	H11	I/O	66	A8	IN
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	IN	51	G11	I/O	68	A7	IN

Pin Capacitance (f=1MHz T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV5000 fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

The security fuse also inhibits Preload and Observability.

Erasure Characteristics

The entire memory array of an ATV5000 is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	50	ATV5000-25JC ATV5000-25KC ATV5000-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
30	20	40	ATV5000-30JC ATV5000-30KC ATV5000-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-30KI ATV5000-30UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-30KM ATV5000-30UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-30KM/883 ATV5000-30UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5000-35JC ATV5000-35KC ATV5000-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-35KI ATV5000-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-35KM ATV5000-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-35KM/883 ATV5000-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

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Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	20	40	ATV5000L-30JC ATV5000L-30KC ATV5000L-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
35	25	33	ATV5000L-35JC ATV5000L-35KC ATV5000L-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000L-35KI ATV5000L-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000L-35KM ATV5000L-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000L-35KM/883 ATV5000L-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

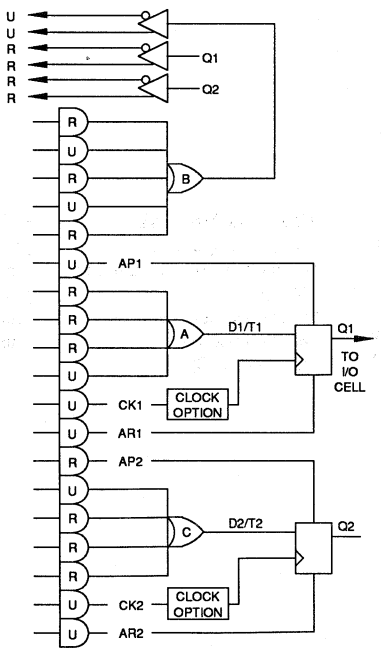
Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Using the ATV5000

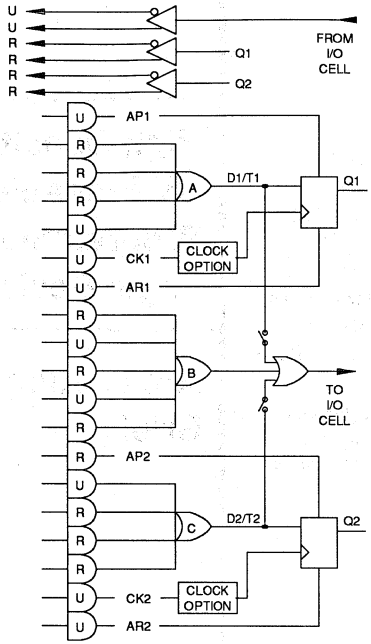
The ATV5000 Logic Cells retain the ATV2500's basic features with two registers, three sum terms and Q1, Q2, and pin feedback options. In addition, these following features make the ATV5000 even more versatile:

1. Input latches are added to every I/O pin. Each latch can be enabled or disabled independently.
2. The ATV5000 can be configured to feedback a combinatorial sum term and send Q1 to the output. Feeding the combinatorial sum term internally makes implementing logic equations with large number of product terms possible without sacrificing an I/O pin.
3. Dedicated clock pins and individual clock product terms create multiple clock options for each flip-flop.
4. The addition of the Buried Logic Cells handles more logic than ever.
5. Each flip-flop can be configured as D or T type flip-flop.
6. Asynchronous Preset, Asynchronous Reset and programmable output polarity allow registered outputs using fewer product terms.

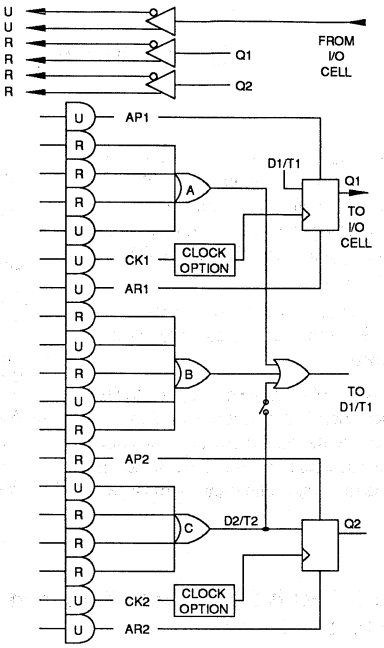
Logic Cell with Buried Sum Term and Register to I/O Cell



Logic Cell, 2 Buried Registers, Combinatorial to I/O Cell



Logic Cell with Combinable Sum Terms, Register to I/O Cell



The following are sections of ABEL and CUPL source files to illustrate how each of these features is described in the ABEL and CUPL high level description languages.

Pin and Node Assignments

All the buried registers used in the design need to be assigned node numbers. The following tables show the complete set of node numbers by quadrant.

ABEL and Atmel-ABEL

```
LENA,CLOCK pin 1,2;
ACK pin 4 istype 'reg_d,buffer';
OUTA pin 5;
DRAM node 121 istype 'reg_t';
EXPAND node 70;
ACKL node 813;
```

CUPL

```
pin 1,2 = LENA,CLOCK;
pin 4 = ACK;
pin 5 = OUTA;
pinnode 105 = DRAM;
pinnode 208 = EXPAND;
```

ATV5000 ABEL and Atmel-ABEL Node Numbers

Quadrant I

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
4	813	761	69	121
5	814	762	70	122
6	815	763	71	123
7	816	764	72	124
8	817	765	73	125
9	818	766	74	126
10	819	767	75	127
11	820	768	76	128
12	821	769	77	129
13	822	770	78	130
14	823	771	79	131
15	824	772	80	132
17	825	773	81	133

6 Buried Logic Cells
B23 - B18 node 173 - 178
LCK1 pin 1; Quadrant Latch clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
18	826	774	82	134
19	827	775	83	135
21	828	776	84	136
22	829	777	85	137
23	830	778	86	138
24	831	779	87	139
25	832	780	88	140
26	833	781	89	141
27	834	782	90	142
28	835	783	91	143
29	836	784	92	144
30	837	785	93	145
31	838	786	94	146

6 Buried Logic Cells
B17 - B12 node 179 - 184
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
38	839	787	95	147
39	840	788	96	148
40	841	789	97	149
41	842	790	98	150
42	843	791	99	151
43	844	792	100	152
44	845	793	101	153
45	846	794	102	154
46	847	795	103	155
47	848	796	104	156
48	849	797	105	157
49	850	798	106	158
51	851	799	107	159

6 Buried Logic Cells
B11 - B6 node 185 - 190
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
52	852	800	108	160
53	853	801	109	161
55	854	802	110	162
56	855	803	111	163
57	856	804	112	164
58	857	805	113	165
59	858	806	114	166
60	859	807	115	167
61	860	808	116	168
62	861	809	117	169
63	862	810	118	170
64	863	811	119	171
65	864	812	120	172

6 Buried Logic Cells
B5 - B0 node 191 - 196
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

ATV5000 CUPL Node Numbers

Quadrant I

Sum Term

Pin	A	B	C
4	157	209	105
5	156	208	104
6	155	207	103
7	154	206	102
8	153	205	101
9	152	204	100
10	151	203	99
11	150	202	98
12	149	201	97
13	148	200	96
14	147	199	95
15	146	198	94
17	145	197	93

6 Buried Logic Cells
B23 - B18 node 74 - 69
LCK1 pin 1; Quadrant Latch Clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Sum Term

Pin	A	B	C
18	158	210	106
19	159	211	107
21	160	212	108
22	161	213	109
23	162	214	110
24	163	215	111
25	164	216	112
26	165	217	113
27	166	218	114
28	167	219	115
29	168	220	116
30	169	221	117
31	170	222	118

6 Buried Logic Cells
B17 - B12 node 75 - 80
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Sum Term

Pin	A	B	C
38	183	235	131
39	182	234	130
40	181	233	129
41	180	232	128
42	179	231	127
43	178	230	126
44	177	229	125
45	176	228	124
46	175	227	123
47	174	226	122
48	173	225	121
49	172	224	120
51	171	223	119

6 Buried Logic Cells
B11 - B6 node 86 - 81
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

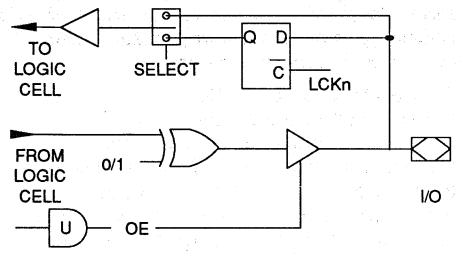
Sum Term

Pin	A	B	C
52	184	236	132
53	185	237	133
55	186	238	134
56	187	239	135
57	188	240	136
58	189	241	137
59	190	242	138
60	191	243	139
61	192	244	140
62	193	245	141
63	194	246	142
64	195	247	143
65	196	248	144

6 Buried Logic Cells
B5 - B0 node 87 - 92
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

Input Latch

Each of the 52 I/Os has an input latch that can be enabled and disabled individually. When the latch is enabled and latch clock is high, the pin value is latched. When the quadrant latch clock is low, the latch becomes transparent. When the latch is disabled, an ATV5000 I/O acts like those of the ATV750 and ATV2500 I/O's. The pin input is fed directly to the array (except when sum term B is being used as a buried feedback).



The .D and the .LE (latch enable) equations are required to enable the input latch in ABEL AHDL. The only allowed input to the latch is the IO pin with which it is associated. The only allowed .LE input is the quadrant latch clock (pin 1,34, 35, or 68). Notice that CUPL does not have node numbers for the input latches. Any pin name used in a feedback with the dot extension IOL tells CUPL that particular pin should be a latched pin.

ABEL and Atmel-ABEL	CUPL
ACKL.D = ACK;	
ACKL.LE = LENA;	
OUTA := ACKL;	OUTA.D = ACK.IOL;

Internal Combinatorial Feedback for an I/O Cell

To implement the combinatorial feedback of the B sum term, first define the node name with the corresponding node number. This node will take a 5 product term equation. Regular syntax describing a combinatorial equation will describe the B sum term.

Note: This B sum term node number is defined only when this feature is needed. When this feature is used, the output is from Q1 through an inverter/buffer. The I/O pin becomes a output-only pin. It cannot be used as an input or as an input/output.

ABEL and Atmel-ABEL	CUPL
OUTA pin 5;	pin 5 = OUTA;
EXPAND node 70;	pinnode 208 = EXPAND;
OUTA.D = INA&INB# !INC&!IND;	OUTA.D = INA&INB#!INC&!IND;
EXPAND = INA & !INC # IND;	EXPAND = INA & !INC # IND;

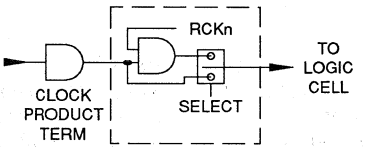
(OUTA and EXPAND are in the same I/O Logic Cell. OUTA is the Q1 output to pin after the inverter/buffer and EXPAND is the combinatorial sum term feedback. The feedbacks from this Logic Cell are Q1 before the inverter/buffer, Q2, and the B sum term)

Clocking Options

There are different methods of clocking the registers in the ATV5000. The clock options can best described as either the AND function of (Quadrant Clock & Clock Product Term) or purely the function of the Clock Product Term (like ATV750 and ATV2500).

Synchronous Operation

The quadrant clock is the only clocking element in this mode of operation. The clock product term must be defined to be equal to 1. In ABEL AHDL, .CK defines the clock product term and .CE is the corresponding quadrant clock.



In CUPL, .CE has a different implication. The keyword .CE means the user wants the AND function (Quadrant Clock & Clock Product Term) for the clock.

ABEL and Atmel-ABEL	CUPL
OUTA.CK = 1;	
OUTA.CE = CLOCK; "CLOCK is pin 2	OUTA.CE = 'B'1;

Gated Synchronous Operation

This clock option still uses the fast quadrant register clock pin, but now it has a gating element. The clock product term enables or disables the clock going to the register.

ABEL and Atmel-ABEL	CUPL
OUTA.CK = INX & INY & !INZ;	
OUTA.CE = CLOCK; "CLOCK is pin 2	OUTA.CE = INX&INY&!INZ;

Asynchronous Operation

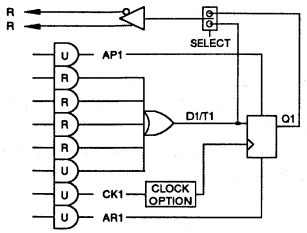
The quadrant clock has no effect on the register in this mode of clock option. The register is clocked by the clock product term like the ATV750 and ATV2500 registers.

ABEL and Atmel-ABEL	CUPL
OUTA.CK = INA & !INB & INC;	OUTA.CK = INA & !INB & INC;

8

Buried Logic Cells

There are 6 Buried Logic Cells in each quadrant. Every Buried Logic Cell can be configured as a buried register or as a combinatorial feedback to the quadrant array. In the buried register mode, it's used the same way as Q1 and Q2. In the combinatorial feedback mode, it's used the same way as the B sum term feedback.



ABEL and Atmel-ABEL	CUPL
ADDR,XDATA node 173,174;	pinnode 74,73 = ADDR,XDATA;
ADDR = A16&A15&!A14#RST;	ADDR = A16&A15&!A14#RST;
XDATA.T = !A16 & RST;	XDATA.T = !A16 & RST;
XDATA.CK = INA & INC;	XDATA.CK = INA & INC;
XDATA.AR = INB;	XDATA.AR = INB;

D-Type and T-type Registers

All the registers in the ATV5000 can be configured as D or T type. The ISTYPE statement after the PIN or NODE definition in ABEL AHDL tells ABEL which type of register is needed.

ABEL and Atmel-ABEL	CUPL
ABC node 123 istype 'reg_t';	pinnode 103 = ABC;
XYZ pin 7 istype 'reg_d';	pin 7 = XYZ;
ABC.T = INA & INB # INC;	ABC.T = INA & INB # INC;
XYZ.D = !INA # INC;	XYZ.D = !INA # INC;

In both languages, the .T extension is reserved for T flip-flop and .D extension for D flip-flop.

Asynchronous Preset

One of the advantanges of having a programmable output polarity I/O is that the same combinatorial output often take fewer product terms to implement using negative logic rather than positive logic or vice versa.

The same can be done for a registered output provided the power-up state is not crucial (all flip-flops are reset upon power up). With an Asynchronous Preset and an Asynchronous Reset, simply swap the two product terms and invert your equation and polaritywill let you take advantage of expressing the same logic in a different polarity. The following example shows a 4 to 1 reduction in product term requirement.

ABEL and Atmel-ABEL	CUPL
OUTC pin 8 istype 'invert,reg_d';	pin 8 = OUTC;
OUTD pin 9 istype 'buffer,reg_d';	pin 9 = !OUTD;
OUTC.D = INA# !INB#INC# !IND;	OUTC.D = INA#!INB#INC#!IND;
OUTC.CK = CLK;	OUTC.CK = CLK;
OUTC.AR = !INA & RST;	OUTC.AR = !INA & RST;
OUTC.AP = INB & PRESET;	OUTC.AP = INB & PRESET;
OUTD.D = !INA&INB&!INC&IND;	OUTD.D = !INA&INB&!INC&IND;
OUTD.CK = CLK;	OUTD.CK = CLK;
OUTD.AR = INB & PRESET;	OUTD.AR = INB & PRESET;
OUTD.AP = !INA & RST;	OUTD.AP = !INA & RST;

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Example ABEL Description File

```
module V5000;
title       'Demo ATV5000 features with ATMEL-ABEL (IBM386 or compatible)
            ATMEL Corporation EPLD      Joe Yu                  April 28, 1991'
V5K device 'P5000';

"   The IOs, registers, latches, inputs, and combinatorial sum terms feedbacks are named with the
"   following prefixes for clarity:

"   Prefix
"   I       -   Quadrant Clocks, Latch Enables.
"   IO      -   IO pins
"   IL      -   Input Latches
"   BLC     -   Buried Logic Cells
"   STF     -   Sum Term Feedbacks

"   Valid ABEL AHDL identifiers can be used in place of them.

declarations

I1 pin 1;       " Quadrant 1  Latch Enable/Input
I2 pin 2;       " Quadrant 1  Synchronous Register Clock/Input

I32 pin 32;     " Quadrant 2 Synchronous Register Clock/Input
I34 pin 34;     " Quadrant 2 Latch Enable/Input

I35 pin 35;     " Quadrant 3 Latch Enable/Input
I36 pin 36;     " Quadrant 3 Synchronous Register Clock/Input

I66 pin 66;     " Quadrant 4 Synchronous Register Clock/Input
I68 pin 68;     " Quadrant 4 Latch Enable/Input

"     **** Quadrant I ****

" I/O LOGIC CELL
" ===============
IO4,IO5,IO6,IO7,IO8,IO9                         pin 4,5,6,7,8,9 istype 'buffer,reg_d';
STF4,STF5,STF6,STF7,STF8,STF9                   node 69,70,71,72,73,74;
IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1             node 761,762,763,764,765,766 ;
IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2             node 121,122,123,124,125,126 ;

IO10,IO11,IO12,IO13,IO14,IO15,IO17              pin 10,11,12,13,14,15,17 istype 'buffer,reg_d';
STF10,STF11,STF12,STF13,STF14,STF15,STF17       node 75,76,77,78,79,80,81;
IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1  node 767,768,769,770,771,772,773 ;
IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2  node 127,128,129,130,131,132,133 ;

" INPUT LATCHES
" ===============
IL4,IL5,IL6,IL7,IL8,IL9                         node 813,814,815,816,817,818;
IL10,IL11,IL12,IL13,IL14,IL15,IL17              node 819,820,821,822,823,824,825;

" BURIED LOGIC CELL
" ================
BLC18,BLC19,BLC20,BLC21,BLC22,BLC23             node 178,177,176,175,174,173 ;

declarations " **** Quadrant II ****

" I/O LOGIC CELL
" ==============
IO18,IO19,IO21,IO22,IO23,IO24                   pin 18,19,21,22,23,24 istype 'buffer,reg_d';
STF18,STF19,STF21,STF22,STF23,STF24             node 82,83,84,85,86,87;
IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1       node 774,775,776,777,778,779;
IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2       node 134,135,136,137,138,139;

IO25,IO26,IO27,IO28,IO29,IO30,IO31              pin 25,26,27,28,29,30,31 ISTYPE 'BUFFER';
STF25,STF26,STF27,STF28,STF29,STF30,STF31       node 88,89,90,91,92,93,94;
IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1  node 780,781,782,783,784,785,786 ;
IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2  node 140,141,142,143,144,145,146 ;

" INPUT LATCHES
" ===============
IL18,IL19,IL21,IL22,IL23,IL24                   node 826,827,828,829,830,831;
IL25,IL26,IL27,IL28,IL29,IL30,IL31              node 832,833,834,835,836,837,838;
```

```
" BURIED LOGIC CELL
" ==================
BLC12,BLC13,BLC14,BLC15,BLC16,BLC17                    node 184,183,182,181,180,179;

declarations " **** Quadrant III ****

" I/O LOGIC CELL
"==============
IO38,IO39,IO40,IO41,IO42,IO43                          pin 38,39,40,41,42,43;
STF38,STF39,STF40,STF41,STF42,STF43                    node 95,96,97,98,99,100;
IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1              node 787,788,789,790,791,792;
IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2              node 147,148,149,150,151,152 istype 'reg_t';

IO44,IO45,IO46,IO47,IO48,IO49,IO51                     pin 44,45,46,47,48,49,51;
STF44,STF45,STF46,STF47,STF48,STF49,STF51              node 101,102,103,104,105,106,107;
IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1       node 793,794,795,796,797,798,799;
IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2       node 153,154,155,156,157,158,159;

" INPUT LATCHES
" ==============
IL38,IL39,IL40,IL41,IL42,IL43                          node 839,840,841,842,843,844;

IL44,IL45,IL46,IL47,IL48,IL49,IL51                     node 845,846,847,848,849,850,851;

" BURIED LOGIC CELL
" ==================
BLC6,BLC7,BLC8,BLC9,BLC10,BLC11                        node 190,189,188,187,186,185 ISTYPE 'REG_D';

declarations " **** Quadrant IV ****

" I/O LOGIC CELL
" ==============
IO52,IO53,IO55,IO56,IO57,IO58                          pin 52,53,55,56,57,58 istype 'buffer';
STF52,STF53,STF55,STF56,STF57,STF58                    node 108,109,110,111,112,113;
IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1              node 800,801,802,803,804,805;
IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2              node 160,161,162,163,164,165;

IO59,IO60,IO61,IO62,IO63,IO64,IO65                     pin 59,60,61,62,63,64,65 istype 'buffer';
STF59,STF60,STF61,STF62,STF63,STF64,STF65              node 114,115,116,117,118,119,120;
IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1       node 806,807,808,809,810,811,812;
IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2       node 166,167,168,169,170,171,172;

" INPUT LATCHES
" ==============
IL52,IL53,IL55,IL56,IL57,IL58                          node 852,853,854,855,856,857;
IL59,IL60,IL61,IL62,IL63,IL64,IL65                     node 858,859,860,861,862,863,864;

" BURIED LOGIC CELL
" ==================
BLC0,BLC1,BLC2,BLC3,BLC4,BLC5                          node 196,195,194,193,192,191;

    H,L,C,D,K,U,X,Z = 1,0,.C.,.D.,.K.,.U.,.X.,.Z.;

"    MACRO (INPUT LATCH)
INPUT_LATCH MACRO (IL,IO,QUAD_LE)
{?IL.D  =   ?IO;
?IL.LE  =   ?QUAD_LE;}

equations
"                   INPUT LATCH
"   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high, the pin value is latched.
"   When the quadrant latch clock is low, the latch becomes transparent.

IL4.D   =   IO4;    "The .D and the .LE (latch enable) extentions are  required to describe a latch in
IL4.LE  =   I1;     "ABEL AHDL. The only allowed input to he latch is the IO pin it associates with.The
                    "only allowed .LE input is the quadrant latch enable. They are Pin 1, 34, 35, and 68.

"   INPUT_LATCH macro is another way to describe the latch.
INPUT_LATCH (IL5,IO5,I1);   "Latch Pin 5
INPUT_LATCH (IL6,IO6,I1);   "Latch Pin 6

IO4.d   =   !IO4.fb;  " When .oe is enabled by IO8, IO4 outputs a 1 bit counter.
IO4.oe  =   IO8;      " When .oe is disabled by !IO8, IO4 latches a data bit  from the bus.
IO4.ck  =   1;
IO4.ce  =   I2;
```

```
IO7 =   IL4;

test_vectors ( "Test the latches...
[I1,I2,IO8,IO4]-[IO4,IO7])
[ 0, 0,   1,  X  ]  ->  [   0,  0  ];  "Transparent
[ 0, C,   1,  X  ]  ->  [   1,  1  ];  "Transparent
[ U, 0,   0,  0  ]  ->  [   Z,  0  ];  "Disable .oe and latch 0
[ 1, C,   1,  X  ]  ->  [   0,  0  ];  "Latched 0
[ 1, C,   1,  X  ]  ->  [   1,  0  ];  "Latched 0
[ D, C,   1,  X  ]  ->  [   0,  0  ];  "Transparent
[ 0, C,   1,  X  ]  ->  [   1,  1  ];  "Transparent
[ 0, C,   1,  X  ]  ->  [   0,  0  ];  "Transparent
[ U, 0,   0,  1  ]  ->  [   Z,  1  ];  "Disable .oe and latch 1
[ 1, 0,   1,  X  ]  ->  [   0,  1  ];  "Latched 1
[ 1, C,   1,  X  ]  ->  [   1,  1  ];  "Latched 1
[ 1, C,   1,  X  ]  ->  [   0,  1  ];  "Latched 1

equations
"     CLOCKING OPTIONS
"     There are different methods of clocking the registers in the ATV5000. The clock is best described as either
"     the AND function of (Quadrant Clock & Clock Product term) or the product term by it self. In the following
"     examples the register can be a name from a pin, Q1, Q2, or Buried Logic Cell. The register can be either .t or
"     .d flip-flop.

IO22.d  =   !IO22.fb;
IO22.ck =   IO18 & !IO19;     "Note there is no .ce equation defined.This is an asynchronous clocking method
IO22.ar =   IO21;             "where the quadrant clock  has no effect.

test_vectors (
[IO18,IO19,IO21 ]   ->  [  IO22 ])
[   0,  0,  1   ]   ->  [   0   ];
[   0,  0,  0   ]   ->  [   0   ];
[   C,  0,  0   ]   ->  [   1   ];
[   C,  0,  0   ]   ->  [   0   ];

equations
IO23.d  =   !IO23.fb;
IO23.ck =   IO18 & !IO19;     "The clock product term (.ck) is used to gate the quadrant clock pin.
IO23.ce =   I32;              "Using quadrant clock pin in a synchronous mode allows higher clock rate.
IO23.ar =   IO21;             "Pin 32 is the Quadrant 2 clock pin.

test_vectors (
[I32,IO18,IO19,IO21   ]   ->  [  IO23 ])
[   0,  1,  0,  1   ]   ->  [   0   ];
[   C,  0,  0,  0   ]   ->  [   0   ]; "Product term blocks quadrant clock
[   C,  1,  0,  0   ]   ->  [   1   ]; "Product term enables quadrant clock
[   C,  1,  0,  0   ]   ->  [   0   ];

equations
IO24.d  =   !IO24.fb;
IO24.ck =   1;          "Note that the .ck is defined to 1. The quadrant clock is the only clocking element.
IO24.ce =   I32;        "The .ce is Pin 32 because it's the proper quadrant clock to use for synchronous
IO24.ar =   IO21;       "operation.

test_vectors (
[  I32,  IO21 ]   ->  [  IO24 ])
[   0,   1    ]   ->  [   0   ];
[   C,   0    ]   ->  [   1   ];
[   C,   0    ]   ->  [   0   ];
[   C,   0    ]   ->  [   1   ];

"     D-TYPE and T-TYPE REGISTERS
"     All the registers in the ATV5000 can be configured as D or T type. The ISTYPE statement after the PIN
"     or NODE definition tells ABEL which type of register is needed.

"     ABC     node    122 istype 'reg_t';
"     XYZ     pin     5 istype 'reg_d';

"     Use the .t extension for ABC and .d extension for XYZ when you write the equations.

equations
" 3 Bit Synchronous Counter using T flip-flops

IO38Q2.t = 1;       IO38Q2.ck = 1;      IO38Q2.ce = I36;    IO38Q2.ar = IO38;
```

```
IO39Q2.t = IO38Q2;                IO39Q2.ck = 1;          IO39Q2.ce = I36;      IO39Q2.ar = IO38;
IO40Q2.t = IO38Q2 & IO39Q2;       IO40Q2.ck = 1;          IO40Q2.ce = I36;      IO40Q2.ar = IO38;

test_vectors (
[ I36, IO38 ]   ->  [ IO40Q2,IO39Q2,IO38Q2])
[   0,  1   ]   ->  [   0,   0,   0   ];
[   C,  0   ]   ->  [   0,   0,   1   ];
[   C,  0   ]   ->  [   0,   1,   0   ];
[   C,  0   ]   ->  [   0,   1,   1   ];
[   C,  0   ]   ->  [   1,   0,   0   ];
[   C,  0   ]   ->  [   1,   0,   1   ];
[   C,  0   ]   ->  [   1,   1,   0   ];
[   C,  0   ]   ->  [   1,   1,   1   ];
[   C,  0   ]   ->  [   0,   0,   0   ];

equations
" 3 Bit Synchronous Counter using D flip-flops

BLC6.d = !BLC6;                   BLC6.ck = 1;            BLC6.ce = I36;        BLC6.ar = IO38;
BLC7.d = BLC6 $ BLC7;             BLC7.ck = 1;            BLC7.ce = I36;        BLC7.ar = IO38;
BLC8.d = BLC8 $ (BLC6 & BLC7);    BLC8.ck = 1;            BLC8.ce = I36;        BLC8.ar = IO38;

test_vectors (
[ I36, IO38 ]   ->  [BLC8,BLC7,BLC6])
[   0,  1   ]   ->  [   0,   0,   0   ];
[   C,  0   ]   ->  [   0,   0,   1   ];
[   C,  0   ]   ->  [   0,   1,   0   ];

[   C,  0   ]   ->  [   0,   1,   1   ];
[   C,  0   ]   ->  [   1,   0,   0   ];
[   C,  0   ]   ->  [   1,   0,   1   ];
[   C,  0   ]   ->  [   1,   1,   0   ];
[   C,  0   ]   ->  [   1,   1,   1   ];
[   C,  0   ]   ->  [   0,   0,   0   ];

"       UNIVERSAL AND REGIONAL PRODUCT TERMS
"   A Regional product term has inputs from all the feedbacks of its quadrant Buried Logic Cells, Q1's, Q2's,
"   and the dedicated Inputs. In addition, a Universal product term has the Pin/B Sum Term Feedbacks.

"       OUTPUTS and FEEDBACKS
"   Combinatorial:
"   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or 13 product terms
"   depending on the need of the reduced equation. If the reduced equation requires 5 or less product terms,
"   it leaves Q1 and Q2 each with 4 product terms to use.

"       IO52            =   up to 5 PRODUCT TERMS (2 UNIVERSAL)
"       IO52.oe         =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.(d or t) =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"       IO52Q1.ck       =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.ce       =   QUADRANT CLOCK
"       IO52Q1.ar       =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.ap       =   1 PRODUCT TERM (1 UNIVERSAL)

"       IO52Q2.(d or t) =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"       IO52Q2.ck       =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce       =   QUADRANT CLOCK
"       IO52Q2.ar       =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ap       =   1 PRODUCT TERM (0 UNIVERSAL)

"   ALLOWED FEEDBACKS:          SOURCE:
"   IO52,IO52.PIN               --  Pin feedback, after the buffer/inverter.
"   IO52Q1,IO52Q1.FB,IO52Q1.Q   --  Q1 register feedback.
"   IO52Q2,IO52Q2.FB,IO52Q2.Q   --  Q2 register feedback.

"   Combinatorial:
"   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product terms to use. Q1 will
"   feedback the A Sum Term portion of the output logic.

"       IO52            =   up to 9 PRODUCT TERMS (3 UNIVERSAL)
"       IO52.oe         =   1 PRODUCT TERM (1 UNIVERSAL)

"       IO52Q2.(d or t) =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"       IO52Q2.ck       =   1 PRODUCT TERM (1 UNIVERSAL)

"       IO52Q2.ce       =   QUADRANT CLOCK
```

```
"     IO52Q2.ar      =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52Q2.ap      =   1 PRODUCT TERM (0 UNIVERSAL)

"   ALLOWED FEEDBACKS:              SOURCE:
"   IO52,IO52.PIN                --  Pin feedback, after the buffer/inverter.
"   IO52Q2,IO52Q2.FB,IO52Q2.Q    --  Q2 register feedback.

"   Combinatorial:
"   If the reduced equation requires more than 9 product terms, it leaves no product terms for Q1 and Q2. Q1
"   feeds back A Sum Term and Q2 feeds back C Sum Term.
"     IO52           =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
"     IO52.oe        =   1 PRODUCT TERM (1 UNIVERSAL)

"   ALLOWED FEEDBACKS:              SOURCE:
"   IO52,IO52.PIN                --  Pin feedback, after the buffer/inverter.

"   Registered:
"   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or 13 product terms
"   depending on the need of the reduced equation. If the reduced equation requires 4 or less product terms, you
"   may define a 5 product term equation for the STF (Sum Term Feedback) and define a 4 product term
"   equation for Q2.

"     IO52.(d or t)  =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"     IO52.oe        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ck        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ce        =   QUADRANT CLOCK
"     IO52.ar        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ap        =   1 PRODUCT TERM (1 UNIVERSAL)

"     STF52          =   up to 5 PRODUCT TERMS (2 UNIVERSAL)

"     IO52Q2.(d or t)=   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"     IO52Q2.ck      =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52Q2.ce      =   QUADRANT CLOCK
"     IO52Q2.ar      =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52Q2.ap      =   1 PRODUCT TERM (0 UNIVERSAL)

"   ALLOWED FEEDBACKS:              SOURCE:
"   IO52.FB,IO52.Q               --  Register feedback prior to buffer/inverter.
"   IO52Q2,IO52Q2.FB,IO52Q2.Q    --  Q2 register feedback.
"   STF52                        --  Sum Term Feedback for logic expansion.

"   Registered:
"   If the reduced equation requires 9 to 5 product terms, you may write a 4 product term equation for Q2.

"     IO52.(d or t)  =   up to 9 PRODUCT TERMS (3 UNIVERSAL)
"     IO52.oe        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ck        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ce        =   QUADRANT CLOCK
"     IO52.ar        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ap        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52Q2.(d or t)=   up to 4 PRODUCT TERMS (1 UNIVERSAL)

"     IO52Q2.ck      =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52Q2.ce      =   QUADRANT CLOCK
"     IO52Q2.ar      =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52Q2.ap      =   1 PRODUCT TERM (0 UNIVERSAL)

"   ALLOWED FEEDBACKS:              SOURCE:
"   IO52,IO52.PIN                --  Pin feedback, after the buffer/inverter.
"   IO52.FB,IO52.Q               --  Register feedback prior to buffer/inverter.
"   IO52Q2,IO52Q2.FB,IO52Q2.Q    --  Q2 register feedback.

"   Registered:
"   If the reduced equation requires more than 9 product terms, it leaves zero product terms for Q1 and Q2.

"     IO52.(d or t)  =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
"     IO52.oe        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ck        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ce        =   QUADRANT CLOCK
"     IO52.ar        =   1 PRODUCT TERM (1 UNIVERSAL)
"     IO52.ap        =   1 PRODUCT TERM (1 UNIVERSAL)

"   ALLOWED FEEDBACKS:              SOURCE:
```

```
"    IO52,IO52.PIN          --    Pin feedback, after the buffer/inverter.
"    IO52.FB,IO52.Q         --    Register feedback prior to buffer/inverter.

"         AP, AR, and CK
"    Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous Reset) and .CK. All
"    ARs and CKs are Universal product terms. The APs are Universal product terms except the APs for Q2.
"    NOTE:  AP and AR should never be active at the same time.

equations
IO10.d  =   !IO10.fb;
IO10.ck =   IO8;
IO10.ar =   IO11;
IO10.ap =   IO12;

test_vectors (
[ IO8, IO11, IO12 ]   ->  [  IO10 ])
[    0,   1,   0  ]   ->  [    0   ]; "AR
[    0,   0,   0  ]   ->  [    0   ];
[    C,   0,   0  ]   ->  [    1   ];
[    C,   0,   0  ]   ->  [    0   ];
[    0,   0,   1  ]   ->  [    1   ]; "AP
[    0,   1,   0  ]   ->  [    0   ]; "AR

"         BURIED LOGIC CELLS
"    Buried Logic Cell can be configured as a register feedback like Q2. It can also be configured as
"    combinatorial feedback to accommodate for logic expansion.

equations
BLC17.t    =   1;   "Registered
BLC17.ck   =   IO9;
BLC17.ar   =   IO21;

BLC14      =   I1;  "Combinatiorial

IO25       =   BLC17;
IO26       =   BLC14;

test_vectors (
[IO9,  IO21,  I1   ]   ->  [ BLC17,BLC14,IO25,IO26])
[    0,   1,   0   ]   ->  [    0,   0,   0,  0 ];
[    C,   0,   0   ]   ->  [    1,   0,   1,  0 ];
[    0,   0,   1   ]   ->  [    1,   1,   1,  1 ];
[    C,   0,   1   ]   ->  [    0,   1,   0,  1 ];
[    C,   0,   0   ]   ->  [    1,   0,   1,  0 ];

END;
```

Example CUPL Description File

```
Name     V5K;
Partno   NA;
Date     7/22/91;
Revision 01;
Designer Joe Yu;
Company  ATMEL Corporation;
Assembly NA;
Location U1;
Device   V5000;
Format   j;

/* Compiled with CUPL 386 version */

/*  The IOs, registers, inputs, and combinatorial sum terms feedbacks are named with the following prefixes
 *  for clarity:

 *  Prefix
 *  I      -   Quadrant Clocks, Latch Enables.
 *  IO     -   IO pins
 *  BLC    -   Buried Logic Cells
 *  STF    -   Sum Term Feedbacks

 *  Valid CUPL HDL identifiers can be used in place of them. */

pin 1   =  I1;    /* Quadrant 1   Latch Enable/Input                */
pin 2   =  I2;    /* Quadrant 1   Synchronous Register Clock/Input  */

pin 32  =  I32;   /* Quadrant 2   Synchronous Register Clock/Input  */
pin 34  =  I34;   /* Quadrant 2   Latch Enable/Input                */

pin 35  =  I35;   /* Quadrant 3   Latch Enable/Input                */
pin 36  =  I36;   /* Quadrant 3   Synchronous Register Clock/Input  */

pin 66  =  I66;   /* Quadrant 4   Synchronous Register Clock/Input  */
pin 68  =  I68;   /* Quadrant 4   Latch Enable/Input                */

          /**** Quadrant I ****/

/* I/O LOGIC CELL   */
/* ==============  */

pin      [4..9]       =  [IO4..9];
pinnode  [209..204]   =  [STF4..9];
pinnode  [157..152]   =  [IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1];
pinnode  [105..100]   =  [IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2];

pin      [10..15,17]  =  [IO10..15,IO17];
pinnode  [203..197]   =  [STF10..15,STF17];
pinnode  [151..145]   =  [IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1];
pinnode  [99..93]     =  [IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2];

/* BURIED LOGIC CELL  */
/* ================  */

pinnode  [69..74]     =  [BLC18..23];

          /**** Quadrant II ****/

/* I/O LOGIC CELL   */
/* ==============  */

pin      [18,19,21..24] =  [IO18,IO19,IO21..24];
pinnode  [210..215]     =  [STF18,STF19,STF21..24];
pinnode  [158..163]     =  [IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1];
pinnode  [106..111]     =  [IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2];
pin      [25..31]       =  [IO25..31];
pinnode  [216..222]     =  [STF25..31];
pinnode  [164..170]     =  [IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1];
pinnode  [112..118]     =  [IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2];

/* BURIED LOGIC CELL  */
/* ================  */
```

```
pinnode [80..75]     =   [BLC12..17];
                /**** Quadrant III ****/
/* I/O LOGIC CELL   */
/* ==============  */

pin     [38..43]     =   [IO38..43];
pinnode [235..230]   =   [STF38..43];
pinnode [183..178]   =   [IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1];
pinnode [131..126]   =   [IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2];

pin     [44..49,51]  =   [IO44..49,IO51];
pinnode [229..223]   =   [STF44..49,STF51];
pinnode [177..171]   =   [IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1];
pinnode [125..119]   =   [IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2];

/* BURIED LOGIC CELL */
/* ================= */

pinnode [81..86]     =   [BLC6..11];
                /**** Quadrant IV ****/

/* I/O LOGIC CELL   */
/* ==============  */

pin     [52,53,55..58] = [IO52,IO53,IO55..58];
pinnode [236..241]   =   [STF52,STF53,STF55..58];
pinnode [184..189]   =   [IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1];
pinnode [132..137]   =   [IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2];

pin     [59..65]     =   [IO59..65];
pinnode [242..248]   =   [STF59..65];
pinnode [190..196]   =   [IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1];
pinnode [138..144]   =   [IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2];

/* BURIED LOGIC CELL */
/* ================= */

pinnode [92..87]     =   [BLC0..5];

/*          INPUT LATCH
    Each of the 52 I/Os has an input latch. When the quadrant latch enable is high, the pin value is latched.
    When the quadrant latch clock is low, the latch becomes transparent.                    */

IO4.d   =   !IO4;
IO4.oe  =   IO8.io;
IO4.ce  =   'B'1;

IO7     =   IO4.IOL;    /*  When the latched input is needed in the design, i.e.. IO4.IOL, IO4 is configured as
                            having a latched input.         */

/*          CLOCKING OPTIONS
    There are different methods of clocking the registers in the ATV5000. The clock is best described as either
    the AND function of (Quadrant Clock & Clock Product term) or the product term by it self. In the following
    examples the register can be a name from a pin, Q1, Q2, or Buried Logic Cell. The register can be either
    .t or .d flip-flop.  */

IO22.d  =   !IO22;
IO22.ck =   IO18 & !IO19;   /* Note there is no .ce equation defined. This is an asynchronous clocking     */
IO22.ar =   IO21;           /* method where the quadrant clock has no effect.                              */

IO23.d  =   !IO23;
IO23.ce =   IO18 & !IO19;   /* The clock product term is used to gate the quadrant clock pin.Using         */
IO23.ar =   IO21;           /* quadrant clock pin in a synchronous mode allows higher clock rate. Pin      */
                            /* 32 is the Quadrant 2 clock pin.                                             */
IO24.d  =   !IO24;
IO24.ce =   'B'1;           /* Note that the .ce is defined to 1. The quadrant clock is the only clocking  */
IO24.ar =   IO21;           /* element. The clock is Pin 32 because it's the proper quadrant clock to use  */
                            /* for synchronous operation.                                                  */

/*          D-TYPE and T-TYPE REGISTERS
    All the registers in the ATV5000 can be configured as D or T type. Use the .d extension for D type
    register and .t extension for T type register.                                          */
/* 3 Bit Synchronous Counter using T flip-flops */
```

```
IO38Q2.t = 'B'1;          IO38Q2.ce = 'B'1;          IO38Q2.ar = IO38;
IO39Q2.t = IO38Q2;        IO39Q2.ce = 'B'1;          IO39Q2.ar = IO38;
IO40Q2.t = IO38Q2 & IO39Q2;  IO40Q2.ce = 'B'1;       IO40Q2.ar = IO38;

/* 3 Bit Synchronous Counter using D flip-flops */

BLC6.d = !BLC6;                 BLC6.ce = 'B'1;     BLC6.ar = IO38;
BLC7.d = BLC6 $ BLC7;           BLC7.ce = 'B'1;     BLC7.ar = IO38;
BLC8.d = BLC8 $ (BLC6 & BLC7);  BLC8.ce = 'B'1;     BLC8.ar = IO38;

/*      UNIVERSAL AND REGIONAL PRODUCT TERMS
A Regional product term has inputs from all the feedbacks of its quadrant Buried Logic Cells, Q1's, Q2's,
and the dedicated Inputs. In addition, a Universal product term has the Pin/B Sum Term Feedbacks.   */

/*          OUTPUTS and FEEDBACKS
Combinatorial:
Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or 13 product terms
depending on the need of the reduced equation. If the reduced equation requires 5 or less product terms,
it leaves Q1 and Q2 each with 4 product terms to use.

    IO52            =  up to 5 PRODUCT TERMS (2 UNIVERSAL)
    IO52.oe         =  1 PRODUCT TERM (1 UNIVERSAL)

    IO52Q1.(d or t) =  up to 4 PRODUCT TERMS (1 UNIVERSAL)
    IO52Q1.(ck or ce) = 1 PRODUCT TERM (1 UNIVERSAL)

    IO52Q1.ar       =  1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q1.ap       =  1 PRODUCT TERM (1 UNIVERSAL)

    IO52Q2.(d or t) =  up to 4 PRODUCT TERMS (1 UNIVERSAL)
    IO52Q2.(ck or ce) = 1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ar       =  1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ap       =  1 PRODUCT TERM (0 UNIVERSAL)

ALLOWED FEEDBACKS:    SOURCE:
IO52,IO52.IO  --      Pin feedback, after the buffer/inverter.
IO52Q1        --      Q1 register feedback.
IO52Q2        --      Q2 register feedback.      */

/*  Combinatorial:
If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product terms to use. Q1
will feedback the A Sum Term portion of the output logic.

    IO52            =  up to 9 PRODUCT TERMS (3 UNIVERSAL)
    IO52.oe         =  1 PRODUCT TERM (1 UNIVERSAL)

    IO52Q2.(d or t) =  up to 4 PRODUCT TERMS (1 UNIVERSAL)
    IO52Q2.(ck or ce) = 1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ar       =  1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ap       =  1 PRODUCT TERM (0 UNIVERSAL)

ALLOWED FEEDBACKS:    SOURCE:
IO52,IO52.IO  --      Pin feedback, after the buffer/inverter.
IO52Q2        --      Q2 register feedback.      */

/*  Combinatorial:
If the reduced equation requires more than 9 product terms, it leaves no product terms for Q1 and Q2.
Q1 feeds back A. Sum Term and Q2 feeds back C Sum Term.

    IO52            =  up to 13 PRODUCT TERMS (4 UNIVERSAL)
    IO52.oe         =  1 PRODUCT TERM (1 UNIVERSAL)

ALLOWED FEEDBACKS:    SOURCE:
IO52,IO52.IO  --      Pin feedback, after the buffer/inverter.      */
/*  Registered:
Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or 13 product terms
depending on the need of the reduced equation. If the reduced equation requires 4 or less product terms,
you may define a 5 product term equation for the STF (Sum Term Feedback) and define a 4 product
term equation for Q2.

    IO52.(d or t)   =  up to 4 PRODUCT TERMS (1 UNIVERSAL)
    IO52.oe         =  1 PRODUCT TERM (1 UNIVERSAL)
    IO52.(ck or ce) =  1 PRODUCT TERM (1 UNIVERSAL)
    IO52.ar         =  1 PRODUCT TERM (1 UNIVERSAL)
    IO52.ap         =  1 PRODUCT TERM (1 UNIVERSAL)
```

```
    STF52    = up to 5 PRODUCT TERMS (2 UNIVERSAL)

    IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
    IO52Q2.(ck or ce) =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)

  ALLOWED FEEDBACKS:      SOURCE:
  IO52              --    Register feedback prior to buffer/inverter.
  IO52Q2            --    Q2 register feedback.
  STF52             --    Sum Term Feedback for logic expansion.          */

/*  Registered:
    If the reduced equation requires 9 to 5 product terms, you may write a 4 product term equation for Q2.

    IO52.(d or t)     =   up to 9 PRODUCT TERMS (3 UNIVERSAL)

    IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52.(ck or ce)   =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52.ar           =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52.ap           =   1 PRODUCT TERM (1 UNIVERSAL)

    IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
    IO52Q2.(ck or ce) =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)

  ALLOWED FEEDBACKS:      SOURCE:
  IO52.IO           --    Pin feedback, after the buffer/inverter.
  IO52              --    Register feedback prior to buffer/inverter.
  IO52Q2            --    Q2 register feedback.           */

/*  Registered:
    If the reduced equation requires more than 9 product terms, it leaves zero product terms for Q1 and Q2.

    IO52.(d or t)     =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
    IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52.(ck or ce)   =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52.ar           =   1 PRODUCT TERM (1 UNIVERSAL)
    IO52.ap           =   1 PRODUCT TERM (1 UNIVERSAL)

  ALLOWED FEEDBACKS:      SOURCE:
  IO52.IO           --    Pin feedback, after the buffer/inverter.
  IO52              --    Register feedback prior to buffer/inverter.     */

/*          AP, AR, and CK
    Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous Reset) and .CK or .CE.
    All ARs and CKs are Universal product terms. The APs are Universal product terms except the APs for Q2.
    NOTE:  AP and AR should never be active at the same time.           */

IO10.d  =  !IO10;
IO10.ck =  IO8;
IO10.ar =  IO11;
IO10.ap =  IO12;

/*          BURIED LOGIC CELLS
    Buried Logic Cell can be configured as a register feedback like Q2. It can also be configured as
    combinatorial feedback to accommodate for logic expansion.         */

BLC17.t   =  'B'1;    /*Registered */
BLC17.ck  =  IO9;
BLC17.ar  =  IO21;

BLC14     =  I1;  /*Combinatiorial */

IO25      =  BLC17;
IO26      =  BLC14;

END;
```

CMOS Programmable Multi-function PLD (42 x 105 x 12)

Features

- High-speed EPROM-based CMOS Multi-Function PLD
- Two Fully Programmable Arrays Eliminate "P-term Depletion"
  - Up to 64 P-terms per OR Function
- Improved Output Macro Cell Structure
  - Individually Programmable as:
    - Registered Output with Feedback
    - Registered Input
    - Combinatorial I/O with Buried Register
    - Dedicated I/O with Feedback
    - Dedicated Input (Combinatorial)
  - Bypassed Registers are 100% Functional with Separate Input and Feedback Paths
  - Individual Output Enable Control Functions
    - From pin or AND Array
- Eleven Clock Sources
- Register Preload and Diagnostic Test Mode Features
- Security Fuse
- Second Source to Signetic's PLC42VA12

Description

The new ATS42VA12 CMOS PLD from Atmel exhibits a unique combination of the two architectural concepts that revolutionized the PLD marketplace.

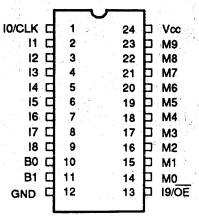
The unique Output Macro Cell (OMC) embodies all the advantages and none of the disadvantages associated with the "V" type Output Macro Cell devices. This new design, combined with added functionality of two programmable arrays, represents a significant advancement in the configurability and efficiency of multi-function PLDs.

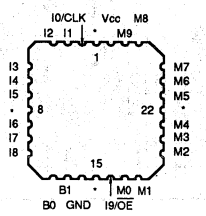
The most significant improvement in the Output Macro Cell structure is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other "V" type devices, the register in the ATS42VA12 Macro Cell remains fully functional as a buried register. Both the combinatorial I/O and buried register have separate input paths (from the AND array). In most V-type architectures, the register is lost as a resource when the cell is configured as a combinatorial I/O. This feature provides the capability to operate the buried register independently from the combinatorial I/O.

The ATS42VA12 is an EPROM-based CMOS device. Designs can be generated using Signetics AMAZE, SNAP and SLICE PLD design software packages or one of several other commercially available JEDEC standard PLD design software packages, such as ABEL™ and CUPL™.

Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply





ABEL™ is a trademark of Data I/O Corporation.
CUPL™ is a trademark of Logical Devices, Inc.

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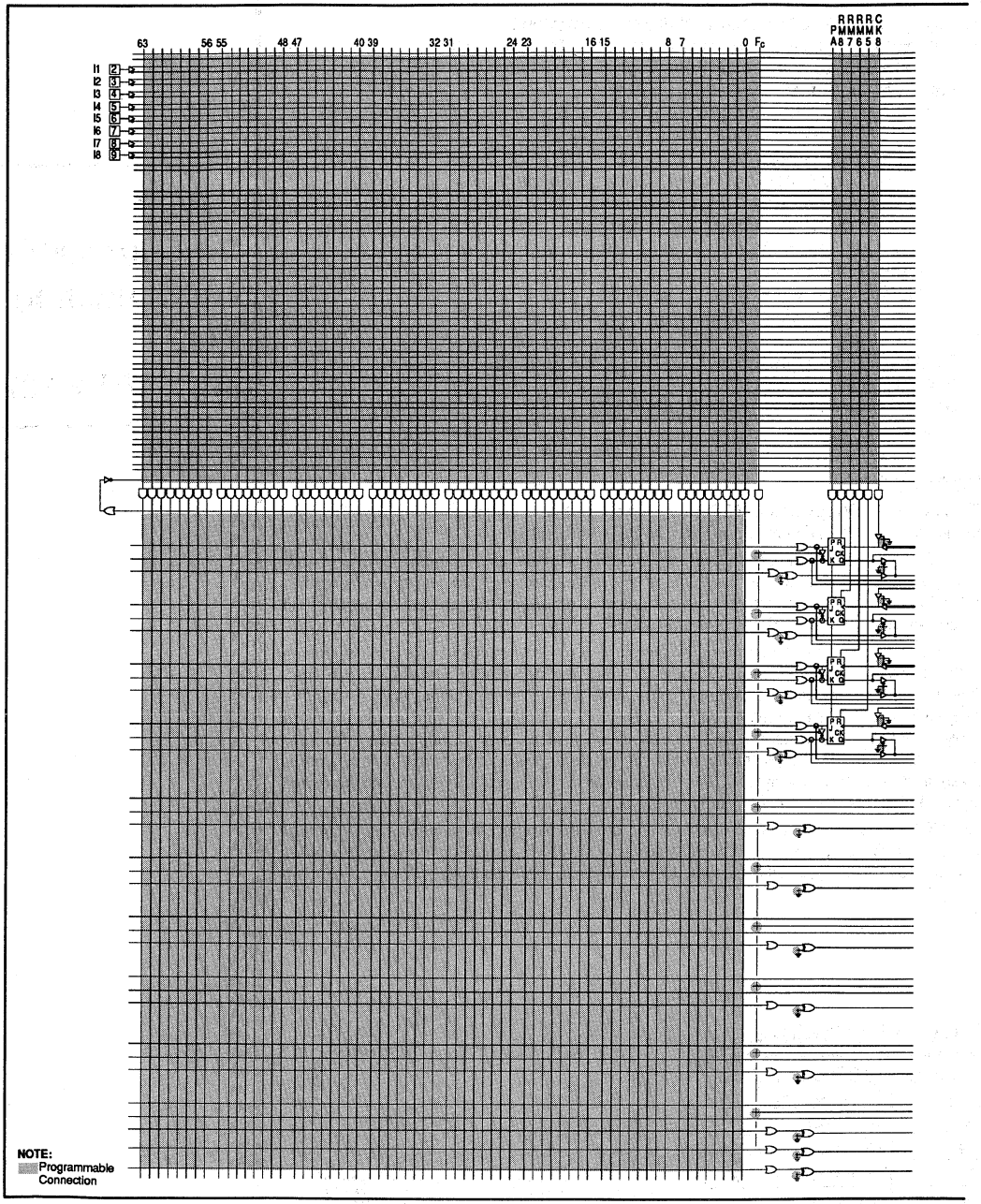
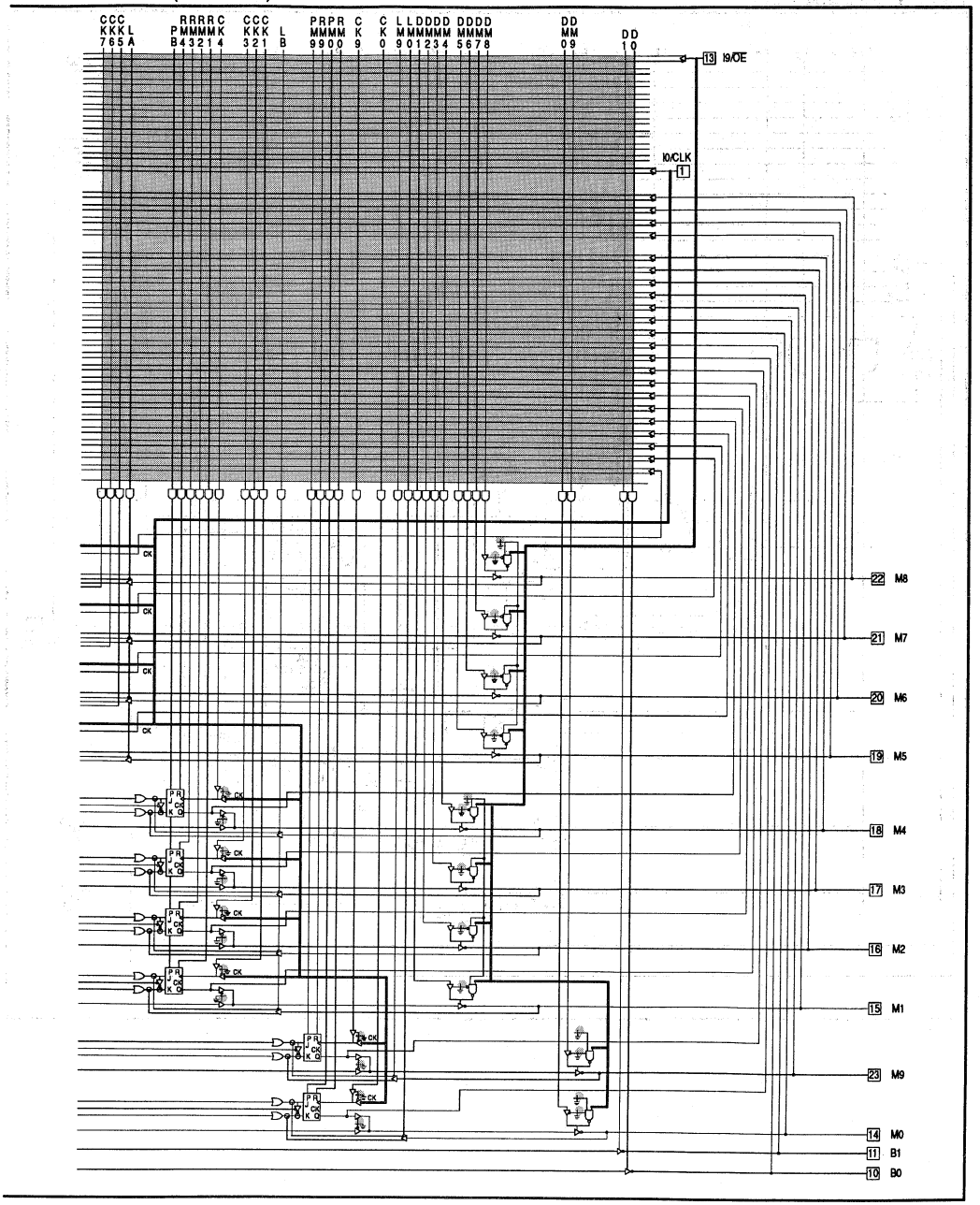
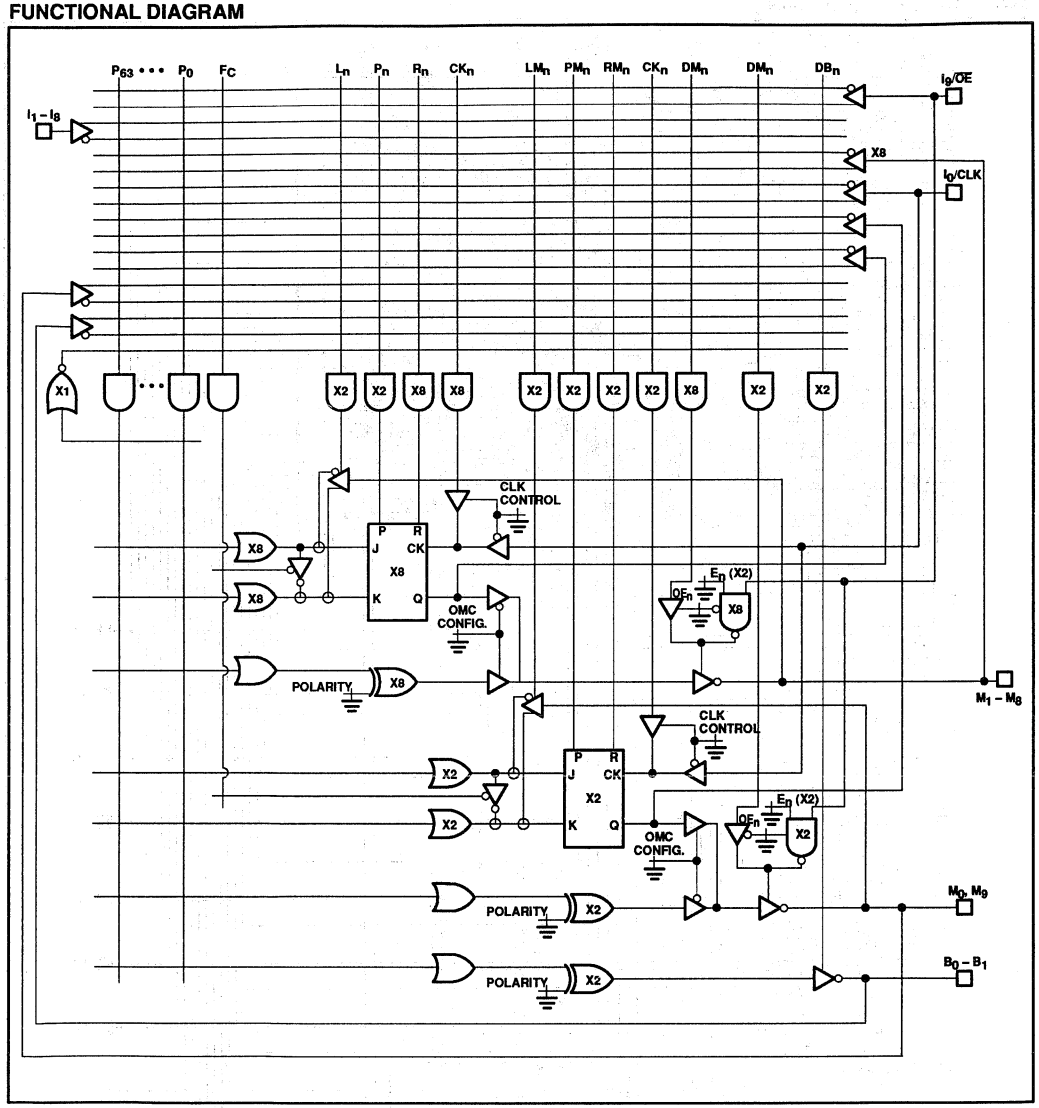
LOGIC DIAGRAM



LOGIC DIAGRAM (Continued)



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V_{DC}
V_{IN}	Input voltage	−0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	−0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	−10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	−65 to +150	°C

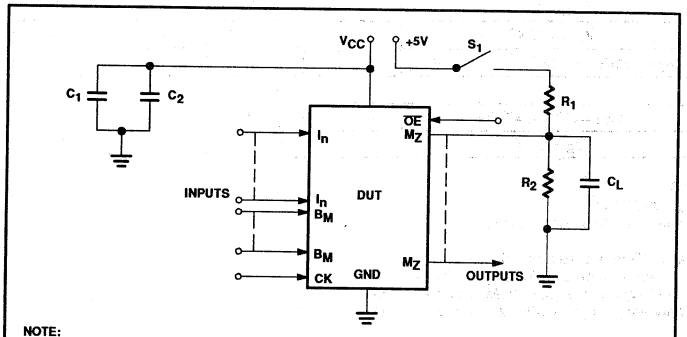
NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

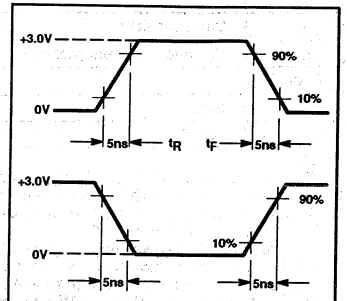
AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

8

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN; I_{OL} = 16mA		0.3	0.5	V
V_{OH}	High	V_{CC} = MIN; I_{OH} = –3.2mA	2.4	4.3		V
Input current						
I_{IL}	Low	V_{IN} = GND		–1	–10	µA
I_{IH}	High	V_{IN} = V_{CC}		+1	10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND		1 –1	10 –10	µA µA
I_{OS}	Short-circuit[3,6]	V_{OUT} = GND			–130	mA
I_{CC}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA, f = 15MHz[5], V_{CC} = MAX		90	120	mA
Capacitance						
C_I	Input	V_{CC} = 5V; V_{IN} = 2.0V		12		pF
C_B	I/O [6]	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short–circuit should not exceed one second. Test one at a time.
4. Tested with V_{IL} = 0.45V, V_{IH} = 2.4V.
5. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
   The I_{CC} increases by 1.5mA per MHz for the frequency range of 16MHz up to 25MHz.
   The I_{CC} remains at a worst case of 135mA for the frequency range of 26MHz up to 37MHz.
   The I_{CC} decreases by 1.0mA per MHz for the frequency range of 14MHz down to 1MHz (106mA @ 1MHz).
   The worst case I_{CC} is calculated as follows:
   - All dedicated inputs are switching.
   - All OMCs are configured as JK flip-flops in the toggle mode. . .all are toggling.
   - All 12 outputs are disabled.
   - The number of product terms connected does not impact the I_{CC}.
   - I_{CC} levels are identical for both TTL and CMOS input levels.
6. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

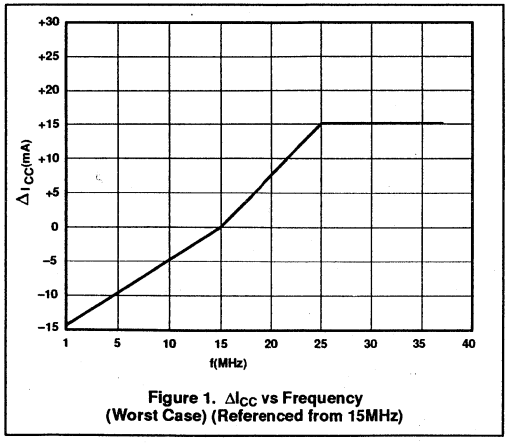


Figure 1. ΔI_{CC} vs Frequency (Worst Case) (Referenced from 15MHz)

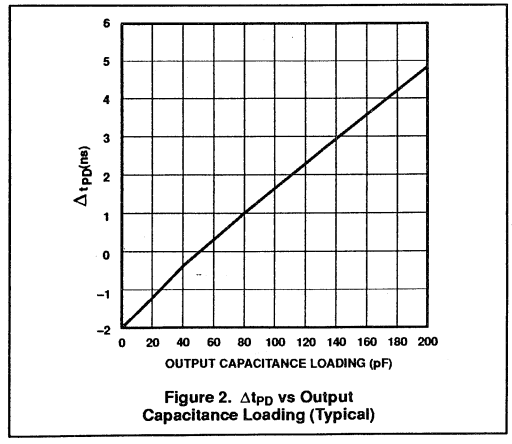


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12 MIN	PLC42VA12 TYP[1]	PLC42VA12 MAX	UNIT
Set-up Time								
t_{IS1}	Input; dedicated clock	(I, B, M) +/–	CK+	50	23	16		ns
t_{IS2}	Input; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	20	13		ns
t_{IS3}[3]	Preload; dedicated clock	(M) +/–	CK+	50	10	3.5		ns
t_{IS4}[3]	Preload; P-term clock	(M) +/–	(I, B, M) +/–	50	2	–1.0		ns
t_{IS5}[3]	Input through complement array; dedicated clock	(I, B, M) +/–	CK+	50	50	34		ns
t_{IS6}[3]	Input through complement array; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	40	30		ns
Propagation Delay								
t_{PD1}	Propagation Delay	(I, B, M) +/–	(I, B, M) +/–	50		20	35	ns
t_{PD2}	Propagation Delay with complement array (2 passes)	(I, B,) +/–	(I, B, M) +/–	50		36	55	ns
t_{CKO1}	Clock to Output; Dedicated clock	CK+	(M) +/–	50		13	17	ns
t_{CKO2}	Clock to output; P-term clock	(I, B, M) +/–	(M) +/–	50		18	27	ns
t_{RP1}	Registered operating period; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		29	40	ns
t_{RP2}	Registered operating period; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		31	47	ns
t_{RP3}[3]	Register preload operating period; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50		16.5	27	ns
t_{RP4}[3]	Register preload operating period; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50		17	29	ns
t_{RP5}[3]	Registered operating period with complement array; dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		47	67	ns
t_{RP6}[3]	Registered operating period with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		48	67	ns
t_{OE1}	Output Enable; from /OE pin[4]	/OE –	(M) +/–	50		10	20	ns
t_{OE2}	Output Enable; from P-term[4]	(I, B, M) +/–	(B, M) +/–	50		12.5	25	ns
t_{OD1}	Output Disable; from /OE pin[4]	/OE +	Outputs disabled	5		10	20	ns
t_{OD2}	Output Disable; from P-term[4]	(I, B, M) +/–	Outputs disabled	5		14.5	25	ns
t_{PRO}[3]	Preset to Output	(I, B, M) +/–	(M) +/–	50		25	35	ns
t_{PPR}[3]	Power-on Reset (Mn = 1)	V_{CC} +	(M) +/–	50			15	ns
Hold Time								
t_{IH1}	Input (Dedicated clock)	CK+	(I, B, M) +/–	50	0	–13		ns
t_{IH2}	Input (P-term clock)	(I, B, M) +/–	(I, B, M) +/–	50	5	–7.5		ns
t_{IH3}[3]	Input; from Mn (Dedicated clock)	CK+	(M) +/–	50	5	–1.5		ns
t_{IH4}[3]	Input; from Mn (P-term clock)	(I, B, M) +/–	(M) +/–	50	10	3.5		ns
Pulse Width								
t_{CKH1}	Clock High; Dedicated clock	CK+	CK–	50	10	5		ns
t_{CKL1}	Clock Low; Dedicated clock	CK–	CK+	50	10	5		ns
t_{CKH2}	Clock High; P-term clock	CK+	CK–	50	15	7		ns
t_{CKL2}	Clock Low; P-term clock	CK–	CK+	50	15	7		ns
t_{PRH}[3]	Width of preset/reset input pulse	(I, B, M) +/–	(I, B, M) +/–	50	30	7		ns

Notes on page 8-108

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AC ELECTRICAL CHARACTERISTICS (Continued)

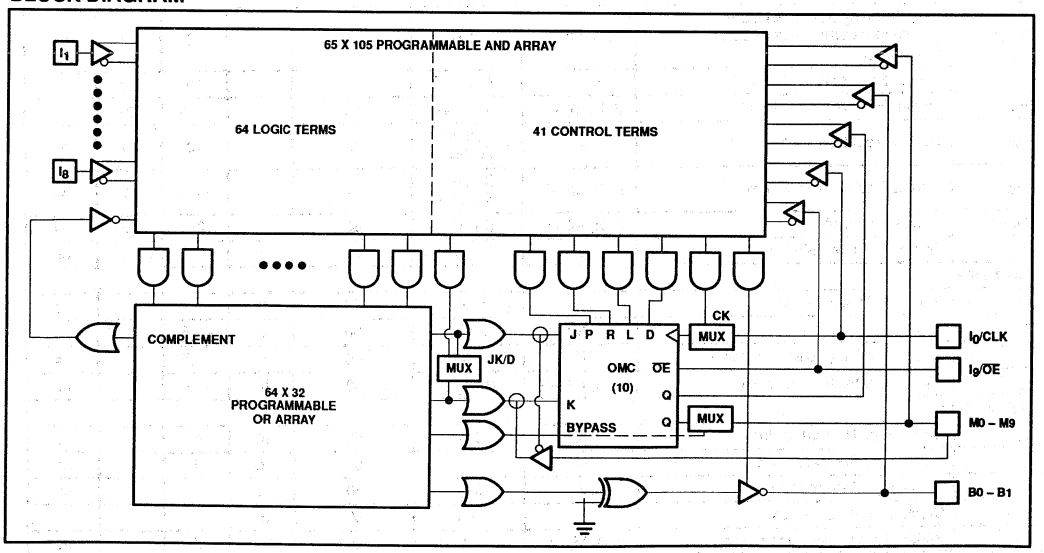
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12 MIN	PLC42VA12 TYP[1]	PLC42VA12 MAX	UNIT
Frequency of Operation								
f_{CK1}	Dedicated clock frequency	C+	C+	50	50	100		MHz
f_{CK2}	P-term clock frequency	C+	C+	50	33	71.4		MHz
f_{MAX1}	Registered operating frequency; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	25	34.5		MHz
f_{MAX2}	Registered operating frequency; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	21.3	32.3		MHz
f_{MAX3}[3]	Register preload operating frequency; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50	37	60.6		MHz
f_{MAX4}[3]	Register preload operating frequency; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50	34.5	58.8		MHz
f_{MAX5}[3]	Registered operating frequency with complement array; Dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	14.9	21.3		MHz
f_{MAX6}[3]	Registered operating frequency with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	14.9	20.8		MHz

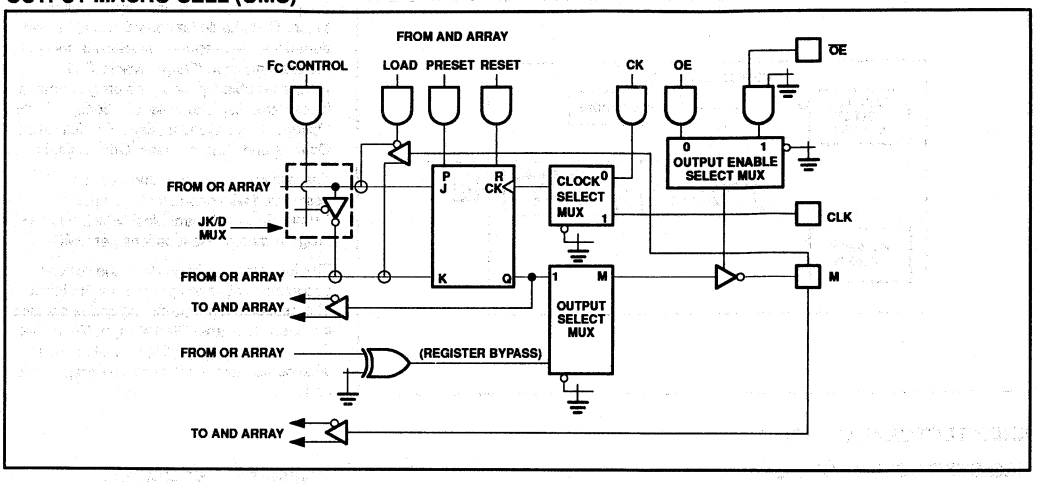
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$. These limits are not tested/guaranteed.
2. Refer also to AC Test Conditions (Test Load Circuit).
3. These limits are not tested, but are characterized periodically and are guaranteed by design.
4. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

BLOCK DIAGRAM



OUTPUT MACRO CELL (OMC)



Output Macro Cell Configuration

Atmel's unique Output Macro Cell design represents a significant advancement in the configurability of multi-function Programmable Logic Devices.

The PLC42VA12 has 10 programmable Output Macro Cells. Each can be individually programmed in any of 5 basic configurations:

- Dedicated I/O (combinatorial) with feedback to AND array
- Dedicated Input
- Combinatorial I/O with feedback and Buried Register with feedback (register bypass)
- Registered Input
- Registered Output with feedback

Each of the registered options can be further customized as J-K type or D-type, with either an internally derived clock (from the AND array) or clocked from an external source. With these additional programmable options, it is possible to program each Output Macro Cell in any one of 14 different configurations.

These 14 configurations, combined with the fully programmable OR array, make the PLC42VA12 the most versatile and silicon efficient of all the Output Macro Cell-type PLDs.

The most significant Output Macro Cell (OMC) feature is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other Output Macro Cell-type devices, the register in the OMC is fully functional as a buried register. Furthermore, both the combinatorial I/O and the buried register have separate input paths (from the AND array) and separate feedback paths (to the AND array). This feature provides the capability to operate the buried register independently from the combinatorial I/O.

The PLC42VA12 is ideally suited for both synchronous and asynchronous logic functions. Eleven clock sources – 10 driven from the AND array and one from an external source – make it possible to design synchronous state machine functions, event-driven state machine functions and combinatorial (asynchronous) functions all on the same chip.

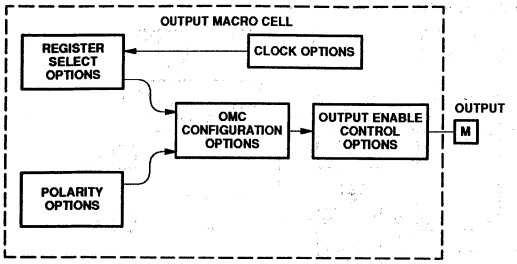
Sophisticated control functions support individual OE control and Reset functions from the AND array. OE control is also available from the $I_9/\overline{OE}$ pin. Register Preset and Load functions are controlled from the AND array, in 2 banks of 4 for OMCs M_1 – M_8. Output Macro Cells M_0 and M_9 have individual Preset and Load Control terms.

Output Polarity for the combinatorial I/O paths is configurable via 12 programmable EX-OR gates. The output of each register can be configured as inverting (active Low) or non-inverting (active High) via manipulation of the logic equations.

The output of each buried register can also be configured as inverting or non-inverting via the input buffer which feeds back to the AND array.

8

OUTPUT MACRO CELL PROGRAMMABLE OPTIONS



OMC Programmable Options

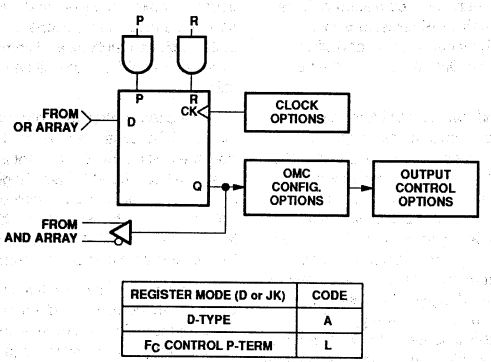
For purposes of programming, the Output Macro Cell should be considered to be partitioned into five separate blocks. As shown in the drawing titled "Output Macro Cell Programmable Options", the programmable blocks are: Register Select Options, Polarity Options, Clock Options, OMC Configuration Options and Output Enable Control Options.

There is one programmable location associated with each block except the Output Enable Control block which has two programmable fuse locations per OMC.

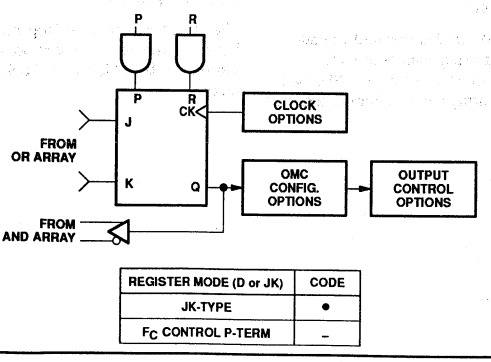
The following drawings detail the options associated with each programmable block. The associated programming codes are also included. The table titled "Output Macro Cell Configurations" (page 15) lists all the possible combinations of the five programmable options.

ARCHITECTURAL OPTIONS

REGISTER SELECT OPTIONS



REGISTER MODE (D or JK)	CODE
D-TYPE	A
F_C CONTROL P-TERM	L



REGISTER MODE (D or JK)	CODE
JK-TYPE	•
F_C CONTROL P-TERM	–

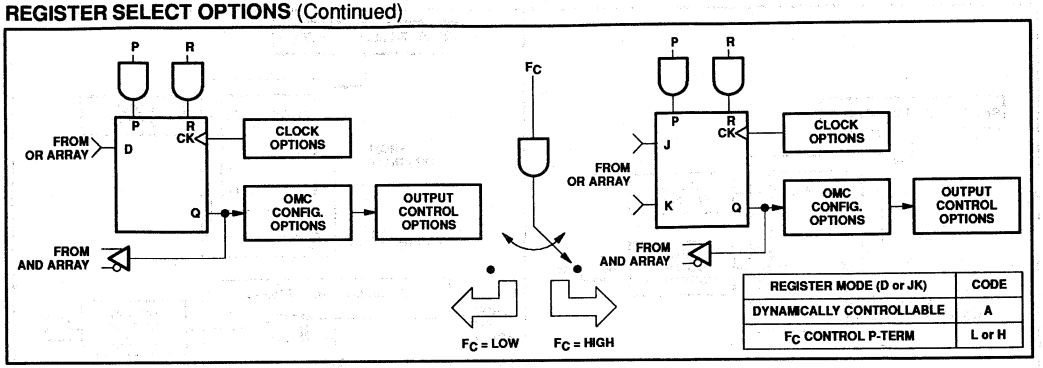
Register Select Options

Each OMC Register can be configured either as a dedicated D-type or a J-K flip-flop. The Flip-Flop Control term, Fc, provides the option to control each Register dynamically—switching from D-type to J-K type, based on the Fc control signal.

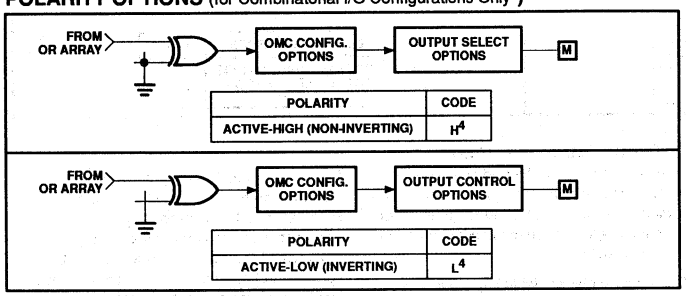
Register Preset and Reset are controlled from the AND array. Each OMC has an individual Reset Control term (RMn). The Register Preset function is controlled in two banks of 4 for OMCs $M_1 - M_3$ and $M_4 - M_8$ (via the control terms PA and PB). OMCs M_0 and M_9 have individual control terms (PM_0 and PM_9 respectively).

Notes on page 8-115

REGISTER SELECT OPTIONS (Continued)



POLARITY OPTIONS (for Combinatorial I/O Configurations Only[1])

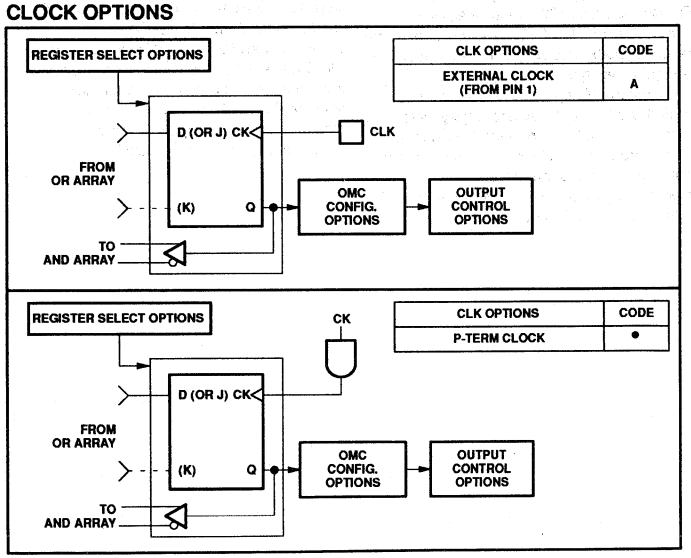


Polarity Options

When an OMC is configured as a Combinatorial I/O with Buried Register, the polarity of the combinatorial path can be programmed as Active-High or Active-Low. A configurable EX-OR gate provides polarity control.

If an OMC is configured as a Registered Output, /Q is propagated to the output pin. Note that either Q or /Q can be fedback to the AND array by manipulating the feedback logic equations. (TRUE or COMPLEMENT).

CLOCK OPTIONS



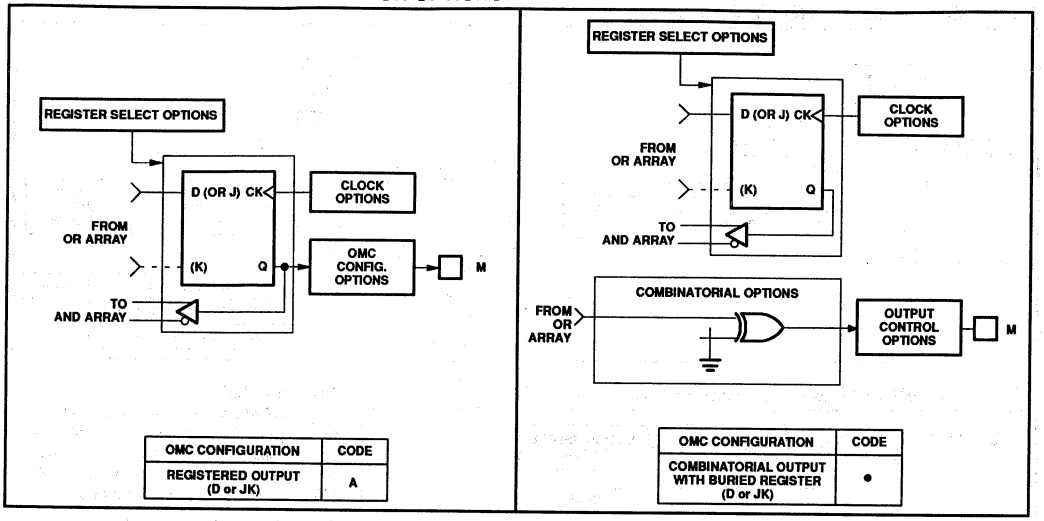
Clock Options

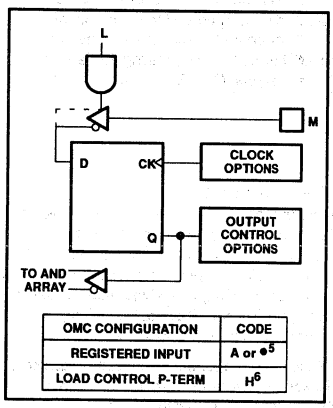
In the unprogrammed state, all Output Macro Cell clock sources are connected to the External Clock pin (I_0/CLK pin 1). Each OMC can be individually programmed such that its P-term Clock (CK_n) is enabled, thus disabling it from the External Clock and providing event-driven clocking capability.

This feature supports multiple state machines, clocked at several different rates, all on one chip, or the ability to collect large amounts of random logic, including 10 separately clocked flip-flops.

Notes on page 8-115

OUTPUT MACRO CELL CONFIGURATION OPTIONS





OMC Configuration Options

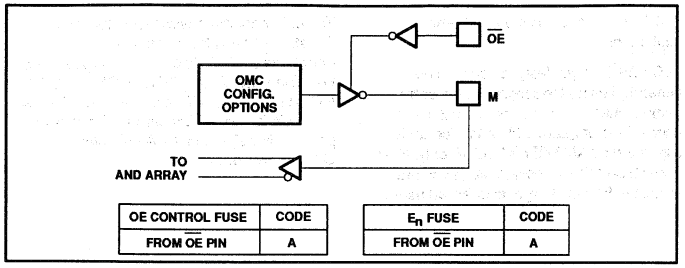
Each OMC can be configured as a Registered Output with feedback, a Registered Input or a Combinatorial I/O with Buried Register. Dedicated Input and dedicated I/O configurations are also possible.

When the Combinatorial I/O option is selected, (the Register Bypass option), the Buried Register remains 100% functional, with its own inputs from the AND array and a separate feedback path. This unique feature is ideal for designing any type of state machine; synchronous Mealy-types that require both Buried and Output Registers, or asynchronous Mealy-types that require buried registers and combinatorial output functions. Both synchronous and asynchronous Moore-type state machines can also be easily accommodated with the flexible OMC structure.

Note that an OMC can be configured as either a Combinatorial I/O (with Buried Register) or a Registered Output with feedback and it can still be used as a Registered Input. By disabling the outputs via any OE control function, the M pin can be used as an input. When the Load Control P-term is asserted HIGH, the register is preloaded from the M pin(s). When the L_C P-term is Active-Low and the output is enabled, the OMC will again function as configured (either a combinatorial I/O or a registered output with feedback). This feature is suited for synchronizing input signals prior to commencing a state sequence.

Notes on page 8-115

OUTPUT CONTROL OPTIONS



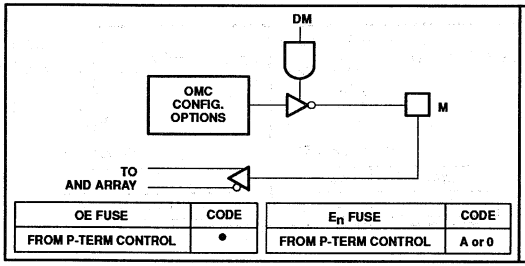
OE CONTROL FUSE	CODE
FROM $\overline{OE}$ PIN	A

E_n FUSE	CODE
FROM $\overline{OE}$ PIN	A

Output Enable Control Options

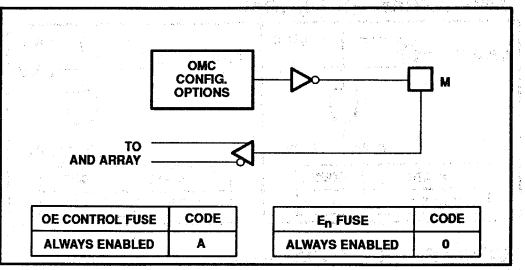
Similar to the Clock Options, the Output Enable Control for each OMC can be connected either to an external source (I_9/$\overline{OE}$, pin 13) or controlled from the AND array (P-terms DM_n). Each Output can also be permanently enabled.

Output Enable control for the two bi-directional I/O (B pins 10 and 11) is from the AND array only (P-terms DB0 and DB1 respectively).



OE FUSE	CODE
FROM P-TERM CONTROL	•

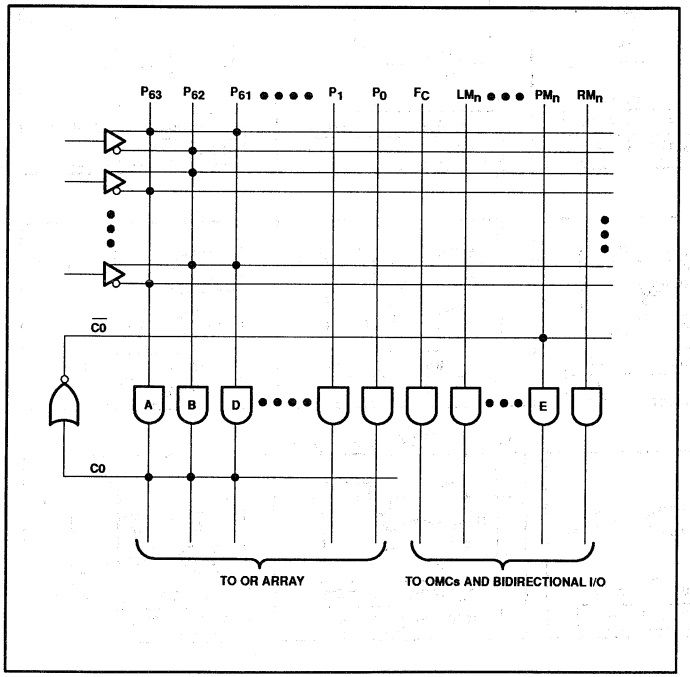
E_n FUSE	CODE
FROM P-TERM CONTROL	A or 0



OE CONTROL FUSE	CODE
ALWAYS ENABLED	A

E_n FUSE	CODE
ALWAYS ENABLED	0

COMPLEMENT ARRAY DETAIL



Complement Array Detail

The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and $(\overline{A + B + C})$ are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

Notes on page 8-115

LOGIC PROGRAMMING

The PLC42VA12 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics AMAZE, SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLC42VA12 architecture.

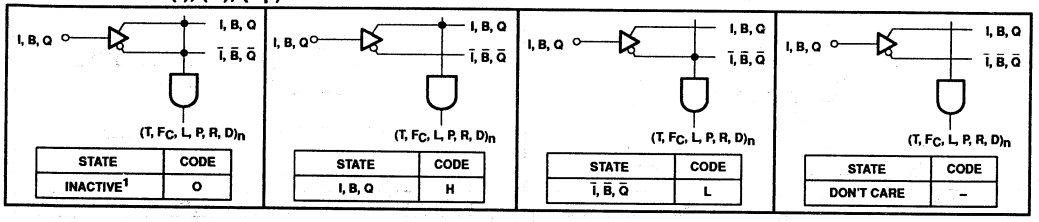
All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC42VA12 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by AMAZE and SLICE only. Both AMAZE and SLICE design packages are available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below. Symbols for OMC configuration have been previously defined in the Architectural Options section.

LOGIC IMPLEMENTATION

"AND" ARRAY – (I), (B), (Qp)



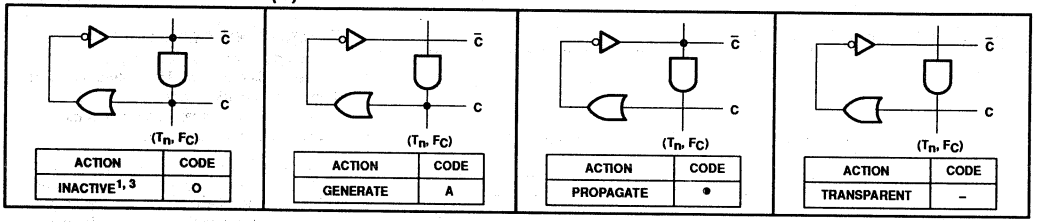
STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B, Q	H

STATE	CODE
$\overline{I}, \overline{B}, \overline{Q}$	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



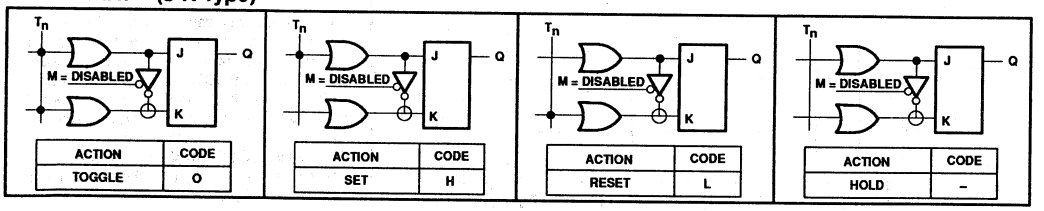
ACTION	CODE
INACTIVE[1, 3]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (J-K Type)



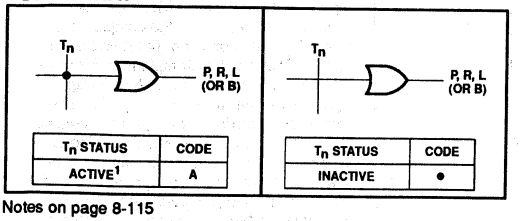
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

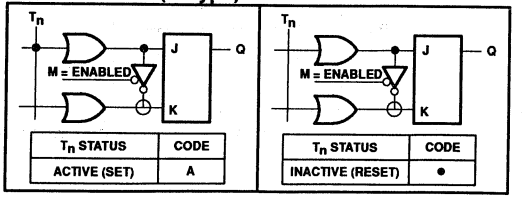
"OR" ARRAY



T_n STATUS	CODE
ACTIVE[1]	A

T_n STATUS	CODE
INACTIVE	•

"OR" ARRAY – (D-Type)



T_n STATUS	CODE
ACTIVE (SET)	A

T_n STATUS	CODE
INACTIVE (RESET)	•

Notes on page 8-115

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

LOGIC IMPLEMENTATION (Continued)

OUTPUT MACRO CELL CONFIGURATIONS

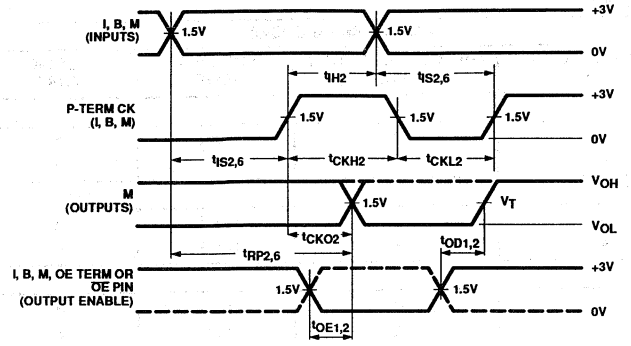
OUTPUT MACRO CELL CONFIGURATION	PROGRAMMING CODES			
	REGISTER SELECT FUSE	OMC CONFIGURATION FUSE	POLARITY FUSE	CLOCK FUSE
Combinatorial I/O with Buried D-type register				
External clock source	A	•	H or L	A
P-term clock source	A	•	H or L	•
Combinatorial I/O with Buried J-K type register				
External clock source	•	•	H or L	A
P-term clock source	•	•	H or L	•
Registered Output (D-type) with feedback				
External clock source	A	A	N/A	A
P-term clock source	A	A	N/A	•
Registered Output (J-K type) with feedback				
External clock source	•	A	N/A	A
P-term clock source	•	A	N/A	•
Registered Input (Clocked Preload) with feedback				
External clock source	A	A or •[5]	Optional[5]	A
P-term clock source	A	A or •[5]	Optional[5]	•

OUTPUT ENABLE CONTROL[8] CONFIGURATION	OUTPUT CONTROL FUSES		CONTROL SIGNAL
	OE CONTROL FUSE	En FUSES	
OMC controlled by /OE pin	A	A	
Output Enabled			Low
Output Disabled			High
OMC controlled by P-term	•	A or 0	
Output Enabled			High
Output Disabled			Low
Output always Enabled	A	0	Not Applicable

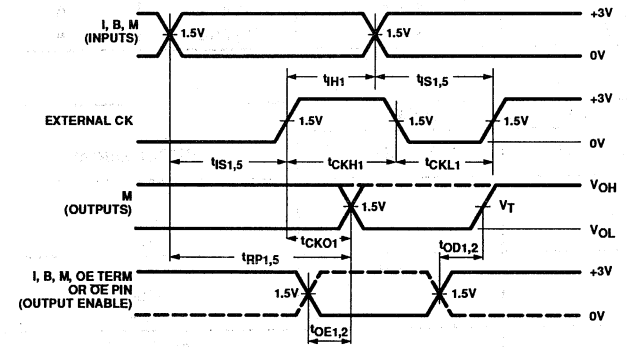
NOTES:

1. This is the initial (unprogrammed) state of the device.
2. Any gate will be unconditionally inhibited if both the TRUE and COMPLEMENT fuses are left intact.
3. To prevent oscillations, this state is not allowed for Complement Array fuse pairs that are coupled to active product terms.
4. The OMC Configuration fuse must be programmed as Combinatorial I/O in order to make use of the Polarity Option.
5. Regardless of the programmed state of the OMC Configuration fuse, an OMC can be used as a Registered Input. Note that the Load Control P-term must be asserted Active-High.
6. Output must be disabled.
7. Program code definitions:
   - A = Active (unprogrammed fuse)
   - 0, • = Inactive (programmed fuse)
   - – = Don't Care (both TRUE and COMPLEMENT fuses unprogrammed)
   - H = Active-High connection
   - L = Active-Low connection
8. OE control for B_0 and B_1 (Pins 10 and 11) is from the AND array only.

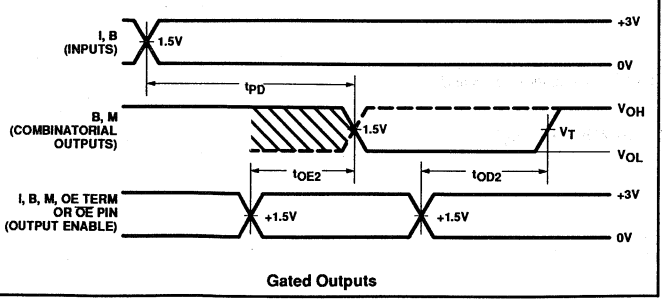
TIMING DIAGRAMS



Flip-Flop Outputs with P-term Clock



Flip-Flop Outputs with External Clock

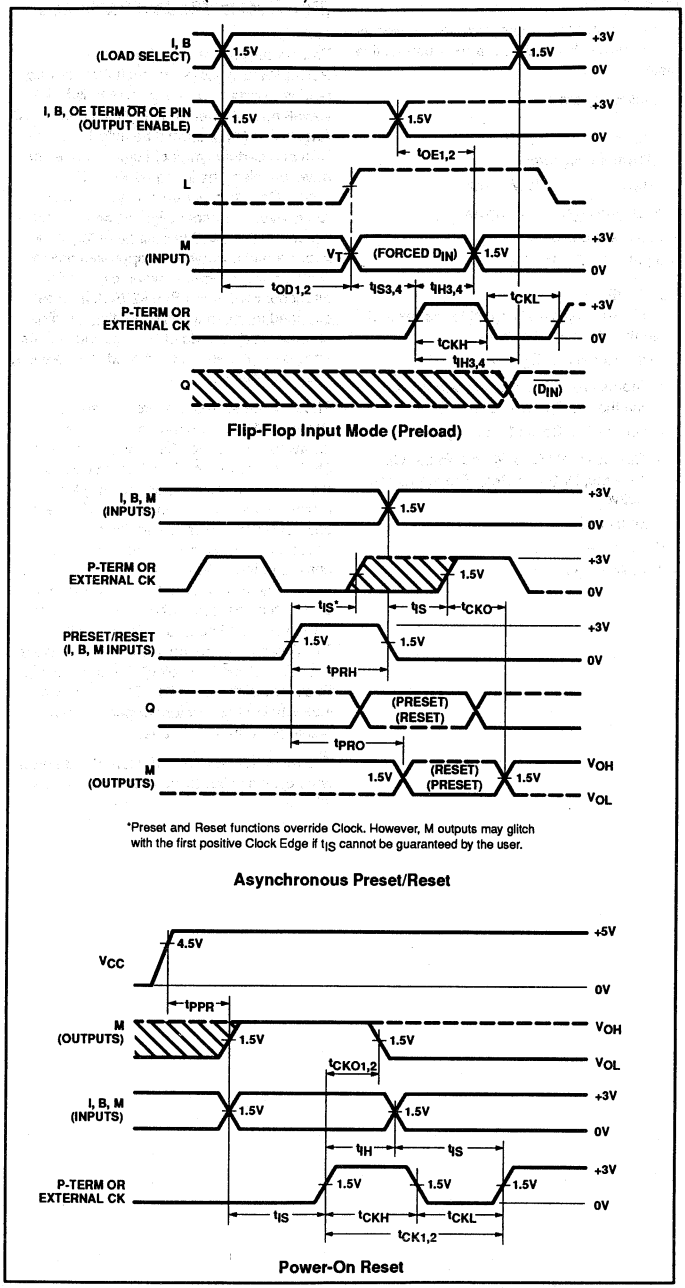


Gated Outputs

TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CK1}	Clock Frequency; External Clock
f_{CK2}	Clock Frequency; P-term Clock
t_{CKH1}	Width of Input Clock Pulse; External Clock
t_{CKH2}	Width of Input Clock Pulse; P-term Clock
t_{CKL1}	Interval between Clock pulses; External Clock
t_{CKL2}	Interval between Clock Pulses; P-term Clock
t_{CKO1}	Delay between the Positive Transition of External Clock and when M Outputs become valid.
t_{CKO2}	Delay between the Positive Transition of P-term Clock and when M Outputs become valid.
t_{RP1}	Delay between beginning of Valid Input and when the M outputs become Valid when using External Clock.
t_{RP2}	Delay between beginning of Valid Input and when the M outputs become Valid when using P-term Clock.
t_{RP3}	Delay between beginning of Valid Input and when the M outputs become Valid when using Preload Inputs (from M pins) and External Clock.
t_{RP4}	Delay between beginning of Valid Input and when the M outputs become valid when using Preload inputs (from M pins) and P-term Clock.
t_{RP5}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and External clock.
t_{RP6}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and P-term Clock.
f_{MAX1}	Minimum guaranteed Operating Frequency; Dedicated Clock
f_{MAX2}	Minimum guaranteed Operating Frequency; P-term Clock
f_{MAX3}	Minimum guaranteed Operating Frequency using Preload; Dedicated Clock (M pin to M pin)
f_{MAX4}	Minimum guaranteed Operating Frequency using Preload; P-term Clock (M pin to M pin)
f_{MAX5}	Minimum guaranteed Operating Frequency using Complement Array; Dedicated Clock
f_{MAX6}	Minimum Operating Frequency using Complement Array; P-term Clock
t_{IH1}	Required delay between positive transition of External Clock and end of valid input data.

TIMING DIAGRAMS (Continued)

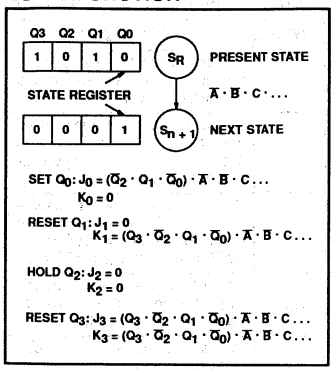


TIMING DEFINITIONS (Continued)

SYMBOL	PARAMETER
t_{IH2}	Required delay between positive transition of P-term Clock and end of valid input data.
t_{IH3}	Required delay between positive transition of External Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IH4}	Required delay between positive transition of P-term Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IS1}	Required delay between beginning of valid input and positive transition of External Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of P-term Clock input.
t_{IS3}	Required delay between beginning of valid Preload input (from M pins) and positive transition of External Clock.
t_{IS4}	Required delay between beginning of valid Preload input (from M pins) and positive transition of P-term Clock input.
t_{IS5}	Required delay between beginning of valid input through Complement Array and positive transition of External Clock.
t_{IS6}	Required delay between beginning of valid input through Complement Array and positive transition of P-term Clock input.
t_{OE1}	Delay between beginning of Output Enable signal (Low) from /OE pin and when Outputs become valid.
t_{OE2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable signal (HIGH) from /OE pin and when Outputs become disabled.
t_{OD2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become disabled.
t_{PD}	Delay between beginning of valid input and when the Outputs become valid (Combinatorial Path).
t_{PRH}	Width of Preset/Reset Pulse.
t_{PRO}	Delay between beginning of valid Preset/Reset Input and when the registered Outputs become Preset ("1") or Reset ("0").
t_{PPR}	Delay between V_{CC} (after power-up) and when flip-flops become Reset to "0". Note: Signal at Output (M pin) will be inverted.

8

LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L_n	CK_n	P_n	R_n	J	K	Q	M
H								Hi-Z
L	X	X	X	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive Logic:
   $J\text{-}K = T_0 + \overline{T}_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \cdot (I_0 \cdot \overline{I}_1 \cdot I_2 \ldots) \cdot (Q_0 \cdot \overline{Q}_1 \ldots) \cdot (B_0 \cdot B_1 \ldots)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at M_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop (Diagnostic mode).

PLC42VA12 UNPROGRAMMED STATE

A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

The following are:

ACTIVE:
- OR array logic terms
- Output Macro Cells M1 – M8;
  - D-type registered outputs
- External clock path
- Inputs: B_0, B_1, M_0, M_9

INACTIVE:
- AND array logic and control terms (except flip-flop mode control term, F_C)
- Bidirectional I/O (B_0, B_1);
  - Inputs are active. Outputs are 3-Stated via the OE P-terms, D_0 and D_1.
- Output Macro Cells M_0 and M_9;
  - Bidirectional I/O, 3-Stated via the OE P-terms, DM_0 and DM_9. The inputs are active.
- P-term clocks
- Complement Array
- J-K Flip-Flop mode

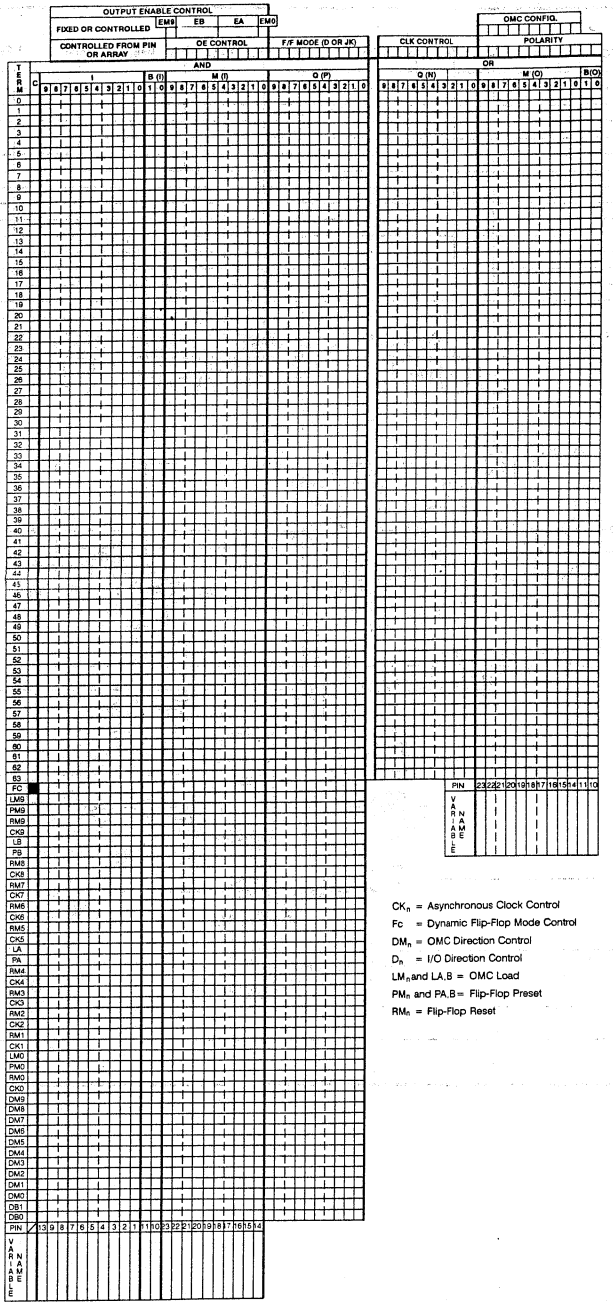
ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC42VA12 devices are such that erasure begins to occur upon exposure to light with wavelength shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC42VA12 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC42VA12 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC42VA12 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retentions exceeds 20 years.

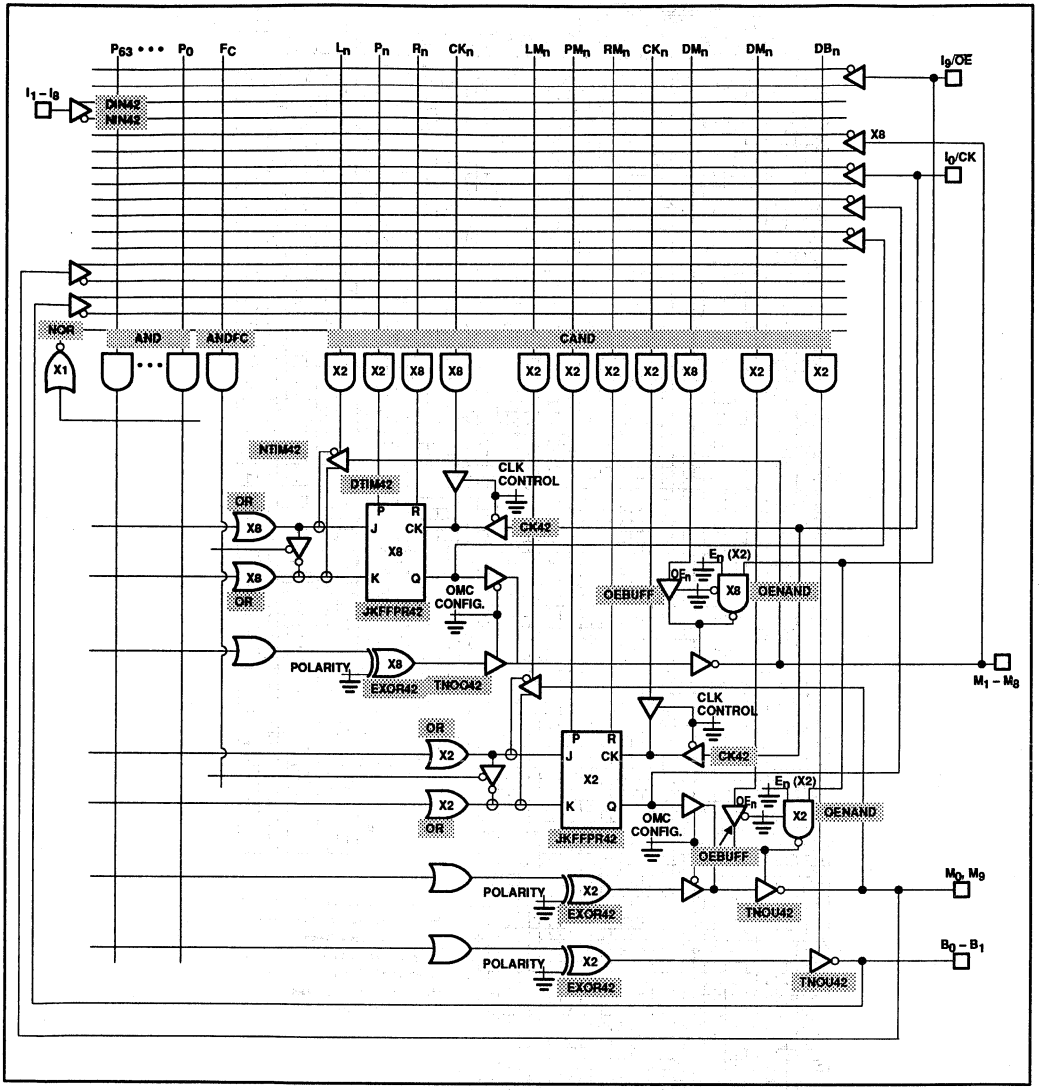
PROGRAM TABLE



CK_n = Asynchronous Clock Control
Fc = Dynamic Flip-Flop Mode Control
DM_n = OMC Direction Control
D_n = I/O Direction Control
LM_n and LA,B = OMC Load
PM_n and PA,B = Flip-Flop Preset
RM_n = Flip-Flop Reset

8

SNAP RESOURCE SUMMARY DESIGNATIONS



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
35	16	27	ATS42VA12-35DC ATS42VA12-35JC ATS42VA12-35PC	24DW3 28J 24P3	Commercial (0°C to 70°C)

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
24P3	24 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)

Features

- Pin-for-Pin Compatible, Functional Superset of PLS105/A and PLUS405 Logic Sequencers
- Zero Standby Power of Less than 100 µA (Worst Case)
  Power Dissipation at f_{MAX} = 80 mA (Worst Case)
- CMOS and TTL Compatible
- Programmable Asynchronous Initialization and OE Functions
  Controllable from AND Array or External Source
- 17 Input Variables
- 8 Output Functions
- 68 Product Terms
  64 Transition Terms
  4 Control Terms
- 8-bit State Register
- 8-bit Output Register
- 2 Transition Complement Arrays
- Multiple Clocks
- Diagnostic Test Modes Features for Access to State and Output Registers
- Power-on Preset of all Registers to "1"
- J-K Flip-flops
  Automatic Hold States
- Security Fuse
- 3-State Outputs
- Second Source to Signetic's PLC415-16

CMOS Programmable Logic Sequencer (17 x 68 x 8)

8

Description

The ATS415 PLD is a CMOS Programmable Logic Sequencer of the Mealy type. The ATS415 is a pin-for-pin compatible, functional superset of the PLS105 and PLUS405 Bipolar Programmable Logic Sequencer devices.

The ATS415 is ideally suited for high density, power sensitive controller functions. The Power Down feature provides true CMOS standby power levels of less than 100 µA. The EPROM-based process technology supports operating frequencies of 16 to 20 MHz. The ATS415 has been designed to accept both CMOS and TTL input levels to facilitate logic integration in almost any system environment.

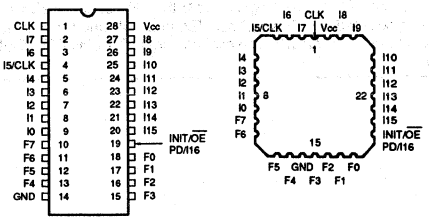
The ATS415 architecture has been tailored for state machine functions. Both arrays are programmable, thus providing full interconnectability. Any one or all of the 64 AND transition terms can be connected to any (or all) of the 8 buried state and 8 output registers.

Two clock sources enable the design of two state machines on one chip. Separate INIT functions and Output Enable functions for each are controllable either from the array or from an external pin. The J-K flip-flops provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. The programmable initialization feature supports asynchronous initialization of the state machine to any user defined pattern.

The unique Complement Array feature supports complex ELSE transition statements with a single product term. The ATS415 has 2 Complement Arrays which allows the user to design two independent complement functions. This is particularly useful if two state machines have been implemented on one chip.

Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks P_{0-3} and F_{0-3} if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5–9, 26–27 20–22	$I_0 - I_4$, I_7, I_6 $I_8 - I_9$ $I_{13} - I_{15}$	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	I_5/CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P_{4-7} and Output Registers F_{4-7}, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I_{12}	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{12} is held at +11V, device outputs $F_0 - F_7$ reflect the contents of State Register bits $P_0 - P_7$. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I_{11}	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{11} is held at +11V, device outputs $F_0 - F_7$ become direct inputs for State Register bits $P_0 - P_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0 - F_7$ into the State Register bits $P_0 - P_7$. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I_{10}	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{10} is held at +11V, device outputs $F_0 - F_7$ become direct inputs for Output Register bits $Q_0 - Q_7$; a Low-to-High transition on the appropriate clock line loads the values on pins $F_0 - F_7$ into the Output Register bits $Q_0 - Q_7$. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10–13 15–18	$F_0 - F_7$	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits $Q_0 - Q_7$, when enabled. When I_{12} is held at +11V, $F_0 - F_7 = (P_0 - P_7)$. When I_{11} is held at +11V, $F_0 - F_7$ become inputs to State Register bits $P_0 - P_7$. When I_{10} is held at +11V, $F_0 - F_7$ become inputs to Output Register bits $Q_0 - Q_7$.	Active-High (H)
19	INIT/$\overline{OE}$ I_{16}/PD	**External Initialization, External /OE, PD or I_{16}:** A user programmable function: Only one of the four options below may be selected. Note that both Initialization and /OE options are alternately available via the AND array. (P-terms INA, INB, OEA, and OEB.)	
		• **External Initialization:** Provides an asynchronous Preset to logic "1" or Reset to logic "0" of any or all State and Output Registers, determined individually on a register-by-register basis. INIT overrides the clock, and when held High, clocking is inhibited. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the INIT pulse goes Low. See timing diagrams for t_{NVCK} and t_{VCK}. Note that if the External Initialization option is selected, I_{16} is disabled automatically via the design software and the Power Down and External OE options are not available. Internal OE is available via P-Terms OEA and/or OEB. This option can be selected for one or both banks of registers.	Active-High (H)
		• **External Output Enable:** Provides an Output Enable/Disable function for Output Registers. Note that if the External OE option is selected, I_{16} is disabled automatically via the design software and the Power Down and External INIT options are not available. Internal INIT is available via P-terms INA and/or INB. This option can be selected for one or both banks of registers.	Active-Low (L)
		• **Power Down:** When invoked, provides a Power Down (zero power) mode. The contents of all Registers is retained, despite the toggling of the Inputs or the clocks. To obtain the lowest possible power level, all Inputs should be static and at CMOS input levels. Note that if the PD options is selected, I_{16} is disabled automatically via the design software and the External INIT and External OE options are not available. Internal INIT is available via P-terms INA and/or INB and Internal OE is available via P-terms OEA and/or OEB.	Active-High (H)
		• **Logic Input:** The 17th external logic input to the AND array as above. Note that when the I_{16} option is selected, the Power Down, External /OE and External INIT are not available. Internal OE and Internal INIT are available from P-Terms OEA/OEB and INA/INB, respectively.	Active-High/Low (H/L)

TRUTH TABLE [1, 2, 3, 4, 5]

V_{CC}	OPTION INIT	OPTION $\overline{OE}$	I_{10}	I_{11}	I_{12}	CK	J	K	Q_P	Q_F	F
	H		X	X	X	X	X	X	H/L	H/L	Q_F
	X		+11V	X	X	↑	X	X	Q_P	L	L
	X		+11V	X	X	↑	X	X	Q_P	H	H
	X		X	+11V	X	↑	X	X	L	Q_F	L
	X		X	+11V	X	↑	X	X	H	Q_F	H
	X		X	X	+11V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
+5V		H	X	X	X	X	X	X	Q_P	Q_F	Hi-Z
		X	+11V	X	X	↑	X	X	Q_P	L	L
		X	+11V	X	X	↑	X	X	Q_P	H	H
		X	X	+11V	X	↑	X	X	L	Q_F	L
		X	X	+11V	X	↑	X	X	H	Q_F	H
		L	X	X	+11V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	L	L	X	X	X	X	X	X	H	H	H

NOTES:

1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)(I_0, I_1, I_2, \ldots)(P_0, P_1 \ldots P_7)$
2. ↑ denotes transition from Low-to-High level.
3. X = Don't Care (≤5.5V)
4. H/L implies that either a High or a Low can occur, depending upon user-programmed Initialization selection (each State and Output Register individually programmable).
5. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

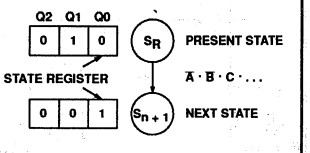
VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$/PD/I_{16} is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All J/K flip-flop inputs are disabled (0).
4. The Complement Arrays are inactive.
5. Clock 1 is connected to all State and Output Registers.

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q_2} \cdot Q_1 \cdot \overline{Q_0}) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q_2} \cdot Q_1 \cdot \overline{Q_0}) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

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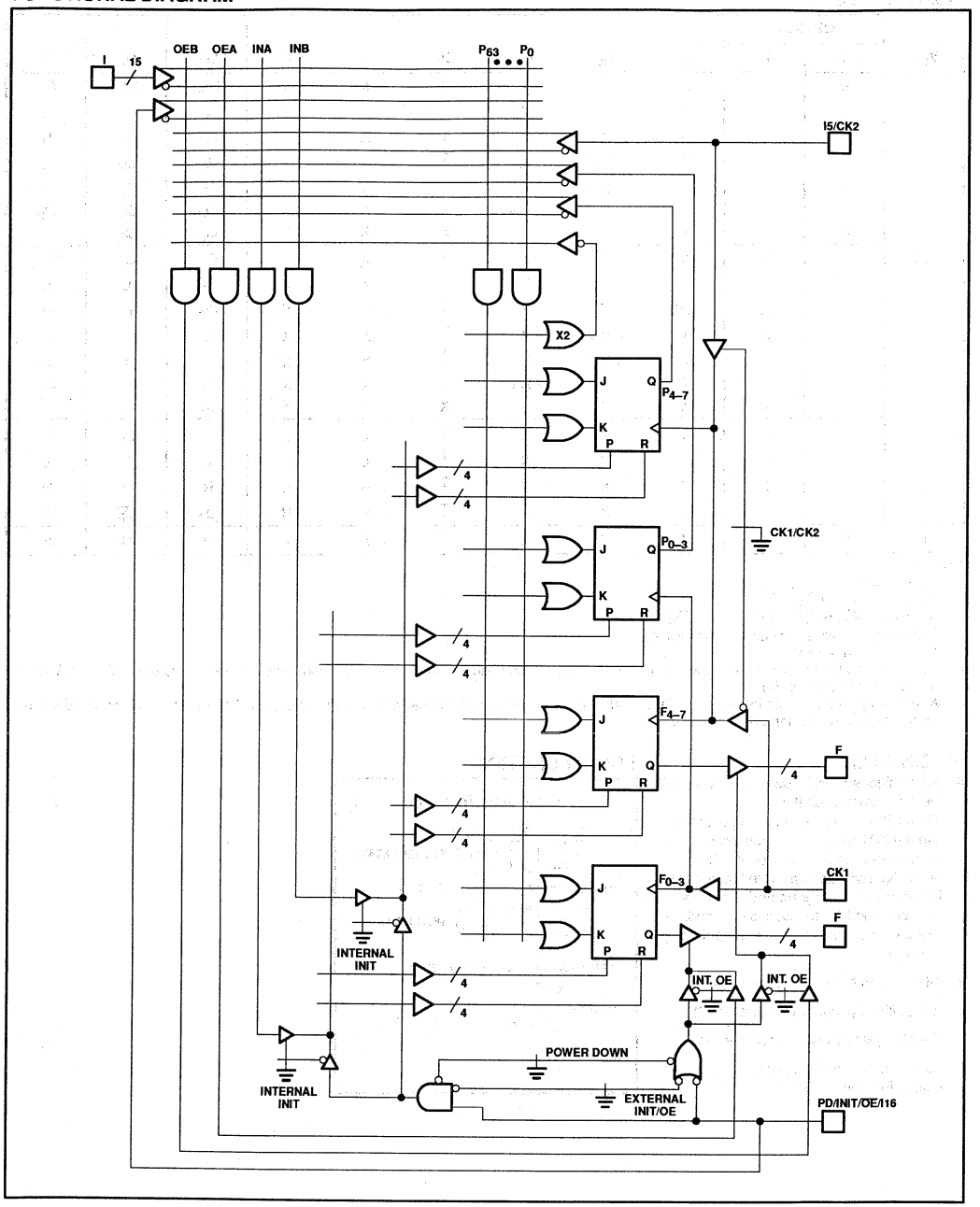
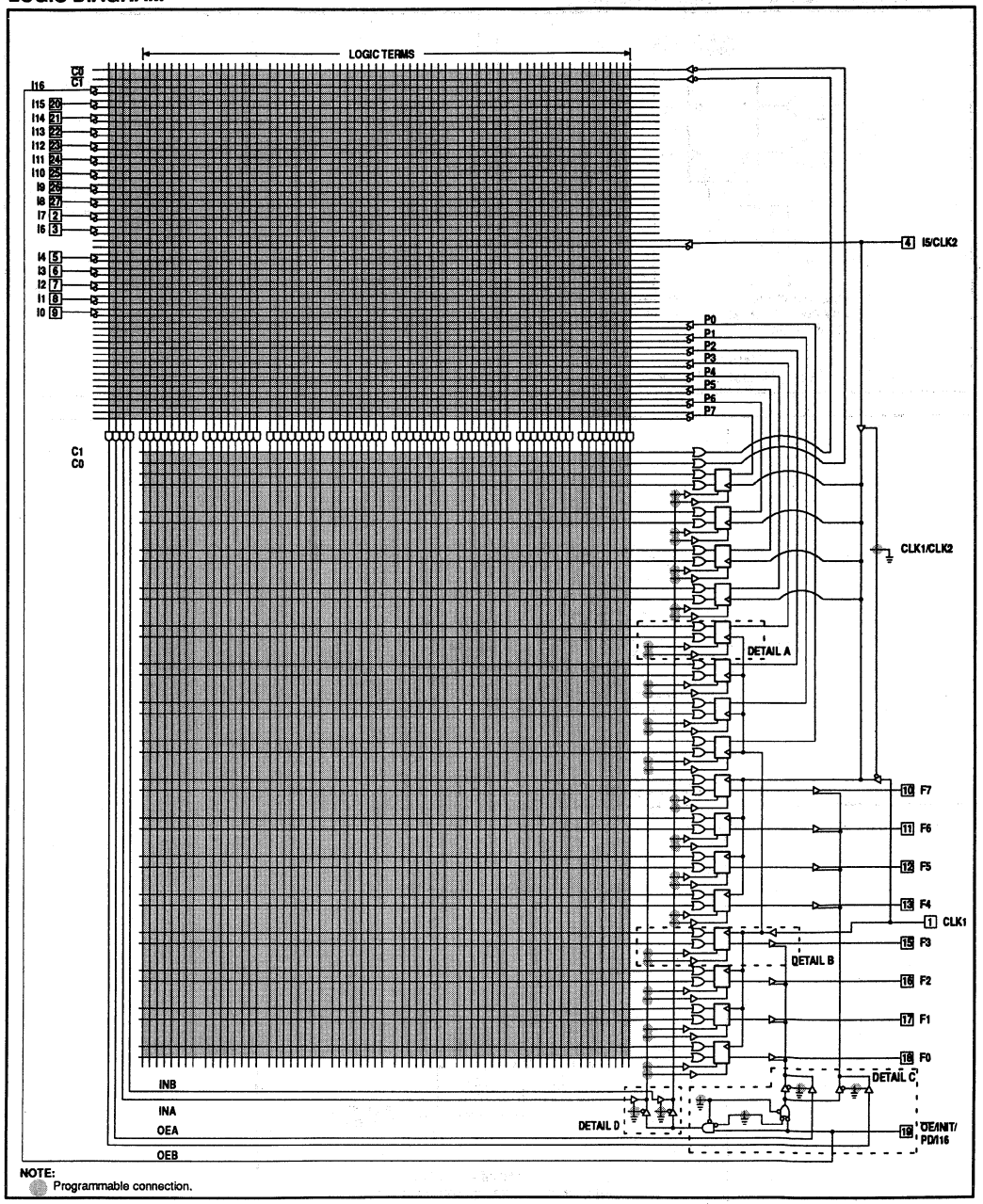
FUNCTIONAL DIAGRAM

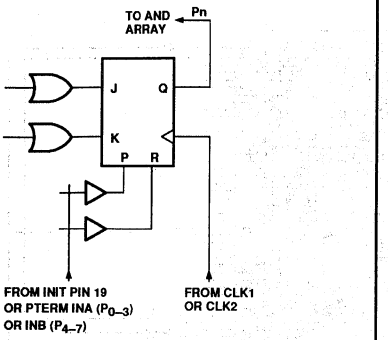


LOGIC DIAGRAM

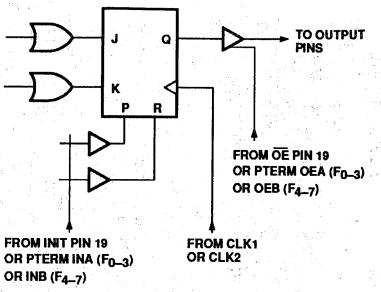


NOTE:
● Programmable connection.

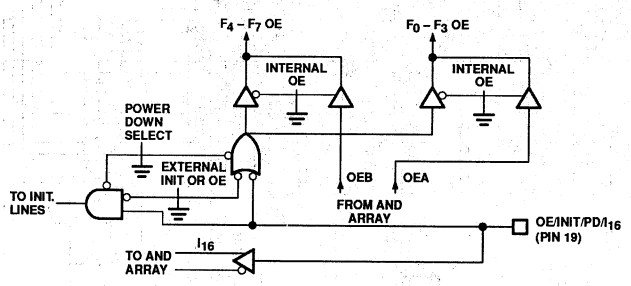
DETAILS FOR PLC415–16 LOGIC DIAGRAM



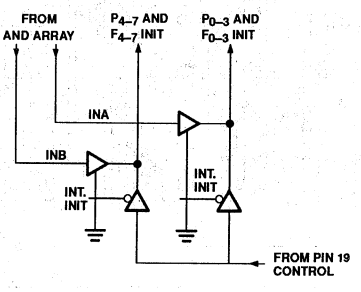
Detail A
State Registers $P_0 - P_7$



Detail B
Output Registers $F_0 - F_7$

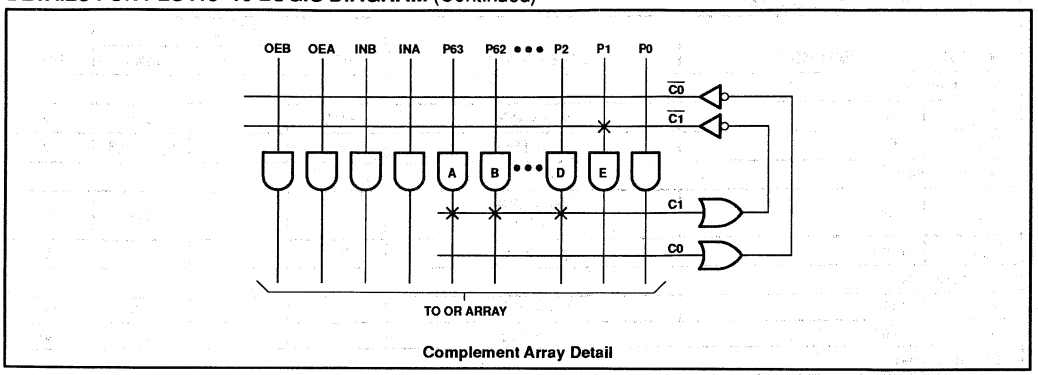


Detail C
Pin 19 Options: $\overline{OE}$, Initialization, Power Down and Input 16



Detail D
Internal and External Initialization

DETAILS FOR PLC415–16 LOGIC DIAGRAM (Continued)



Complement Array Detail

The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A • /B • /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLC415–16 has 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

Note that use of the Complement Array adds an additional delay path through the device. Please refer to the AC Electrical Characteristics for details.

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION		LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage[2]							
V_{IL}	Low	V_{CC} = MIN		–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V_{CC} + 0.3	V
Output voltage[2]							
V_{OL}	Low	V_{CC} = MIN I_{OL} = 16mA				0.5	V
V_{OH}	High	I_{OH} = –3.2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				–10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND				10 –10	µA µA
I_{OS}	Short-circuit [3, 6]	V_{OUT} = GND				–130	mA
I_{CCSB}	V_{CC} supply current with PD asserted[7]	V_{CC} = MAX V_{IN} = 0 or V_{CC}			50	100	µA
I_{CC}	V_{CC} supply current Active [4, 5]	I_{OUT} = 0mA	at f = 1MHz			55	mA
	(TTL or CMOS Inputs)	V_{CC} = MAX	at f = MAX			80	mA
Capacitance							
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V			12		pF
C_B	I/O	V_B = 2.0V			15		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, I_{CC} vs Frequency (worst case).
6. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.
7. The outputs are automatically 3-Stated when the device is in the Power Down mode. To achieve the lowest possible current, the inputs and clocks should be at CMOS static levels.

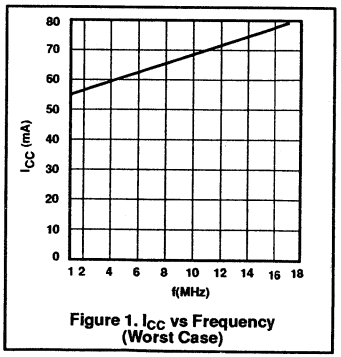

Figure 1. I_{CC} vs Frequency (Worst Case)

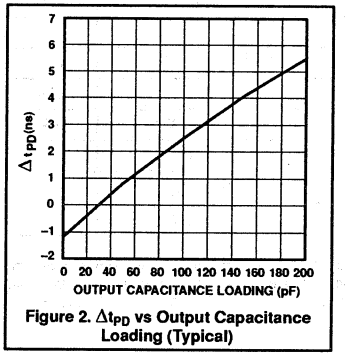

Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

$R_1 = 252\Omega$, $R_2 = 178\Omega$, $0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Pulse width								
t_{CKH}	Clock High	CK+	CK–	30pF	25	10		ns
t_{CKL}	Clock Low	CK–	CK+	30pF	25	10		ns
t_{INITH}	Initialization Input pulse	INIT+	INIT–	30pF	20			ns
Set–up time								
t_{IS1}	Input	(I) +/–	CK+	30pF	38	25		ns
t_{IS2}[1]	Input through Complement array	(I) +/–	CK+	30pF	60	40		ns
t_{ISPD}	Power Down Setup (from PD pin)	PD+	CK+	30pF	38	15		ns
t_{ISPU}	Power Up Setup (from PD pin)	PD–	First Valid CK+	30pF	38	30		ns
t_{VS}[1]	Power on Preset Setup	V_{CC}+	CK–	30pF	0			ns
t_{VCK1}	Clock resume (after INIT) when using INIT pin (pin 19)	INIT–	CK–	30pF	10	–5		ns
t_{VCK2}[1]	Clock resume (after INIT) when using P-term INIT (from AND array)	(I) +/–	CK–	30pF	20	8		ns
t_{NVCK1}	Clock lockout (before INIT) when using INIT pin (pin 19)	CK–	INIT–	30pF	10	–3		ns
t_{NVCK2}[1]	Clock lockout (before INIT) when using P-term INIT (from AND array)	CK–	INIT–	30pF	0	–5		ns
Propagation delays								
t_{CKO}	Clock to Output	CK+	(F) +/–	30pF		15	22	ns
t_{PDZ}	Power Down to outputs off	PD+	Outputs Off	5pF		25	30	ns
t_{PUA1}	Power Up to outputs Active with dedicated Output Enable	PD–	Outputs Active	30pF		20	35	ns
t_{PUA2}[1]	Power Up to outputs Active with P-term Output Enable[1]	PD–	Outputs Active	30pF		37	55	ns
t_{IHPU}	Last valid clock to Power Down delay (Hold)	Last Valid Clock	PD+	30pF	25	15		ns
t_{IHPD}	First valid clock cycle before Power Up	Beginning of First Valid Clock Cycle	PD–	30pF	0	–25		ns
t_{OE1}[3]	Output Enable: from /OE pin	OE–	Output Enabled	30pF		15	30	ns
t_{OE2}[1]	Output Enable; from P–term	(I) +/–	Output Enabled	30pF		25	40	ns
t_{OD1}[3]	Output Disable; from /OE pin	OE+	Output Disabled	5pF		20	30	ns
t_{OD2}[3]	Output Disable; from P-term	(I) +/–	Output Disabled	5pF		30	40	ns
t_{INIT1}	INIT to output when using INIT pin	INIT+	(F) +/–	30pF		22	35	ns
t_{INIT2}	INIT to output when using P-term INIT	(I) +/–	(F) +/–	30pF		35	45	ns
t_{PPR}[1]	Power-on Preset ($F_n = 1$)	V_{CC} +	(F) +	30pF			15	ns
t_{RP1}	Registered operating period; ($t_{IS1} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF		40	60	ns
t_{RP2}[1]	Registered operating period with Complement Array ($t_{IS2} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF		55	75	ns

Notes on following page

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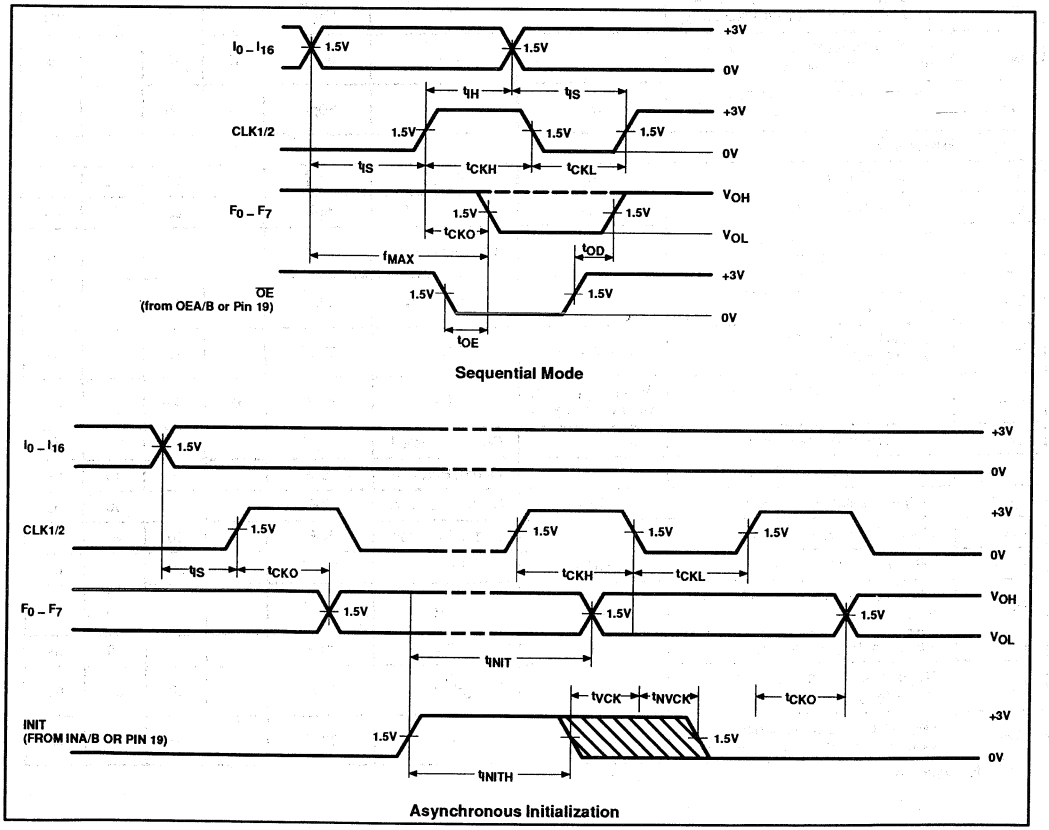
AC ELECTRICAL CHARACTERISTICS (Continued)

$R_1 = 252\Omega$, $R_2 = 178\Omega$, $0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Hold time								
t_{IH}	Input Hold	CK+	(F) +/–	30pF		–10	0	ns
Frequency of operation								
f_{CLK}[1]	Clock (toggle) frequency	C+	C+	30pF	20	50		MHz
f_{MAX1}	Registered operating frequency ($t_{IS1} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF	16.7	25		MHz
f_{MAX2}	Registered operating frequency with Complement Array ($t_{IS2} + t_{CKO1}$)	(I) +/–	(F) +/–	30pF	13.3	18.2		MHz

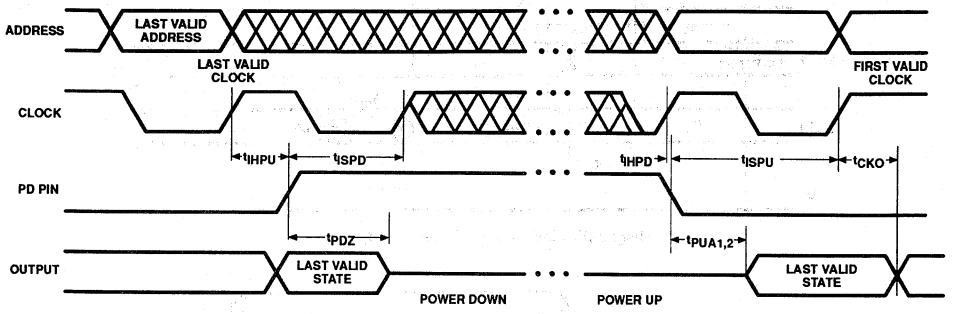
NOTE:
1. Not 100% tested, but guaranteed by design/characterization.
2. All propagation delays and setup times are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TIMING DIAGRAMS

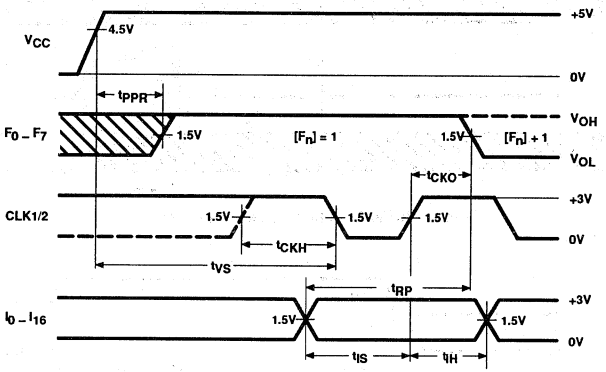


The PLC415–16 has a unique power down feature that is ideal for power sensitive controller and state machine applications. During idle periods, the PLC415 can be powered down to a near zero power consumption level of less than 100 micro Amps. Externally controlled from Pin 19, the power down sequence first saves the data in all the State and Output registers. In order to insure that the last valid states are saved, there are certain hold times associated with the first and last valid clock edges and the Power Down input pulse. The Outputs are then automatically 3-Stated and power consumption is reduced to a minimum. Once in the power down mode, any or all of the inputs, including the clocks, may be toggled without the loss of data. To obtain the lowest possible power level, the inputs should be at static CMOS input levels during the power down period.

TIMING DIAGRAMS (Continued)

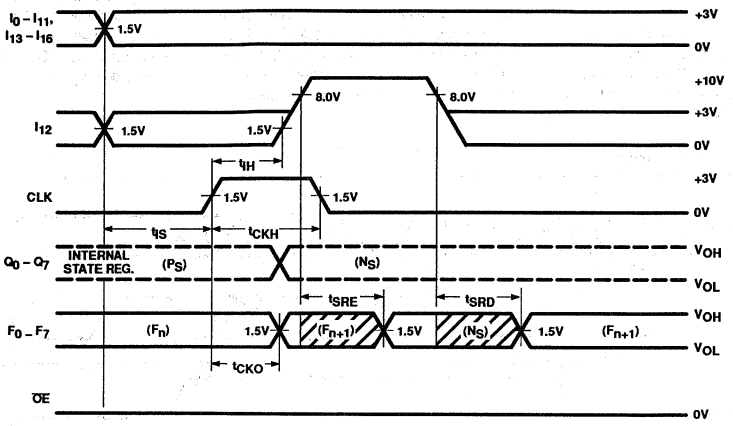


Power Down Enable and Disable

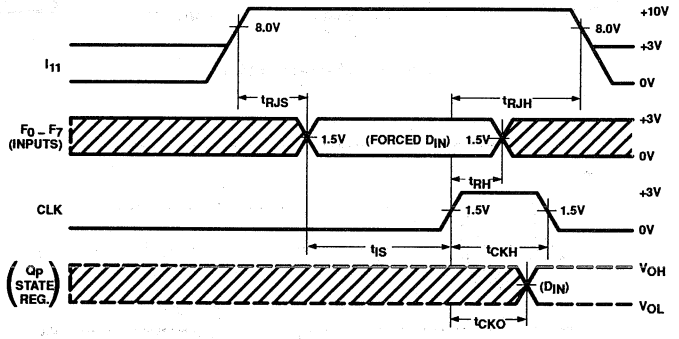


Power-On Preset

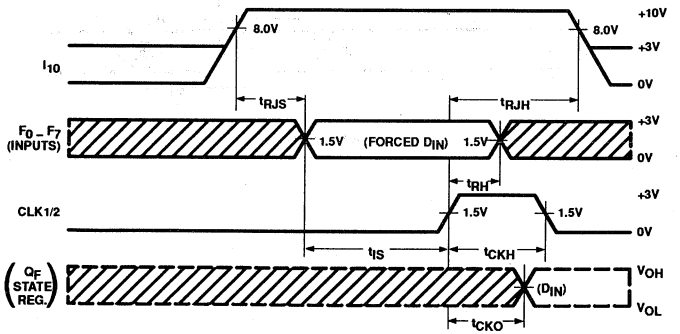
TIMING DIAGRAMS (Continued)



Diagnostic Mode—State Register Outputs



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—Output Register Input Jam

TIMING DEFINITIONS

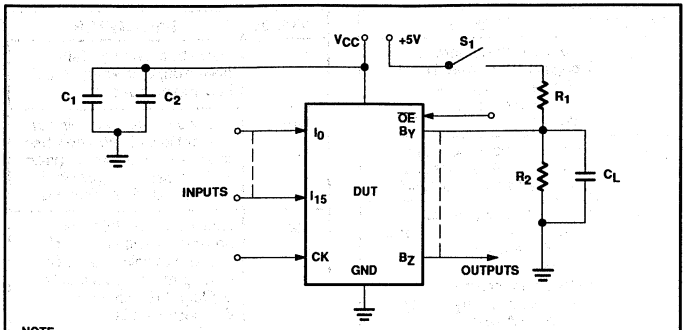
SYMBOL	PARAMETER
f_{CLK}	Minimum guaranteed toggle frequency of the clock (from Clock HIGH to Clock HIGH).
$f_{MAX1,2}$	Minimum guaranteed operating frequency.
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{RP1}	Minimum guaranteed operating period – when not using Complement Array.
t_{RP2}	Minimum guaranteed operating period – when using Complement Array.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with outputs enabled).
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IHPD}	Required delay between the positive transition of the beginning of the first valid clock cycle to the beginning of Power Down LOW to insure that the last valid states are intact and that the next positive transition of the clock is valid.
t_{IHPU}	Required delay between the positive transition of the last valid clock and the beginning of Power Down HIGH to insure that last valid states are saved.
t_{INITH}	Width of initialization input pulse.
t_{INIT1}	Delay between positive transition of Initialization and when Outputs become valid when using external INIT control (from pin 19).
t_{INIT2}	Delay between positive transition of Initialization and when outputs become valid when using internal INIT control (from P-terms INA and INB).
t_{ISPD}	Required delay between the beginning of Power Down HIGH (from pin 19) and the positive transition of the next clock to insure that the clock edge is not detected as a valid Clock and that the last valid states are saved.

SYMBOL	PARAMETER
t_{ISPU}	Required delay between the beginning of Power Down LOW and the positive transition of the first valid clock.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{NVCK1}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization when using external INIT control (from pin 19) to guarantee that the clock edge is not detected as a valid negative transition.
t_{NVCK2}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization, when using the internal INIT control (from P-terms INA and INB), to guarantee that the clock edge is not detected as a valid negative transition.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-State, when using external OE control (from pin 19).
t_{OD2}	Delay between beginning of Output Enable High and when outputs are in the OFF-State when using internal OE control (from P-terms OEA and OEB).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid when using external OE control from pin 19.
t_{OE2}	Delay between beginning of Output Enable Low and when outputs become valid when using internal OE control (from P-terms OEA and OEB).
t_{PDZ}	Delay between beginning of Power Down HIGH and when outputs are in OFF–State and the circuit is "powered down".

SYMBOL	PARAMETER
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
$t_{PUA1,2}$	Delay between beginning of Power Down LOW and when outputs become Active (valid) and the circuit is "powered up". See AC Specifications.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{RJH}	Required delay between positive transition of Clock and end of inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively.
t_{RJS}	Required delay between when inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the output pins become available as inputs.
t_{SRD}	Delay between input I_{12} transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I_{12} transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VCK1}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding the first valid clock pulse when using external INIT control (pin 19).
t_{VCK2}	Required delay between the negative transition of the Asynchronous Initialization and the negative transition of the clock preceding the first valid clock pulse when using internal INIT control (from P–terms INA and INB).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.

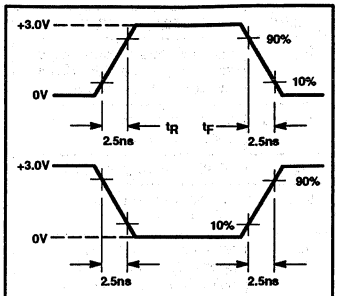
8

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

LOGIC PROGRAMMING

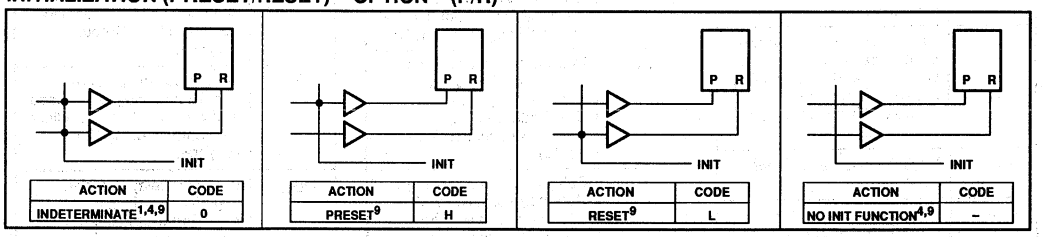
The PLC415–16 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics AMAZE, SLICE and SNAP design software packages. ABEL™ and CUPL™ design software packages also support the PLC415–16 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC415–16 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by AMAZE and SLICE only. Both AMAZE and SLICE design packages are available, free of charge, to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations if assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION (PRESET/RESET)[11] OPTION – (P/R)



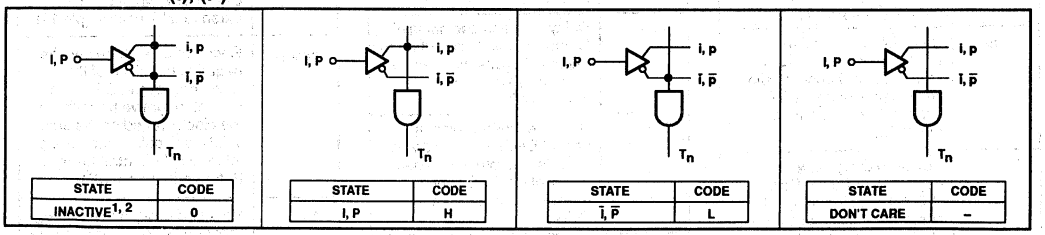
ACTION	CODE
INDETERMINATE[1,4,9]	0

ACTION	CODE
PRESET[9]	H

ACTION	CODE
RESET[9]	L

ACTION	CODE
NO INIT FUNCTION[4,9]	–

"AND" ARRAY – (I), (P)



STATE	CODE
INACTIVE[1, 2]	0

STATE	CODE
I, P	H

STATE	CODE
$\bar{I}, \bar{P}$	L

STATE	CODE
DON'T CARE	–

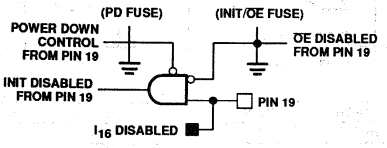
Notes on page 8-138

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

LOGIC PROGRAMMING (Continued)

PIN 19 FUNCTION: POWER DOWN, INIITALIZATION, $\overline{OE}$, OR INPUT

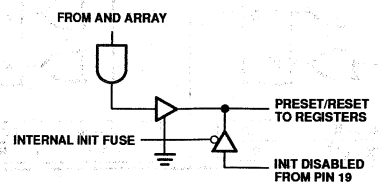
Power Down Mode



POWER DOWN FUSE	CODE
PIN 19 AS POWER DOWN	H[6]

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
EXTERNAL INIT/$\overline{OE}$ DISABLED	L

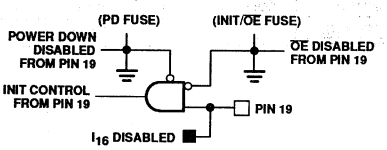
P-Term Initialization Control



INTERNAL INIT FUSES	CODE
P-TERM INIT CONTROL	H[7, 8]

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Initialization Control

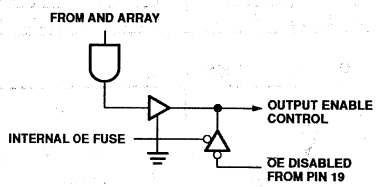


PD FUSE	CODE
POWER DOWN DISABLED	L[1]

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
PIN 19 AS EXTERNAL INIT	L[1]

INTERNAL INIT FUSES	CODE
P-TERM INIT ACTIVE OR INACTIVE	H OR L[7, 8]

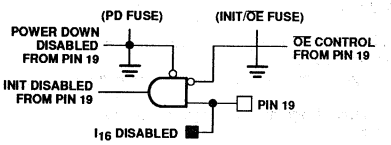
P-Term OE Control



INTERNAL OE FUSES	CODE
P-TERM OE CONTROL	H[7, 8]

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Output Enable Control



PD FUSE	CODE
POWER DOWN DISABLED	L

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
PIN 19 AS EXTERNAL $\overline{OE}$	H

INTERNAL INIT FUSES	CODE
P-TERM $\overline{OE}$ ACTIVE OR INACTIVE	H OR L[7, 8]

Notes are on page 17.

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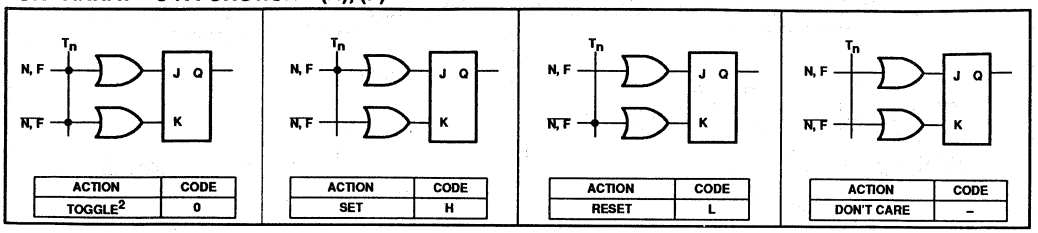
LOGIC PROGRAMMING (Continued)

"OR" ARRAY – J-K FUNCTION – (N), (F)



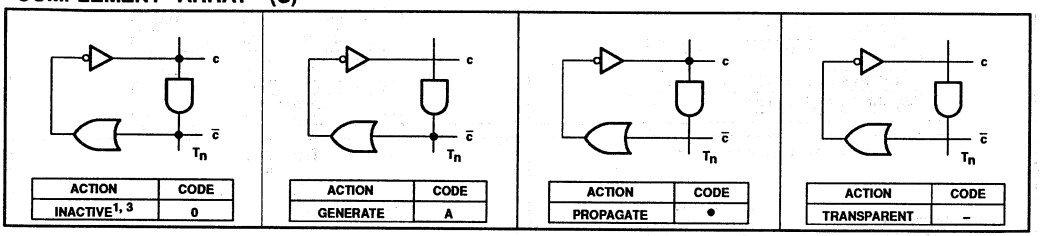
ACTION	CODE
TOGGLE[2]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



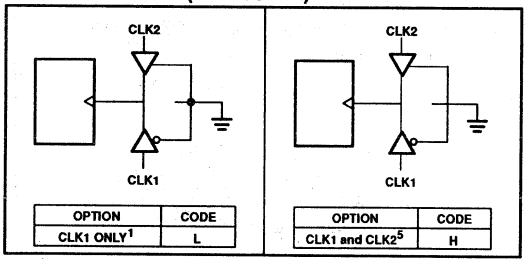
ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

CLOCK OPTION – (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using PRESET/RESET option.
5. Input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. When using Power Down feature, INPUT 16 is automatically disabled via the design software.
7. If the internal (P–term) control fuse for INIT and/or OE is programmed as Active High, the associated External Control function will be permanently disabled, regardless of the state of the External INIT/OE fuse.
8. One internal control fuse exists for each group of 8 registers. P_{0-3} and F_{0-3} are banked together in one group, as are P_{4-7} and F_{4-7}. Control can be split between the INIT/OE pin (Pin 19) and P–terms INA, INB, OEA and OEB.
9. The PLC415–16 also has a power–up preset feature. This feature insures that the device will power–up in a known state with all register elements (State and Output Register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.
10. L = cell unprogrammed.
    H = cell programmed.
11. Inputs 10, 11 and 12 (pins 25, 24, & 23) can be used for supervoltage diagnostic mode tests. It is recommended that these inputs not be connected to product terms INA, INB, OEA or OEB if you intend to make use of the diagnostic modes due to the fact that the patterns associated with the internal INIT and OE control product terms may interfere with the diagnostic mode data loading and reading.

PROGRAM TABLE

AND

(Im, Ps)		(Cn)	
INACTIVE	O	INACTIVE	O
I, P	H	GENERATE	A
$\overline{I}$, $\overline{P}$	L	PROPAGATE	•
DON'T CARE	–	TRANSPARENT	–

OR (Ns, Fn)

TOGGLE	O
SET	H
RESET	L
NO CHANGE	–

OPTIONS

EXTERNAL INIT	L
EXTERNAL OE	H
INTERNAL INIT/OE ENABLED	H
INTERNAL INIT/OE DISABLED	L
POWER DOWN ENABLED	H
POWER DOWN DISABLED	L
CLOCK 1 ONLY	L
CLOCK 1 AND 2	H

INITIALIZATION	
PRESET	H
RESET	L
NO INIT	–
INDETERMINATE	O

PROJECT NAME _____ DATE _____ REVISION _____

CUSTOMER NAME _____ SIGNETICS PART # _____ CUSTOMER PART # _____

TERMS	COMP. ARRAY	INTERNAL INIT		INTERNAL OE		EXTERNAL INIT/OE	CLK 1/1&2	PD	INITIALIZATION																			
		INB	INA	OEB	OEA																							
	NOR	AND							OR																			
	Cn	INPUT (Im)							PRESENT STATE (Ps)								NEXT STATE (Ns)								OUTPUT (Fn)			
	C1	C0	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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PIN NO.		19	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9																	10	11	12	13	15	16	17	18
PIN LABELS																																									

NOTES:

1. In the unprogrammed state all cells are conducting. Thus, the program table for an unprogrammed device would contain "0"s for all product terms (inactive) and initialization states (indeterminate). The default or unprogrammed state of all other options is "L".
2. Unused Cn, Im and Ps cells are normally programmed as Don't Care (–).
3. Unused product terms can be left blank (inactive) for future code modification.

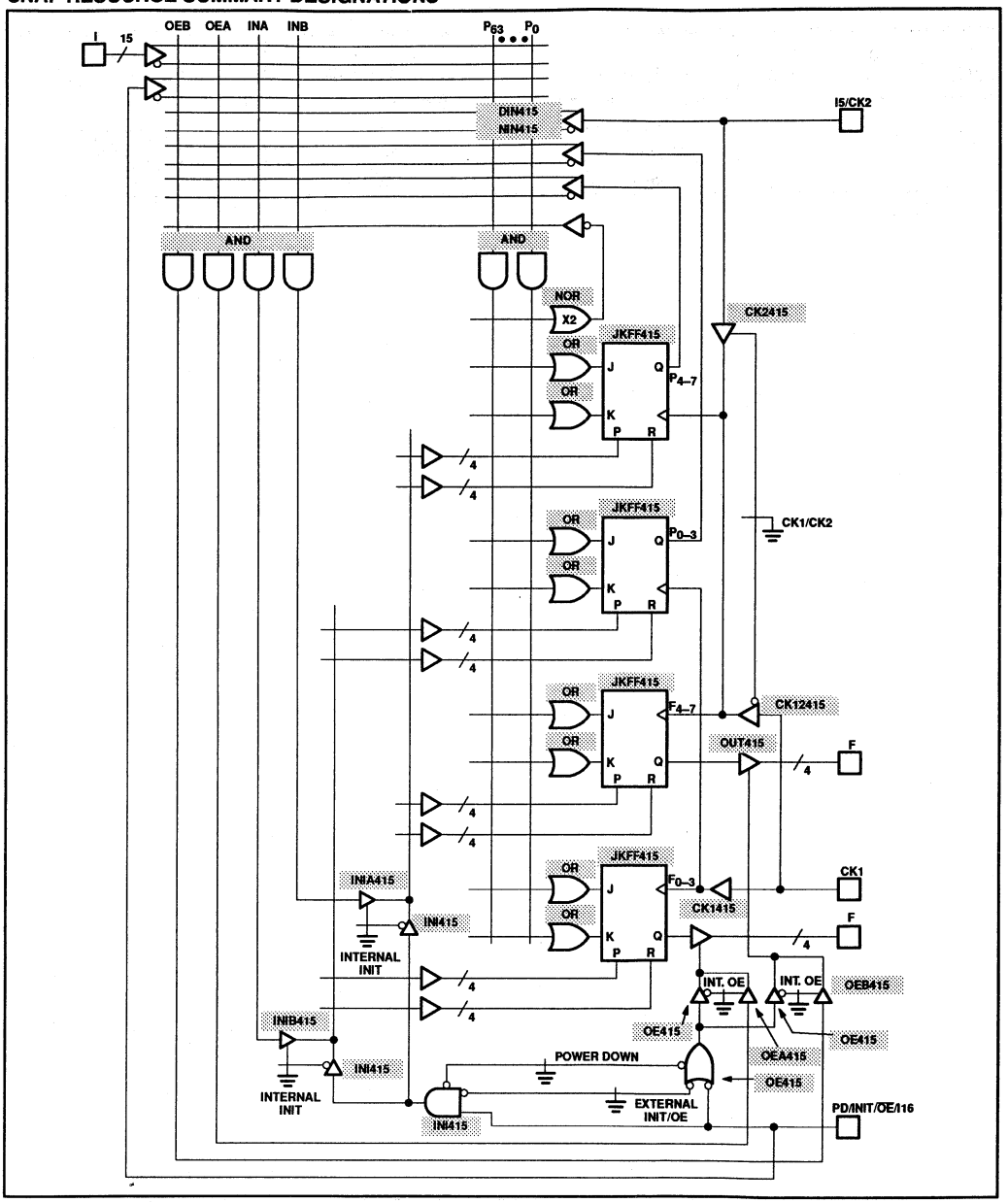
ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC415 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps has wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC415 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC415 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC415 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

SNAP RESOURCE SUMMARY DESIGNATIONS



t_{PD} (MHz)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
16	38	22	ATS415-16DC ATS415-16JC ATS415-16PC	28DW6 28J 28P6	Commercial (0°C to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)

Features

- 68 Pins
- 24 I/O Pins
- 29 Dedicated Inputs
- 52 Flip-Flops
- Foldback NAND Structure
- Full Connectivity
- Erasable Version and One Time Programmable Version Available
- Scan Test
- Power Down Mode
- Power on Reset
- 100% Testable
- Power Dissipation (TTL) = 630 mW
- Power Dissipation (CMOS) = 525 mW
- Power Dissipation (Power-Down Mode) = 52 mW
- Security Fuse for Copy Protection
- Reprogrammable
- Second Source to Signetic's PML2552

CMOS High Density Programmable Macro Logic

8

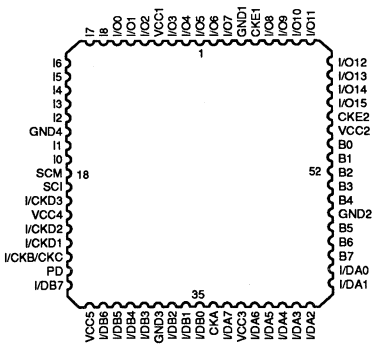
Description

The Atmel ATS2552 provides "instant gate array" capabilities for general purpose logic integration applications. Fabricated in Atmel's high-performance EPROM process, it is an ideal way to reduce NRE costs, inventory problems, and quality concerns. The ATS2552 incorporates a folded NAND array architecture which provides 100% connectivity to eliminate routing restrictions. What distinguishes the ATS2552 from the "classic" PLD architectures is its flexibility and the potent flip-flop building blocks. The device utilizes a folded NAND architecture, which enables the designer to implement multiple levels of logic on a single chip. The ATS2552 eliminates the NRE costs, risks, and hard to use design tools associated with semicustom and full custom approaches. It allows the system designer to manage reliable functionality, in less time and space plus a faster time to market. The ATS2552 is ideal in today's instrumentation, industrial control, EISA, bus interface and dense state machine applications in conjunction with the state-of-the-art CMOS processors. It is capable of replacing large amounts of TTL, SSI and MSI logic and literally allows the designer to build a system on the chip.

Development software gives easy access to the density and flexibility of the ATS2552 through a variety of design entry formats, including schematic, logic equations, and state equations in any combination. The ATS2552 is supported by Signetic's SNAP and SLICE development systems, as well as third-party tools such as ABEL™ and CUPL™.

Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply



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CUPL™ is a trademark of Logical Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM

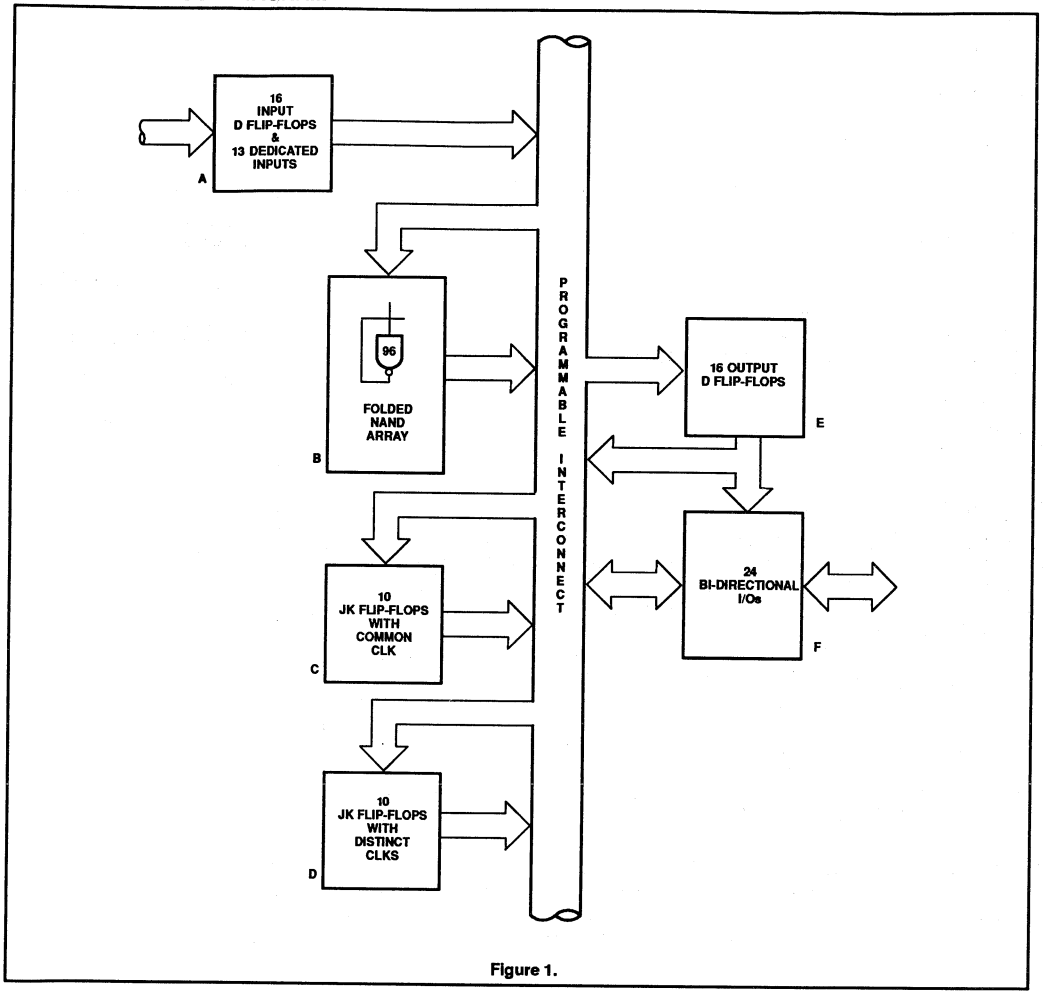
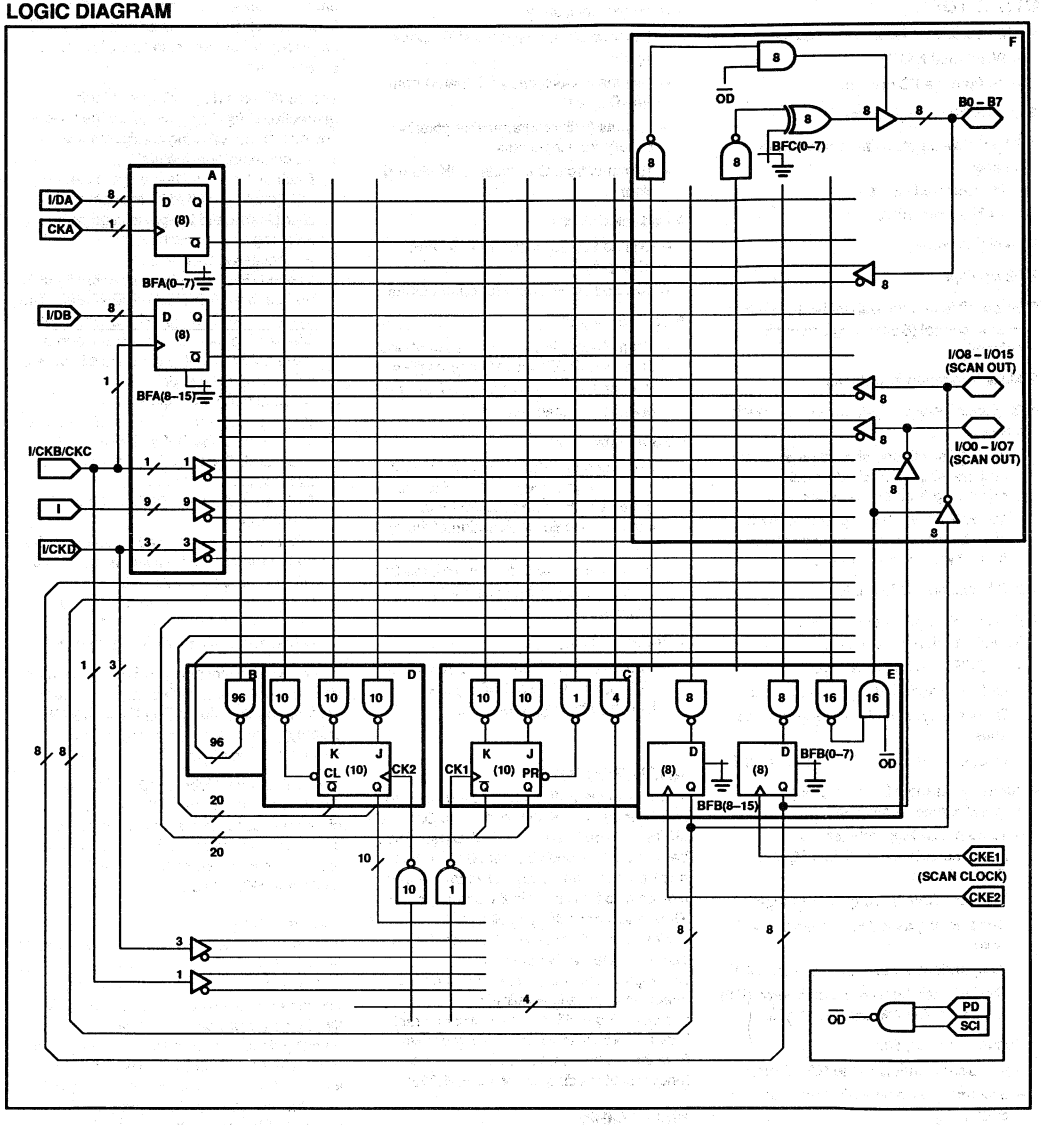


Figure 1.

LOGIC DIAGRAM



STRUCTURE

- 112 possible foldback NAND gates:
  - 96 internal NAND
  - 16 from the I/O macros
- 114 additional logic terms
- 53 possible inputs (with programmable polarity)
  - 29 dedicated inputs
  - 24 bidirectional I/Os
- 24 bidirectional pins
- 52 flip-flops
- 24 possible outputs with individual Output Enable control (8 with programmable polarity)
- Multiple independent clocks
- 20 Buried JK-type flip-flops with foldback (JKFFs):
  - 10 JKFFs with one shared preset signal and one shared clocked signal originating from the clock array.
  - 10 JKFFs with 10 independent clock signals originating from the clock array and 10 independent clear signals
- 258 inputs per NAND gate
- Bypassable Input D-type flip-flop (DFFs)/Combinatorial Inputs:
  - 16 DFFs/combinatorial inputs
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
- Inputs/bypassable D-type flip-flop outputs/foldback NAND gates:
  - 16 output DFFs/combinatorial inputs/outputs with individual Output Enable control
  - DFFs clocked in two groups of eight
  - DFFs not bypassed in unprogrammed state
  - Independent bypass fuse on each DFF
  - The DFF can be used as an internal DFF or an internal foldback NAND gate.
- Combinatorial inputs:
  - 9 dedicated inputs to the NAND array
  - 3 inputs optional to NAND array and/or clock array
  - 1 input optional to NAND array and/or clock array, and/or clock of Input D Flip-Flops (Group B)
- Separate clock array:
  - Separate clock array for JKFFs clock inputs
  - 4 inputs to clock array originated from NAND array
  - 4 inputs (with programmable polarity) directly from input pins
  - 10 inputs from Q outputs of JKFFs with clear
- Dedicated clocks:
  - One dedicated clock for input DFFs (Group A)
  - Two dedicated clocks for output DFFs
- Scan test feature:
  - Scan chain is implemented through the 20 buried JKFFs and 16 output DFFs
  - Pins SCI, SCM, and CKE1 are used to operate the scan test
- Power down mode
  - Dedicated pin (PD) freezes the circuit when brought to logic "1". The circuit remains in the same state prior to the logic "0" to logic "1" transition of the "PD" pin.
  - When in the power down mode, the SCI pin acts as the 3-State pin for the 24 outputs.
- Power on reset:
  - All flip-flops (16 input DFFs, 20 buried JKFFs, and 16 output DFFs) are reset to logic "0" after V_{CC} power on.

ARCHITECTURE

The core of the PML2552 is a programmable NAND array of 96 NAND gates and 20 buried JKFFs. The output of each NAND gate folds back upon itself and all other NAND gates and flip-flops. The 'Q' and '$\overline{Q}$' output of each flip-flop also folds back in the same manner. Thus, total connectivity of all logic functions is achieved in the PML2552. Any logic function can be created within the core without wasting valuable I/O pins. Furthermore, a speed advantage is acquired by implementing multi-level logic within a fast internal core without incurring any delays from the I/O buffers. Figure 1 shows the functional block diagram of the PML2552.

Macro Cells

There are 16 bypassable DFFs on the input to the NAND array. These flip-flops are split in two banks of 8 (Bank A and Bank B). Each bank of flip-flops has a common clock. In the unprogrammed state of the device the flip-flops are active. In order to bypass any DFF, its respective bypass fuse (BFA_X) must be programmed.

The 16 I/O pins (IO_0 - IO_{15}) and their respective D flip-flop macros can be used in any one of the following configurations:

1. As combinatorial input(s).
   Each of the 16 3-State outputs can be individually disabled by the associated NAND term and the pin is used as an inverting or non-inverting input.
2. As registered DFF outputs.
   These DFFs are split into two banks of 8, and each bank is clocked separately. The bypass fuse BFB_X (see PML2552 Logic Diagram) is used to bypass any one of these DFFs. The flip-flops are all active in an unprogrammed device.
3. As combinatorial outputs.
   By programming the bypass (BFB_X) fuse of any one of the DFFs, the flip-flop(s) is bypassed. The I/O pin can then be used as a combinatorial output.
4. As Internal foldback DFFs or foldback NAND gates.
   When the I/O pin is used as an input, the output macro can be used as an internal DFF or a foldback NAND term. If the bypass fuse is programmed, the macro will act as a foldback NAND term. Otherwise it will act as an internal DFF.

The 8 bidirectional pins (B0-B7) can be used as either combinatorial inputs or outputs with programmable polarity. The Exclusive-OR polarity gates are non-inverting in the unprogrammed state.

The NAND signal labeled '$\overline{OD}$' (Output Disable) shown on the PML2552 logic diagram is used for the Power Down mode operation. This signal disables the outputs when the device enters the Power Down mode and SCI is high.

Clock Array

The 20 buried JKFFs can be clocked through the 'Clock Array'. The Clock Array consists of 11 NAND terms. Ten of these terms are connected to the clock inputs of the Bank A flip-flops that can be clocked individually. One NAND gate is connected to Bank B flip-flops that have a common clock. There are 18 inputs to the clock array. Four come directly from the input pins (with programmable polarity), 4 inputs are from 4 NAND gates connected directly to the folded NAND array. 10 inputs are from the Q outputs of the JKFFs with clear.

SCAN TEST FEATURE

With the rise in the ratio of devices on a chip to the number of I/O pins, Design For Testability is becoming an essential factor in logic design methodology. The PML2552 incorporates a variable length scan test feature which permits access to the internal flip-flop nodes without requiring a separate external I/O pin for each node accessed. Figure 2 (Scan Mode Operation) shows how a scan chain is implemented through the 20 buried JKFFs and 16 output DFFs. Two dedicated pins, SCI (Scan In) and SCM (Scan Mode), are used to operate the scan test. The SCM pin is used to put the circuit in scan mode. When this pin is brought to a logic "1", the circuit enters the scan mode.

In this mode it is possible to shift an arbitrary test pattern into the flip-flops. The SCI pin is used to input the pattern. The inverted outputs of flip-flops D0 - D15 are observable on pins I/O0 - I/O15.

The following are features and characteristics of the device when in Scan Mode:

1. CKE1 is the common scan-clock for all the flip-flops when in scan mode. CKE1 overrides all clock resources of normal operational mode.
2. The Preset (PR) and Clear (CL) functions of the flip-flops are disabled.
3. Scan overrides the bypass fuse of the flip-flops. This means that all the bypassable DFFs remain intact during scan operation even though they may have been bypassed during normal operation.
4. To observe the SCAN data, the output buffers must be enabled by the Output Enable (tri-ctrl) terms.
5. The outputs of the flip-flops are complemented on pins I/O0 - I/O15.
6. All external inputs to flip-flops in the scan chain are disabled when the device enters the scan mode.
7. Blowing the security fuse does not disable the Scan Test feature.

SCAN MODE OPERATION

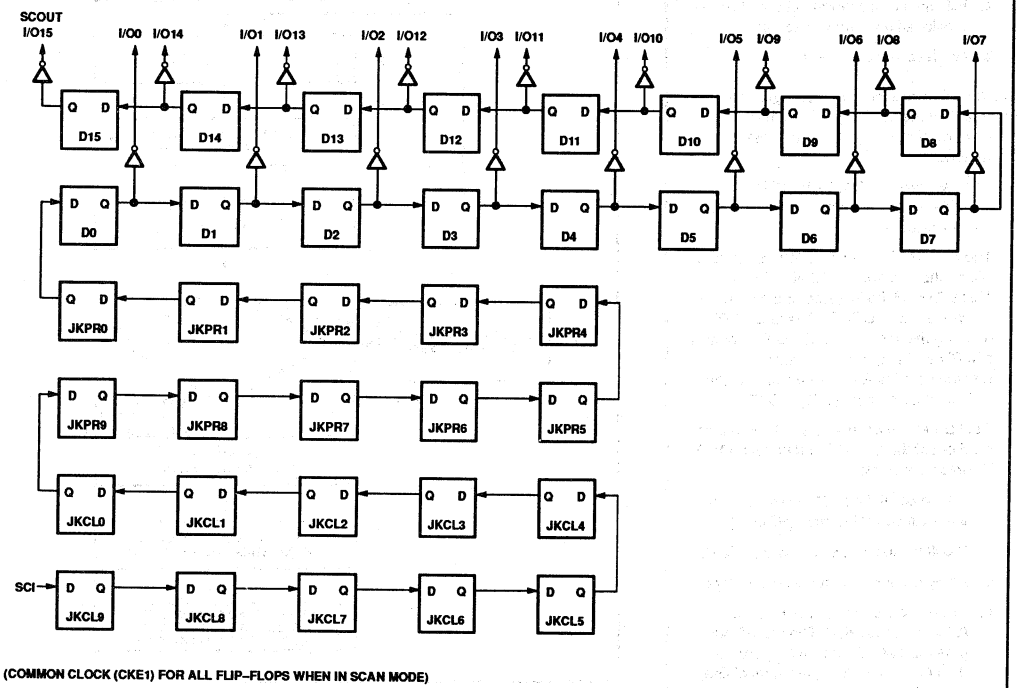


Figure 2.

SCAN TEST STRATEGY

The scan test pattern is design dependent and the user must make considerations for Design For Testability (DFT) during the initial stages of the design. A typical test sequence is to pre-load (i.e., enter a state); revert to normal operation (i.e., activate the next state transition); go back to scan mode to check the result. Note that the scan test feature available in the PML2552 is a variable length scan chain. The DATA entered at SCI (JKCL9) can be accessed anywhere between 21 clock cycles (at I/O0) to 36 clock cycles (at I/O15). For the strategy discussed here, DATA is read out after 36 clocks at I/O15 (i.e., D15). The following operation sequence suggests a possible scan test method.

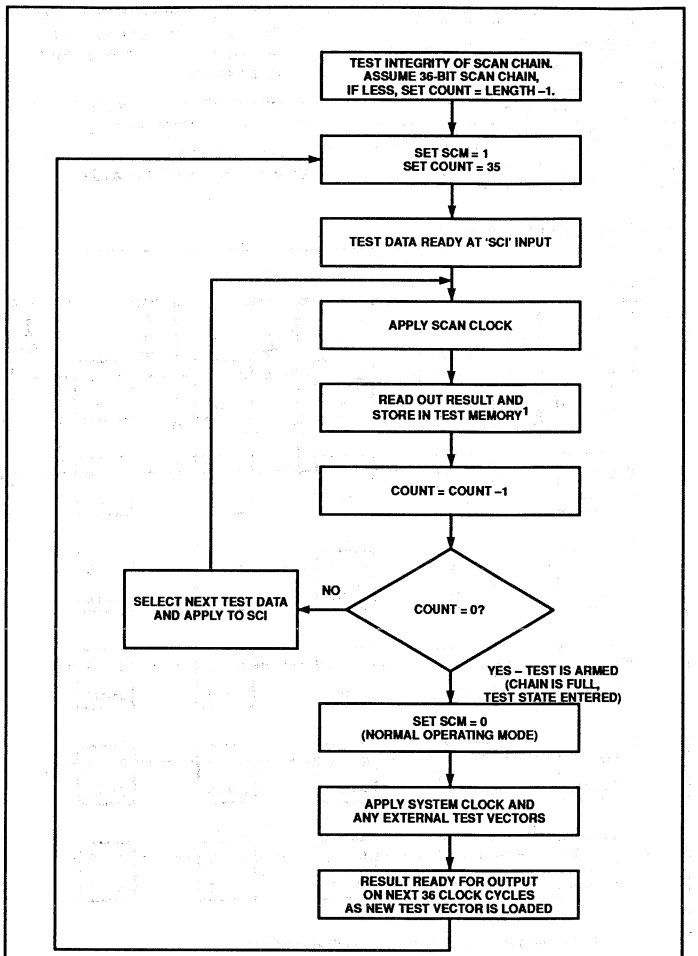
A conservative test policy demands proof that the test facility is working. Thus, to prove Scan Chain holds and maintains correct data:

a. Fill chain with several patterns (for example, all ones and all zeros).

b. Retrieve same patterns.

The user is responsible for managing an external test memory buffer for applied vectors and results, as part of the test equipment.

1. Parallel readout of I/O0 - I/O15 is possible, but assume only I/O15 is used for this strategy.
2. The first DATA entered at SCI (or JKCL9) will be the content of D15 after 36 clocks. This DATA will be inverted at the output pin I/O15 (i.e., SCOUT). The last DATA entering the scan chain will be the content of JKCL9. Thus, the scan chain resembles a first-in-first-out shift register with inverted outputs (I/O0 - I/O15).
3. 'Test Data' is read in at the SCI input and read out of the SCOUT output pin (I/O15). To enter 'Test Data':
   a. Put device in Scan Mode by applying the scan control signals (SCM=1).
   b. Clock device with scan clock (CKE1).
   c. Apply consecutive serial test vectors.
   d. Read back results as new 'Test Data' (States) are applied. The first 36 outputs read at SCOUT (I/O15) are random ('old') data (e.g., remnant of Step 1).
   e. Apply 36 'Test Data' until the chain is full.
4. To apply 'Test Data' (States), exit Scan Mode and apply on system clock together with any other possible test vectors.
5. To read result of the state transition, re-enter scan and apply the scan clock (CKE1). The result of the state transition in JKCL9 will be available at SCOUT (I/O15) after 36 clocks. The results can be stored in a user defined test memory buffer in inverted logic representation.
6. As the results are being read and stored, new 'Test Data' can be entered via SCI.
7. Repeat for all test patterns of interest.
8. Figure 3 (FLOW_CHART) depicts a flow chart version of the test sequence.



NOTE:
1. The first 36 outputs are random ('OLD') data.

Figure 3. FLOW_CHART

A Simple Example

Assume the last three cells of the scan chain (JKCL9, JKCL8, JKCL7 in Figure 4 contain a 3-bit up counter. Our test vector will be a single clock applied to the counter. Suppose we wish to first check the *State 5* (i.e., 101) to *State 6* (i.e., 110) transition, then the *State 3* (i.e., 011) to *State 4* (i.e., 100) transition. Assume the scan chain has been pre-verified and we may begin.

Enter scan mode (set SCM=1)I apply 36 bits in sequence so that the value *101* (i.e., State 5) resides in the last three cells. Exit scan mode (set SCM=0) and apply a single clock to the counter. Now the value *110* (i.e., State 6) resides in the last three cells. Re-enter scan mode (set SCM=1) and read back 36 bits from position I/O15. Note that the outputs are complemented and are also read back in the reverse order. Therefore the value for *STATE 6* read at I/O15 will be 100 which is the complement of *STATE 6* (110) read in the reverse order.

As this is being read back, apply a new state, serially equal to the value *011* (i.e., State 3). This state should be loaded on the last three clock cycles during which *STATE 6* is being read back at I/O15. After *STATE 3* has been loaded (and *STATE 6* read back), exit scan mode and apply a single clock which will invoke the *STATE 3* (i.e., 011) to *STATE 4* (i.e., 100) transition. Re-enter scan mode and read back 36 bits at I/O15. The last three bits should contain *110* which is the complement of *State 4* read in the reverse order. Figure 4 (SCAN_EXAMPLE) shows a flow diagram of this example. Note that the States will always be complemented and read back in the reverse at I/O15. Other sequences may be applied in the same manner.

A possible alternative to this example is to read back the output states at I/O0 (D0) instead of I/O15 (JKCL9). This will allow the outputs to be read back after 21 clock cycles rather than the 36 used in the above example.

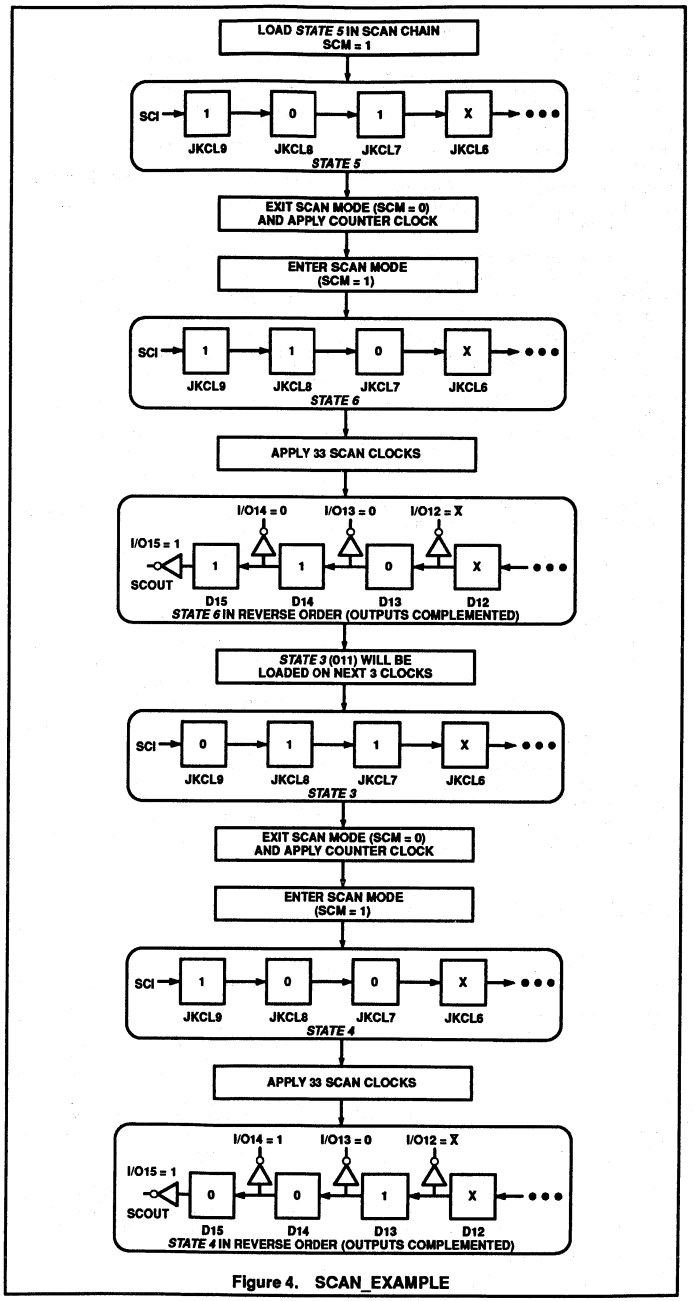


Figure 4. SCAN_EXAMPLE

POWER DOWN

The PML2552 offers the user controlled capability of putting the device to "sleep" where power dissipation is reduced to very low levels. When brought to a logic "1", the PD pin freezes the circuit while reducing the power. All data is retained. This not only includes that of the registers, but also the state of each foldback gate. For those cases where it is desirable to 3-State the outputs, that can be accomplished by raising the SCI pin to a logic "1".

There is one point that should be noted while the circuit is in its power-down mode. The switching of any external clock pin will cause a disruption of the data. All clocks must be frozen before the circuit goes into power-down and stay that way until it powered back up. Clocks that are internally generated and feed the clock array are automatically stopped by the power-down circuitry. Any other input can toggle without any loss of data.

NOTE:
1. During power down, external clocks (CKA, CKB/CKC, CKE1, CKE2) should not change.
2. SCM must be "0" as in normal operation mode.
3. External clock recovery time (low-to-high) is 60ns (high-speed) and 70ns (standard) after the device is powered up.
4. Power Down Timing Diagrams on pages 17 and 18 are for combinatorial operation only.

DEVELOPMENT TOOLS

The PM2552 is supported by the Signetics SNAP software development package and a multitude of hardware and software development tools. These include industry standard PLD programmers and CAD software.

SNAP

Features

- Schematic entry using DASH™ 4.0 or above or OrCAD™ SDT III
- State Equation Entry
- Boolean Equation Entry
- Allows design entry in any combination of above formats
- Simulator
  - Logic and fault simulation
  - Timing model generation for device timing simulation
  - Synthetic logic analyzer format
- Macro library for standard TTL and user defined functions
- Device independent netlist generation
- JEDEC fuse map generated from netlist

SNAP (Synthesis, Netlist, Analysis and Program) is a versatile development tool that speeds the design and testing of PML. SNAP combines a user-friendly environment and powerful modules that make designing with PML simple. The SNAP environment gives the user the freedom to design independent of the device architecture.

The flexibility in the variations of design entry methodologies allows design entry in the most appropriate terms. SNAP merges the inputs, regardless of the type, into a high-level netlist for simulation or compilation into a JEDEC fuse map. The JEDEC fuse map can then be transferred from the host computer to the device programer.

SNAP's simulator uses a synthetic logic analyzer format to display and set the nodes of the design. The SNAP simulator provides complete timing information, setup and hold-time checking, plus toggle and fault grading analysis.

SNAP operates on an IBM® PC/XT, PC/AT, PS/2, or any compatible system with DOS 2.1 or higher. A minimum of 640K bytes of RAM is required together with a hard disk.

SLICE

SLICE, which supports Atmel's PLD line, is easy to understand and simple to use. Select a PLD, assign input and output pins and enter the desired equations in either Boolean or state form. SLICE then checks the equations for errors. It automatically generates a JEDEC-format fuse map for downloading to a PLD programmer.

Fully menu driven, SLICE incorporates a fuse table editor for making quick modifications to the design and a test vector editor for input of test vectors.

A built-in Boolean equation extractor allows existing PLDs to be used as the basis for a new design. the extractor reads JEDEC information from a PLD and creates a file containing the corresponding Boolean equations. The result can then be used to consolidate several PLD designs into a single, denser part.

And SLICE is upward compatible with Signetics extensive design suite, SNAP.

DESIGN SECURITY

The PML2552 has a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary design implemented in the device cannot be copied or retrieved.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	–30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

DASH is a trademark of Data I/O Corporation.
OrCAD is a trademark of OrCAD, Inc.
IBM is a registered trademark of International Business Machines Corporation.

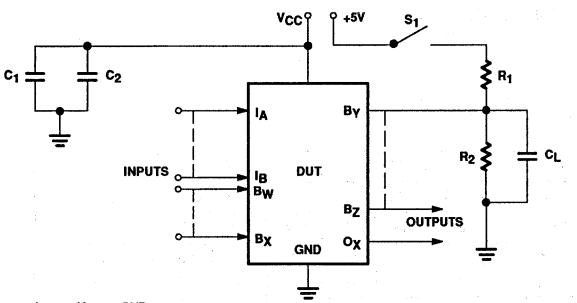
DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Input voltage							
V_{IL}	Low	V_{CC} = MIN		–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V_{CC} + 0.3	V
Output voltage							
V_{OL}	Low	V_{CC} = MIN, I_{OL} = 5mA				0.45	V
V_{OH}	High	V_{CC} = MIN, I_{OH} = –2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				–10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC}				10	µA
		V_{OUT} = GND				–10	µA
I_{OH}	Output High	V_{CC} = MIN, V_{OUT} = 2.4V				–2	mA
I_{OL}	Output Low	V_{CC} = MIN, V_{OUT} = 0.45V				5	mA
I_{OS}	Short-circuit[5]	V_{OUT} = GND				–100	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX, No load	CMOS input[2]		60	100[6]	mA
		f = 1MHz	TTL input[3]		65	120[6]	mA
I_{SB}	Standby V_{CC} supply current	V_{CC} = MAX, No load	CMOS input		1.0	10	mA
		PD = V_{IH}	TTL input		1.5	10	mA
Capacitance							
C_{IN}	Input	V_{CC} = 5V, T_{amb} = +25°C, V_{IN} = 2.0V			8		pF
C_B	I/O	V_{CC} = 5V, T_{amb} = +25°C, V_{IO} = 2.0V			16		pF

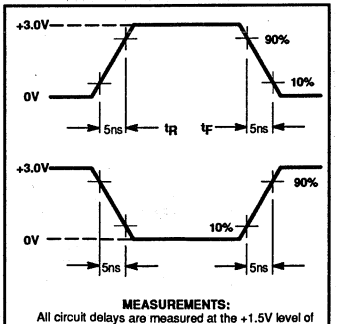
NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. CMOS inputs: V_{IL} = GND, V_{IH} = V_{CC}.
3. TTL inputs: V_{IL} = 0.45V, V_{IH} = 2.4V.
4. All voltage values are with respect to network ground terminal.
5. Duration of short-circuit should not exceed one second. Test one at a time.
6. ΔI_{CC} vs. Frequency = 4mA/MHz max.

TEST LOAD CIRCUITS



NOTES:
C_1 and C_2 are to bypass V_{CC} to GND.
Test Load R_1 = 750Ω, R_2 = 442Ω, C_L = 30pF (C_L = 5pF for Output Disable)
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

8

MACRO CELL AC SPECIFICATIONS

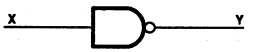
Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

Input Buffer
(DIN552, NIN552, BDIN55, BNIN552 CDIN552, CNIN552, CKDIN552, CKNIN552)

SYMBOL	PARAMETER		LIMITS						UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	X	I	5	7	10	7	10	15	ns
t_{PLH}	X	I	5	7	10	7	10	15	ns
t_{PHL}	Y	I	5	7	10	7	10	15	ns
t_{PLH}	Y	I	5	7	10	7	10	15	ns

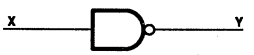
Input Pins: 8–14, 16, 17, 20, 22–24.
Bidirectional Pins: 1–3, 5–7, 46–48, 50–54, 57–64, 67, 68.

Internal NAND of Main Array
(FBNAND, NAND)



SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	10	15	20	12	18	25	ns
t_{PLH}	Y	X	10	15	20	12	18	25	ns

Internal NAND of Clock Array
(NAND)

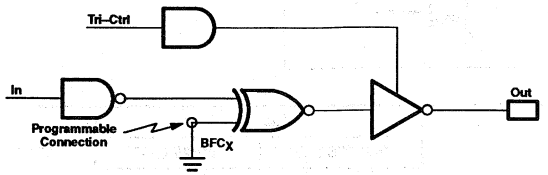


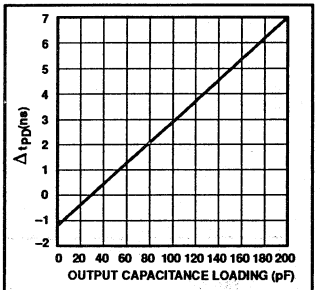
SYMBOL	PARAMETER		LIMITS			LIMITS			UNIT
	To	From	PML2552-35			PML2552-50			
	(Output)	(Input)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Y	X	5	7	10	7	10	15	ns
t_{PLH}	Y	X	5	7	10	7	10	15	ns

MACRO CELL AC SPECIFICATIONS (Continued)

Min: 0°C, 5.25V; Typ: 25°C, 5.0V; Max: 75°C, 4.75V (SNAP Resource Summary Designations in Parentheses)

3-State Output with Programmable Polarity (TOUT552 + EXOR552)



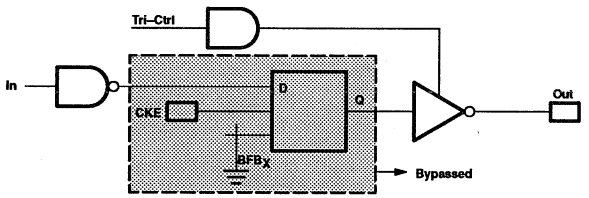


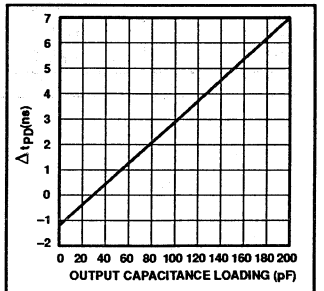
Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

Bidirectional Pins: 46–48, 50–54.

I/O Output Buffer with 3-State Control, DFF Bypassed (TOUT552 + NAND)





Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	To (Output)	From (Input)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Out	In	12	18	25	17	25	35	ns
t_{PLH}	Out	In	12	18	25	17	25	35	ns
t_{OE}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns
t_{OD}[4]	Out	Tri-Ctrl	5	7	10	7	10	15	ns

I/O Pins: 1–3, 5–7, 57–64, 67, 68.

Notes on page 8-157

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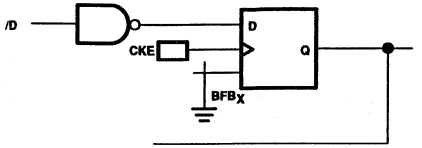
MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

D FLIP-FLOP

Output DFF Used Internally
(ODFF552)



SYMBOL	PARAMETER	LIMITS						UNIT
		PML2552-35			PML2552-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CKE}	Flip-flop toggle rate			50			35	MHz
$t_{W\,CKE}$ High	Clock HIGH	10			14			ns
$t_{W\,CKE}$ Low	Clock LOW	10			14			ns
t_{SETUP} /D	/D setup time to CKE	15			20			ns
t_{HOLD} /D	/D hold time to CKE	4			6			ns

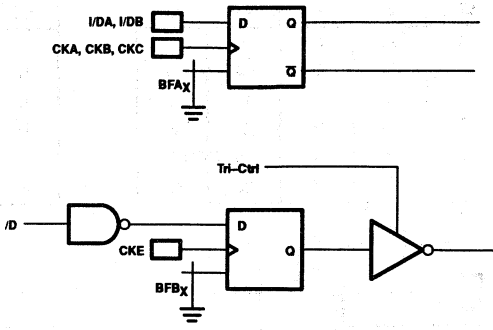
SYMBOL	PARAMETER		LIMITS						UNIT
	From	To	PML2552-35			PML2552-50			
	(Input)	(Output)	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKE ↑	Q	10	15	20	14	20	25	ns
t_{PHL}	CKE ↑	Q	10	15	20	14	20	25	ns

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)
D FLIP-FLOP (Continued)

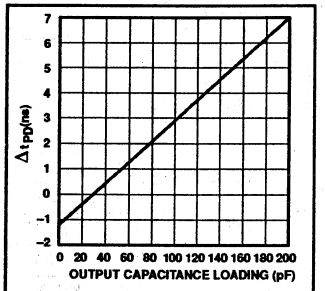
Input and Output
(IDFF552 & ODFF552)

INPUTS		OUTPUTS	
CK	D	Q	$\overline{Q}$
L	X	Q_0	$\overline{Q}_0$
↑	H	H	L
↑	L	L	H

NOTE:
Q_0, $\overline{Q}_0$ represent previous stable condition of Q, $\overline{Q}$.



SYMBOL	LIMITS						UNIT
	PML2552-35			PML2552-50			
	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{CKA, CKB, CKC}$			50			35	MHz
$t_{W\ CKA, CKB, CKC}$ High	10			14			ns
$t_{W\ CKA, CKB, CKC}$ Low	10			14			ns
t_{SETUP} I/DA, I/DB	5			7			ns
t_{HOLD} I/DA, I/DB	5			7			ns
f_{CKE}			50			35	MHz
$t_{W\ CKE}$ High	10			14			ns
$t_{W\ CKE}$ Low	10			14			ns
t_{SETUP} /D	15			20			ns
t_{HOLD} /D	4			6			ns



Δt_{PD} vs Output Capacitance Loading (Typical)

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PHL}	CKA, CKB/CKC ↑	Q, $\overline{Q}$	5	7	10	7	10	15	ns
t_{PLH}	CKE ↑	Out	12	18	25	17	25	35	ns
t_{PHL}	CKE ↑	Out	12	18	25	17	25	35	ns

MACRO CELL AC SPECIFICATIONS (Continued) (SNAP Resource Summary Designations in Parentheses)

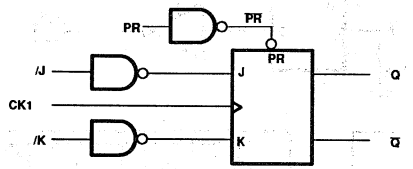
JK FLIP-FLOPS

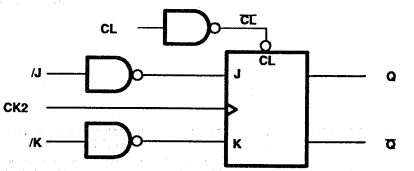
(JKPR552)

INPUTS				OUTPUTS	
$\overline{PR}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$

(JKCL552)

INPUTS				OUTPUTS	
$\overline{CL}$	CK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↑	L	L	Q_0	$\overline{Q}_0$
H	↑	H	L	H	L
H	↑	L	H	L	H
H	↑	H	H	TOGGLE	
H	L	X	X	Q_0	$\overline{Q}_0$





SYMBOL	PARAMETER	LIMITS						UNIT
		PML2552-35			PML2552-50			
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{CK1}	CK1 toggle frequency			50			35	MHz
f_{CK2}	CK2 toggle frequency			50			35	MHz
$t_{W\,CK1}$ High	CK1 clock HIGH	10			14			ns
$t_{W\,CK1}$ Low	CK1 clock LOW	10			14			ns
$t_{W\,CK2}$ High	CK2 clock HIGH	10			14			ns
$t_{W\,CK2}$ Low	CK2 clock LOW	10			14			ns
t_{SETUP} /J, /K	/J, /K setup time to CK1, CK2	27			35			ns
t_{HOLD} /J, /K	/J, /K hold time to CK1, CK2	0			0			ns
t_W PR Low	Preset Low period	10			14			ns
t_W CL Low	Clear Low period	10			14			ns

SYMBOL	PARAMETER		LIMITS						UNIT
	From (Input)	To (Output)	PML2552-35			PML2552-50			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PHL}	CK1,2	Q, $\overline{Q}$	2	3.5	5	3	5	7	ns
t_{PLH}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	PR	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PLH}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns
t_{PHL}	CL	Q, $\overline{Q}$	12	18	25	17	24	30	ns

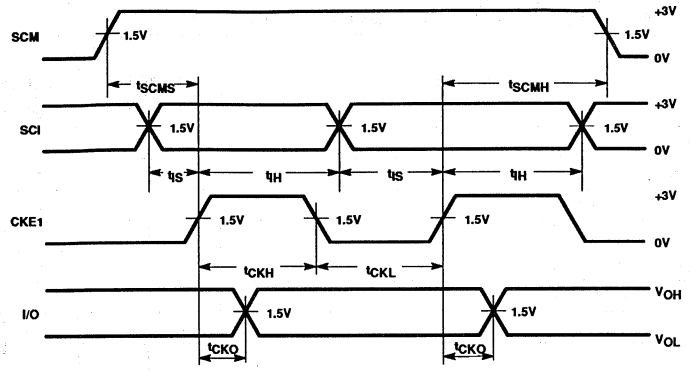
AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$, $V_{PP} = V_{CC}$,
$R_1 = 750\Omega$, $R_2 = 442\Omega$, $C_L = 5pF$ for Output Disable) (See Test Load Circuit Diagram)

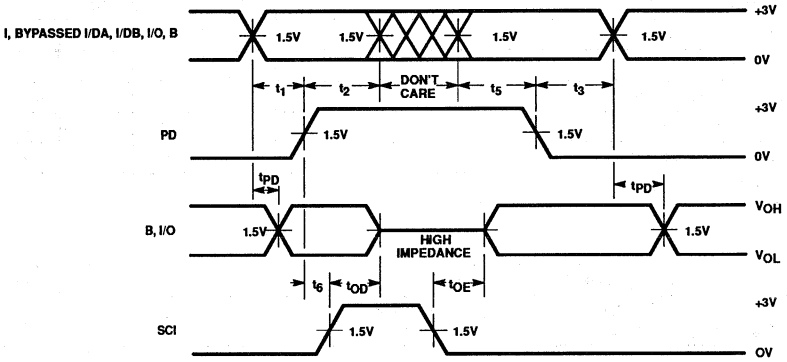
SYMBOL	PARAMETER	LIMITS				UNIT
		PML2552-35		PML2552-50		
		MIN	MAX	MIN	MAX	
Scan mode operation[1]						
t_{SCMS}	Scan Mode (SCM) Setup time	15		15		ns
t_{SCMH}	Scan Mode (SCM) Hold time	25		30		ns
t_{IS}	Data Input (SCI) Setup time	5		5		ns
t_{IH}	Data Input (SCI) Hold time	5		5		ns
t_{CKO}	Clock to Output (I/O) delay		30		40	ns
t_{CKH}	Clock High	10		15		ns
t_{CKL}	Clock Low	10		15		ns
Power down, power up[2]						
t_1	Input (I, bypassed I/DA, I/DB, I/O, B) setup time before power down	40		50		ns
t_2	Input hold time	30		35		ns
t_3	Power Up recovery time		60		70	ns
t_4	Output hold time	0		0		ns
t_5	Input setup time before Power Up	20		25		ns
t_{OE}	SCI to Output Enable time[3]		40		50	ns
t_{OD}	SCI to Output Disable time[3]		40		50	ns
t_6	Power Down setup time	10		15		ns
t_7	Power Up to Output valid		70		80	ns
Power-on reset						
t_{PPR1}	Power-on reset output register (Q = 0) to output (I/O) delay		10		15	ns
t_{PPR2}	Power-on reset input register (Q = 0), buried JK Flip-Flop (Q = 0) to output (B, bypassed I/O) delay		40		50	ns

NOTES:
1. SCM recovery time is 50ns after SCM operation. 50ns after SCM operation, normal operations can be resumed.
2. Timings are measured without foldbacks.
3. Transition is measured at steady state High level (–500mV) or steady state Low level (+500mV) on the output from 1.5V level on the input with specified test load ($R_1 = 750\Omega$, $R_2 = 442\Omega$, $C_L = 5pF$). This parameter is sampled and not 100% tested.
4. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

TIMING DIAGRAMS

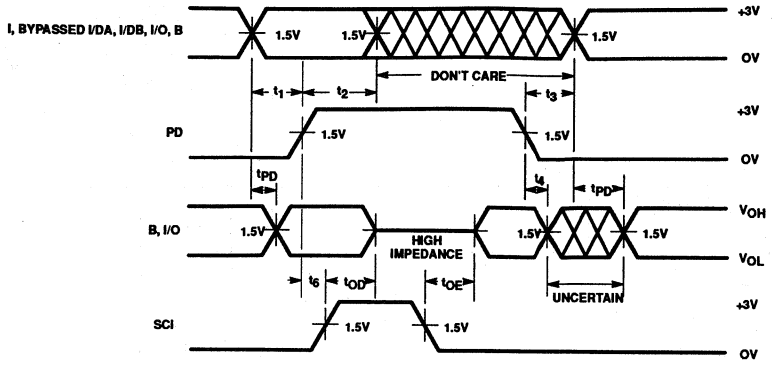


Scan Mode Operation

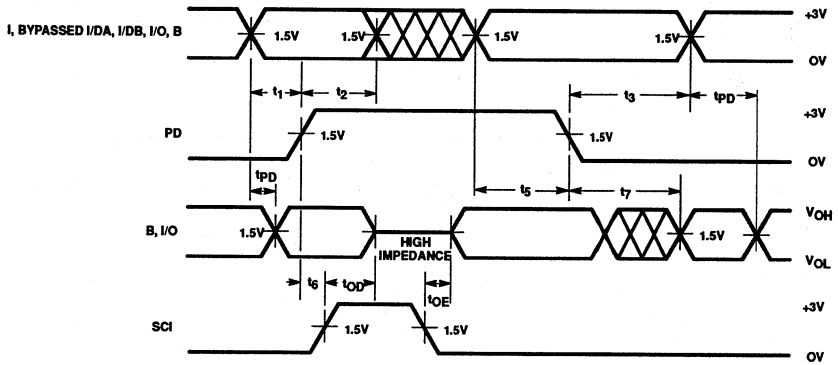


Power Down, Power Up
Input (old) Ready Before Power Up

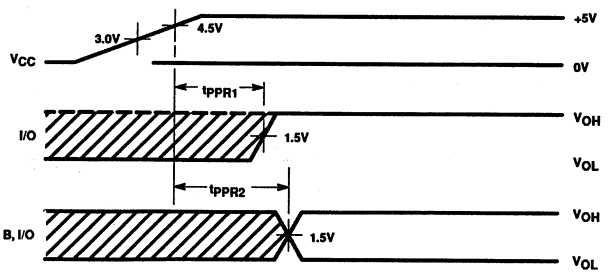
TIMING DIAGRAMS (Continued)



Power Down, Power Up
Input (new) Ready After Power Up

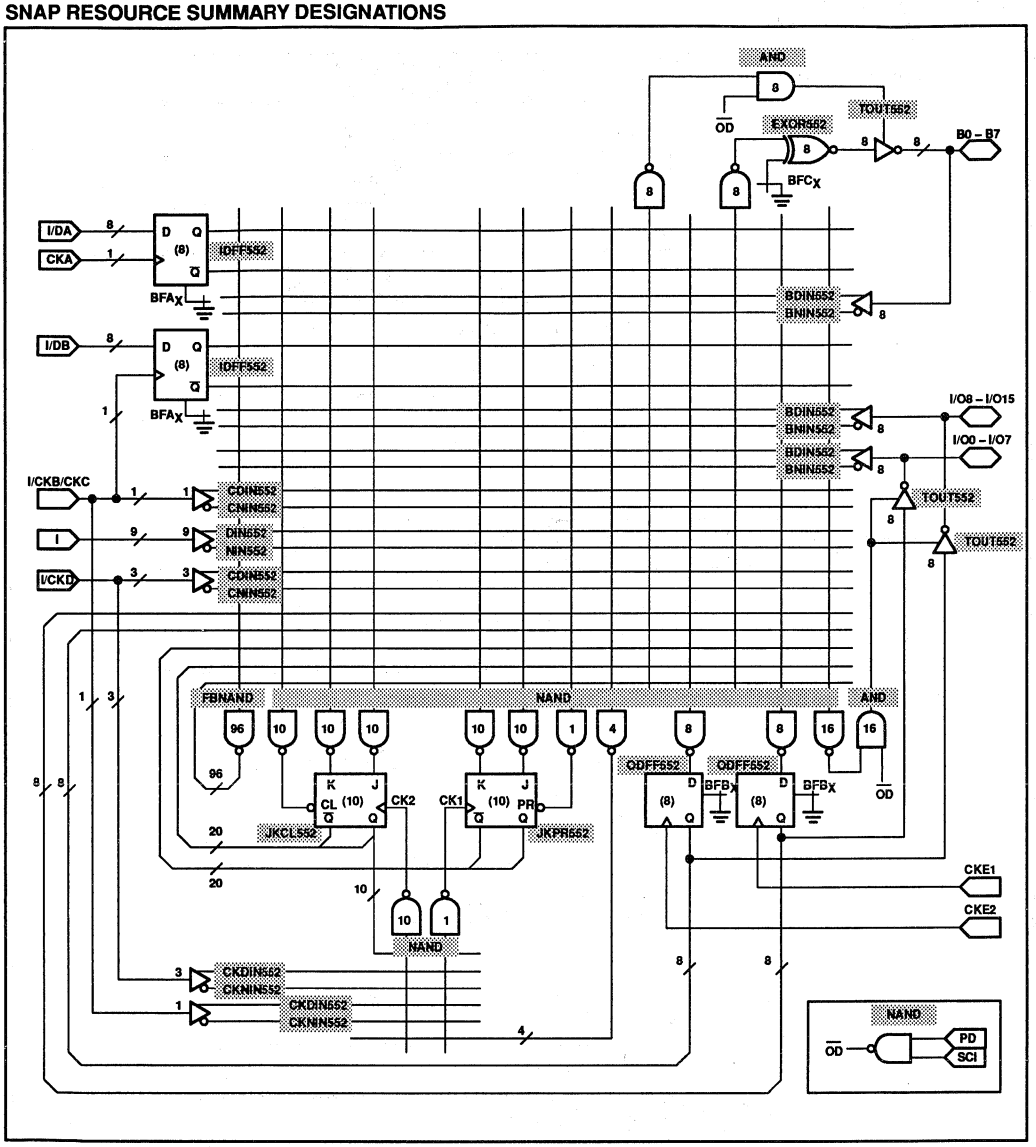


Power Down, Power Up
Input (new) Ready Before Power Up



Power-On Reset

SNAP RESOURCE SUMMARY DESIGNATIONS



ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PML2552 device is such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PML2552 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PML2552 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PML2552 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12,000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING

Refer to the following charts for qualified manufacturers of programmers and software tools:

PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073–9746 (800)247–5700	UNISITE 40/48 V2.8 Pinsite – V2.0	15908C* (with adaptor) 15908D (with pinsite)
STREBOR DATA COMMUNICATIONS 1008 N. NOB HILL AMERICAN FORK, UT 84003	PLP–S1A Programmer MP68CC Adaptor	

* Needs a 40-pin DIP to 68-pin PLCC adaptor that is available from Emulation Technology.
Part Number: AS–68–40–04P–6

EMULATION TECHNOLOGY, INC.
2368B Walsh Avenue, Blvd. D
Santa Clara, California 95051
Telephone No. (408) 982–0660
Fax. No. (408) 982–0664

SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
SIGNETICS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088–3409 (408)991–2000	SNAP SOFTWARE REV. 1.4 AND LATER

8

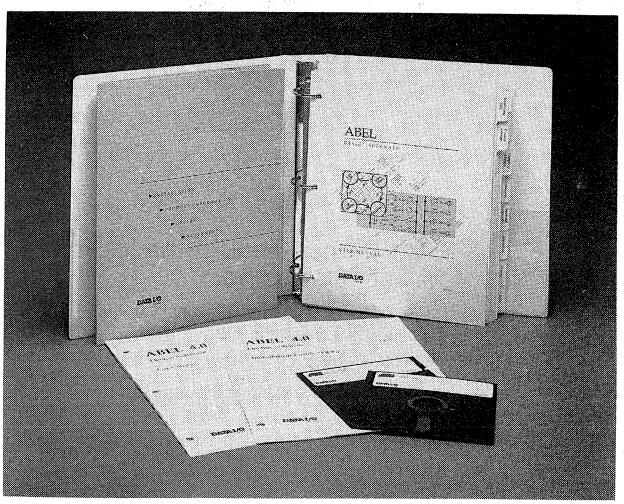
Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
35	15	25	ATS2552-35JC ATS2552-35KC	68J 68KW	Commercial (0°C to 70°C)
50	20	35	ATS2552-50JC ATS2552-50KC	68J 68KW	Commercial (0°C to 70°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Features

- Atmel-ABEL-4 Uses the Industry-Standard ABEL Hardware Description Language
- Multiple Input Methods :
  - Boolean Equations, Truth Tables and State Diagrams
  - Optional Schematic Entry Available
- Automatic Logic Reduction, Simulation, Error Checking, and Generation of Design Documentation
- Automatically Takes Advantage of Atmel's EPLD Architecture, Joining Sum Terms When Extra Product Terms are Needed
- Runs on MS-DOS™ Compatible Personal Computers
- This Inexpensive Package Includes:
  - Atmel-ABEL-4 Software which Supports ATV750, ATV2500 and ATV5000
  - Complete ABEL Manual
  - Logic Diagrams for ATV750, ATV2500, and ATV5000
  - Design Examples
  - Special Offers and Coupons



High-Level Design Tool for Atmel Programmable Logic Devices: ATV750 ATV2500 ATV5000

8

Description

Atmel Programmable Logic Devices (PLDs) offer powerful solutions for logic design. Atmel-ABEL-4, developed by Data I/O Corporation, is a software package specifically designed to support development with Atmel Programmable Logic Devices.

Atmel-ABEL-4 offers all of the function and features of Data I/O's standard ABEL-4 software package while supporting Atmel's three high-density PLDs: the ATV750, ATV2500 and ATV5000. Support for other manufacturer's PLDs is not provided.

Atmel-ABEL-4 automatically takes advantage of Atmel's innovative multiple sum term PLD architecture. When your reduced equations require more product terms than anticipated, the software automatically allocates the next available block of product terms to your equation.

Atmel-ABEL-4 automatically reduces your logic equations to near minimal form. Depending on your requirements, you can choose among several reduction algorithms. The result is a more efficient, cost-effective design.

Behavioral simulation is an integral part of the Atmel-ABEL-4 design package. Simulation may be performed on either the design equations as entered, or after device selection, pin and

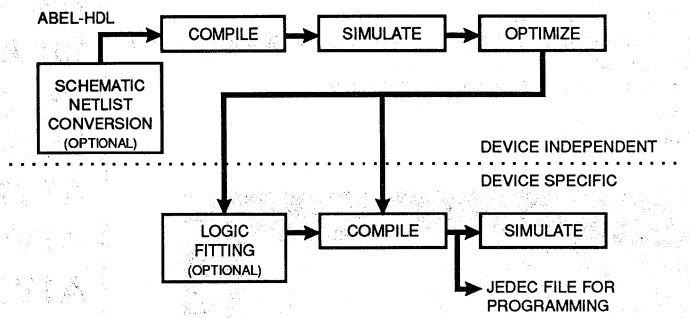
Desciption (Continued)

node assignment, and option selection. This way you can verify that the completed design matches your design input.

Atmel-ABEL-4 uses the Open ABEL format which allows the use of optional logic fitters. These logic fitters perform automatic device pin and node assignment and macrocell option selection to make maximum use of device resources, speeding up the design process.

Once your design is ready, Atmel-ABEL-4 generates standard JEDEC files which can be downloaded to your programmer with the terminal emulation software included with the package.

Design Flow Diagram



Requirements for ATV750 and ATV2500 Support

- MS-DOS Compatible Personal Computer (version 3.0 or higher)
- 5 1/4" High Density Floppy Disk Drive (low density disks available on request)
- 640K RAM

Additional Requirements for ATV5000 Support

- MS-DOS Compatible Personal Computer (version 3.0 or higher)
- 386 or 386SX CPU
- 2 MB RAM (Extended Memory)

Ordering Information

Ordering Code	Description
ATMEL-ABEL-4	High-Level Design Tool for Atmel Programmable Logic Devices ATV750, ATV2500, ATV5000

ABEL™ is a trademark of Data I/O Corporation.
MS-DOS™ is a trademark of Microsoft Corporation.

ABEL-4 Custom Logic Fitter for ATV750 and ATV2500

Features

- **Works with ABEL-4 PLD Design System**
- **Allows Device-Independent Design**
- **Optimizes Resource Utilization**
- **Assigns Signals to Pins and Nodes**
- **Utilizes Atmel's Unique Product Term Joining/Sharing**

Description

Atmel-FIT2500 is a custom logic fitter for Data I/O's ABEL-4 PLD design system which supports both the ATV750 and the ATV2500 PLDs. FIT2500 was written by Data I/O with Atmel's cooperation and approval. This fitter will also work with Atmel-ABEL-4, the special version of ABEL-4 available from Atmel which supports only the ATV750, ATV2500, and ATV5000.

The fitter performs pin/node signal assignment,performs macrocell option selection, takes advantage of Atmel's shared product term architecture where possible, and maximizes resource utilization. This allows a user to do device-independent design and still get maximum utilization for Atmel's ATV750 and ATV2500 PLDs without needing to know all internal details of the devices.

Pin/node assignments may be made by the user, assigned by the fitter, or a combination of both. Optionally, all pin/node assignments can be ignored and the fitter will attempt to fit the design into the target device automatically.

Requirements

- Atmel-FIT2500 requires ABEL-4 or Atmel-ABEL-4 running under MS-DOS, version 3.00 or higher.

Ordering Information

Ordering Code	Description
ATMEL-FIT2500	ABEL-4 Custom Logic Fitter for ATV750 and ATV2500

Programming Software Companies

ACCEL Technologies, Inc.
6825 Flanders Drive
San Diego, CA 92121
(800) 433-7801

Data I/O Corporation (ABEL™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

ISDATA Gmbh (LOG/iC)
Haid-und-Neu- Str. 7
D-7500 Karlsruhe 1
West Germany
0721 / 69309

800 Airport Rd.
Monterey, CA 93940
(408) 373-3607
(800) 777-1202

Logical Devices (CUPL™)
1201 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

PistoHI Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422
(800) 2PISTOHL

Programming Hardware Companies

Advin Systems, Inc.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 243-7000

BP Microsystems
10681 Haddington #190
Houston, TX 77043
(713) 461-9430

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Logical Devices
1201 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

Owen
Ringstr. 11
Postfach 1104
D-6798 Kusel
Germany
(49) 6381-5085

PistoHI Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422

SMS SPRINT International
Im Morgental 13
D-8994 Hergatz
Germany
(49) 7522-5018

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

System General
244 S. Hillview Drive
Milipitas, CA 95035
(408) 263-6667

CMOS EPLD Programming Hardware and Software Support

8

ATMEL

Section 9

CMOS Gate Arrays

Features

- **0.8 µ effective gate lengths (1.0 µ drawn) combined with close metal spacing provides outstanding speed/power performance**
- **There is no new software to learn with Atmel's flexible design system**
- **Design translation of existing ASIC designs provides for easy alternate sourcing with equivalent performance**
- **All ATL arrays can operate at 5.0 volts and 3.3 volts for low-power applications**
- **Product testability is improved using Design-For-Test (DFT) techniques such as serial and boundary scan JTAG and built-in self test**
- **At-speed testing is available up to 50 MHz**
- **Full custom package design capability (including TAB) allows Atmel to precisely fit your application**
- **All ATL arrays can be supplied to military-level (MIL-STD-883C) screening**
- **Memory-driven manufacturing provides cost efficiency for ASIC volumes**

Description

The high-performance ATL Series CMOS gate arrays offer superior system performance, flexibility, testability and board utilization. The ATL gate arrays employ 0.8 µ-effective (1.0 µ-drawn), double-level metal, Si-gate, CMOS technology processed in a U.S.-based, advanced manufacturing facility.

The arrays utilize an enhanced channelless architecture which results in greater than 50 percent usable gates. This efficient routing scheme combined with close spacing for both metal layers allows Atmel to provide more gates per I/O.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The customer can start designing with the ATL series today using existing CAD/CAE tools.

ATL Array Organization

Device	ATL4	ATL10	ATL20	ATL20C	ATL40	ATL60	ATL130	ATL160
Total	4K	10K	22K	22K	40K	57K	131K	157K
Usable	2.6K	6.5K	12K	12K	22K	30K	67K	80K
Total	68	124	144	160	180	224	256	360
I/O	60	116	136	148	168	208	236	320

ATL Series Gate Arrays

9

ATL Design Flow

Library

Atmel provides the cell library consisting of schematic symbols, functional models, and timing models, on the customer's workstation. Design platforms supported include Mentor™, Valid™, Viewlogic™ Cadence™, Racal-Redac and DAZIX™. Schematic capture, simulation and test vector generation are performed by the customer and verified by Atmel.

Simulators

Atmel supports a variety of simulators including QuickSim™, ViewSim™, Verilog-XL™ Synopsys™, CADAT,™ AdvanSIM™ and RapidSIM™.

Design Translation

Atmel has translated designs from most major ASIC suppliers into a gate level netlist using Atmel's ATL series library. The design can be optimized for speed or power consumption, modified to add logic or memory functions, or replicated for a pin-for-pin, drop-in replacement.

Design Synthesis

Atmel can accept Register Transfer Level (RTL) designs for VHDL (MIL-STD-454L, IEEE STD 1076) or Verilog-XL™ HDL format. Atmel will synthesize the design, translate to gate level and optimize for speed and/or size.

Preliminary Design Review (PDR)

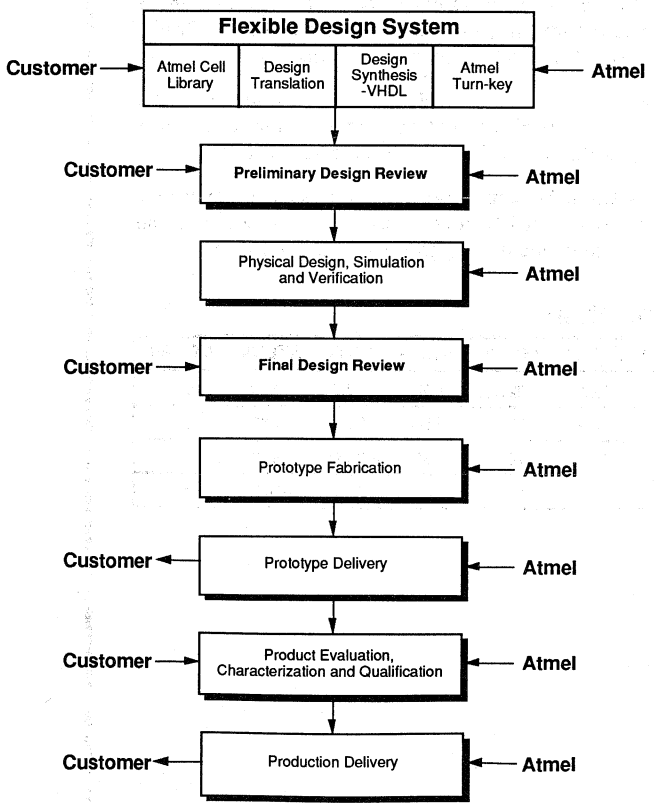
At PDR Atmel will formally accept the customer's design inputs. Prior to the meeting Atmel will perform timing and functional simulation on Verilog-XL™ using customer provided test vectors.

Final Design Review

After physical design, verification and post-route simulation the customer and Atmel will hold a final design review prior to prototype fabrication. Atmel guarantees device performance equal to or better than that predicted from post-route simulation on Verilog-XL™.

ATL Gate Array Design Flow

Development to Production



ATL Series Cell Library

Atmel's ATL series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 114 hard-wired data path elements and has been characterized via extensive SPICE modeling at the transistor level and verified through measurements made on fabricated test arrays. Characterization has been performed over the military temperature and voltage ranges, to ensure that the simulation accurately predicts the performance of the finished product. Atmel is continually expanding the ATL series cell library with both soft and hard macros. Check with your sales representative for the most recent additions.

Cell Guide

Buffers and Inverters	
1 x Buffer	1 x Inverter
2 x Buffer	Dual 1 x Inverter
Tristate Bus Driver with High Enable	Quad 1 x Inverter
Tristate Bus Driver with Low Enable	Quad Tristate Inverter
3 x Buffer	2 x Inverter
4 x Buffer	Dual 2 x Inverter
8 x Buffer	Tristate Inverter with High Enable
12 x Buffer	3 x Inverter
16 x Buffer	4 x Inverter
	8 x Inverter
	10 x Inverter

AND, NAND, OR, NOR Gates	
2-input AND	2-input NOR
2-input AND with High Drive	Dual 2-input NOR
3-input AND	2-input NOR with High Drive
3-input AND with High Drive	3-input NOR
4-input AND	3-input NOR with High Drive
4-input AND with High Drive	4-input NOR
2-input NAND	4-input NOR with High Drive
Dual 2-input NAND	5-input NOR
2-input NAND with High Drive	8-input NOR
3-input NAND	16-input NOR with High Drive
3-input NAND with High Drive	2-input OR
4-input NAND	2-input OR with High Drive
4-input NAND with High Drive	3-input OR
5-input NAND	3-input OR wiht High Drive
5-input NAND with High Drive	4-input OR
6-input NAND	4-input OR with High Drive
6-input NAND with High Drive	
7-input NAND	
7-input NAND with High Drive	
8-input NAND	
8-input NAND with High Drive	

Cell Guide

Multiplexers	
2-input MUX	4-input MUX
2-input MUX with High Drive	4-input MUX with T-gate Data Inputs
2-input MUX with Inverted Output	4-input MUX with T-gate Data Inputs and High Drive
2-input MUX with Inverted Output and High Drive	5-input MUX with High Drive
2-input MUX with Low Enable	8-input MUX
Quad 2-input MUX with Low Enable	8-input MUX with Low Enable
Quad 2-input MUX	8-input MUX with T-gate Data Inputs and High Drive
3-input MUX with Inverted Output	
3-input MUX with Inverted Output and High Drive	

AND/OR, OR/AND Gates	
2-input AND into 2-input NOR	2-input OR into 2-input NAND
2-input AND into 2-input NOR with High Drive	2-input OR into 2-input NAND with High Drive
Symmetric 2-input AND into 2-input NOR	Symmetric 2-input OR into 2-input NAND
Symmetric 2-input AND into 2-input NOR with High Drive	Symmetric 2-input OR into 2-input NAND with High Drive
3 2-input ANDs into 3-input NOR	4 2-input ORs into 4-input NAND
3 2-input ANDs into 3-input NOR with High Drive	2-input OR into 3-input NAND

Exclusive OR/NOR Gates	
1-bit Adder	2-input Exclusive OR with High Drive
1-bit Adder with T Gates	2-input Exclusive NOR
7-input Carry Lookahead	2-input Exclusive NOR with High Drive
2-input Exclusive OR	

Decoders	
2:4 Decoder	3:8 Decoder with Low Enable
2:4 Decoder with Low Enable	

Cell Guide

Flip-flops/Latches	
D Flip-flop	Latch
D Flip-flop with asynchronous CLEAR/PRESET	Latch with Complementary Outputs
D Flip-flop with asynchronous CLEAR	Latch with Complementary Outputs and Inverted Hold
D Flip-flop with High Drive	Quad Latch with Complementary Outputs and Inverted Hold
D Flip-flop with asynchronous RESET	Latch with Complementary Outputs and High Drive
D Flip-flop with asynchronous SET	Quad Inverting Latch
D Flip-flop with asynchronous SET/RESET	Latch with RESET
JK Flip-flop	Latch with SET/RESET
JK Flip-flop with asynchronous CLEAR	

Scan Cells	
Set-scan D Flip-flop	Quad Set-scan D Flip-flop with CONTROLS
Quad Set-scan D Flip-flop with ENABLE	

I/O Options
Input, Output, Bidirectional, Tristate Output and Internal Clock Driver
P&N Drive Value Programmable from 2 mA to 48 mA in 2 mA increments with Slew Rate Control
CMOS or TTL Operation
Schmitt Trigger (Bidirectional, Input)
Testable NAND Gate on Input (Bidirectional, Input)
Inverting Input Buffer (Bidirectional, Input)
Pullup Register - 10K Ω to 320K Ω
Pulldown Register - 7K Ω to 280K Ω

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	$V_{dd}/2$ Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{dd} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{dd} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{dd}$, V_{dd} = 5.5 V		.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{dd} = 5.5 V	-10	.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{dd} = 5.5 V	-325	-160	-40	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{dd}$ or V_{SS}, V_{dd} = 5.5 V	-10	.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{dd} = 5.5 V, $V_{OUT} = V_{dd}$	10	50	100	mA
		V_{dd} = 5.5 V, $V_{OUT} = V_{SS}$	-100	-50	-10	mA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{dd}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{dd}			V
V_T	TTL Switching Threshold	V_{dd} = 5.0 V, 25°C		1.4		V
	CMOS Switching Threshold	V_{dd} = 5.0 V, 25°C		2.4		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage.	I_{OL} = as rated V_{dd} = 4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2 mA I_{OH} per stage.	I_{OH} = as rated V_{dd} = 4.5 V	0.7 x V_{dd}	4.4		V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

3.3 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{dd} = 3.0 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{dd}$, V_{dd} = 3.6 V		.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{dd} = 3.6 V	-10	.01		µA
	40K pull-up	$V_{IN} = V_{SS}$, V_{dd} = 3.6 V	-200	-60	-10	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{dd}$ or V_{SS}, V_{dd} = 3.6 V	-10	.01	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{dd} = 3.6 V, $V_{OUT} = V_{dd}$	5	25	60	mA
		V_{dd} = 3.6 V, $V_{OUT} = V_{SS}$	-5	-25	-60	mA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{dd}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{dd}			V
V_T	CMOS Switching Threshold	V_{dd} = 3.3 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{dd} = 3.0 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1 mA I_{OH} per stage.	I_{OH} = as rated V_{dd} = 3.0 V	0.7 x V_{dd}			V

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance Input Buffer (Die)	5.0 V, 3.3 V		2.4		pF
C_{OUT}	Capacitance Output Buffer (Die)	5.0 V, 3.3 V		5.6		pF
$C_{I/O}$	Capacitance Bi-Directional	5.0 V, 3.3 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.2	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.6	0.8		V
	CMOS Negative Threshold	25°C, 5.0 V	1.0	1.2		V
ΔV	TTL Hystersis	25°C, 5.0 V	0.4	1.0		
	CMOS Hystersis	25°C, 5.0 V	1.0	2.0		
V+	CMOS Positive Threshold	25°C, 3.3 V		2.2	2.3	V
V-	CMOS Negative Threshold	25°C, 3.3 V	.65	0.9		V
ΔV	CMOS Hystersis	25°C, 3.3 V	1.0	1.3		

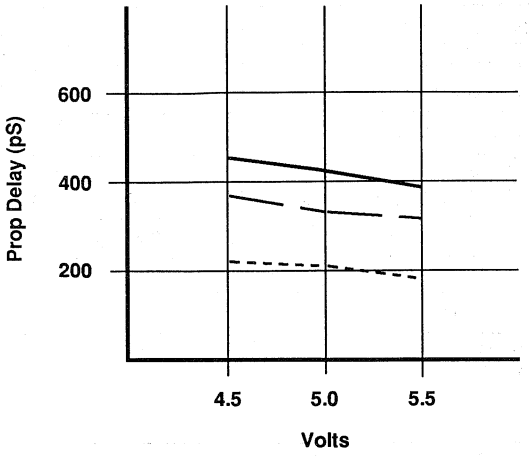
I/O Buffers

- Programmable output drive
  (2 to 24 mA I_{OL}, -2 to -24 mA I_{OH} for 5.0 V
  1 to 12 mA I_{OL}, -1 to -12 mA I_{OH} for 3.3 V)
- ESD input protection up to 3000 volts
- Built-in configurable test logic

The ATL series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 24 mA, and responds to CMOS or TTL logic levels. All outputs can be switched to a high impedance state. I/O locations on this ring can accomodate bidirectional cells.

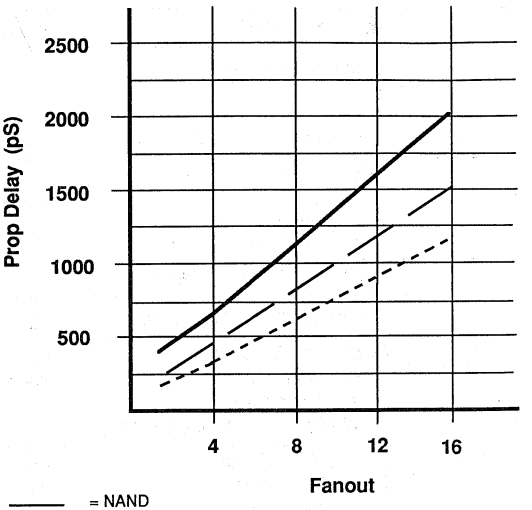
AC Characteristics

Delay vs V_{CC}



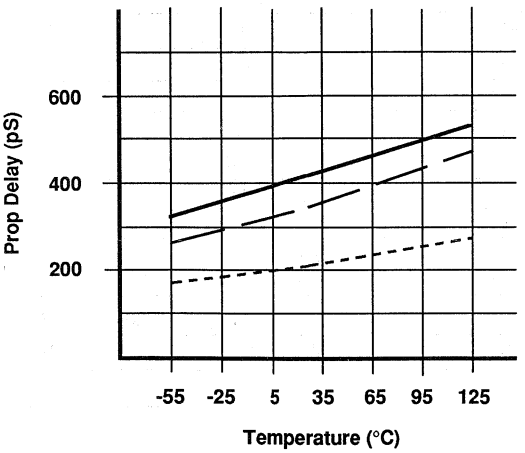
= NAND
= NOR
= INV
FO = 1
T = 25°C

Delay vs Fanout



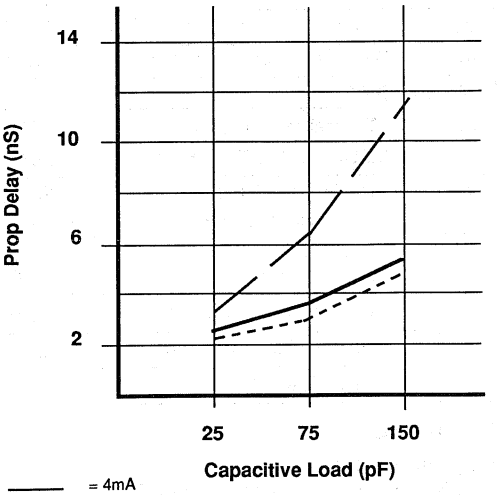
= NAND
= NOR
= INV
T = 25°C
Vcc = +5V

Delay vs Temperature



= NAND
= NOR
= INV
FO = 1
Vcc = +5V

Output Buffer vs Load



= 4mA
= 12mA
= 16mA
T = 25°C
Vcc = +5V

Design for Testability

Atmel's arrays support a full range of Design-for-Test (DFT) testability improvement techniques which reduce design debug time, component test time, and board and system test times. These techniques also improve system diagnostics.

Serial scan techniques, using specially designed registers, improve controllability and observability by allowing the establishment of scan paths deep inside the circuit logic. Serial patterns can be loaded into these registers and signature analysis techniques used to provide an easy means of determining circuit functionality. This testability improvement method is supported on each of the ATL arrays.

Shadow registers, included in the I/O buffer cells for the arrays, facilitate the use of boundary scan techniques. This testability improvement method, coupled with serial scan techniques, provides excellent fault isolation within the array and simplifies the testing of interconnects on the board. Scan registers in the periphery can be configured to generate pseudo-random test patterns and signature analysis registers, thus acting as on-chip test pattern generators.

The ATL arrays also support the Joint Test Action Group (JTAG) boundary scan architecture. This permits testability access to the IEEE 1149.1 standard through only four package pins.

Advanced Packaging

Atmel offers its ATL series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon. Atmel supports a wide variety of standard packages for the ATL series.

All of Atmel's standard packages have been characterized for thermal and electrical performance. When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations, including multichip modules and Tape Automated Bonding (TAB) packages. Atmel's domestic packaging facility manufactures commercial, industrial, Class B and modified Class S level product.

Packaging Options

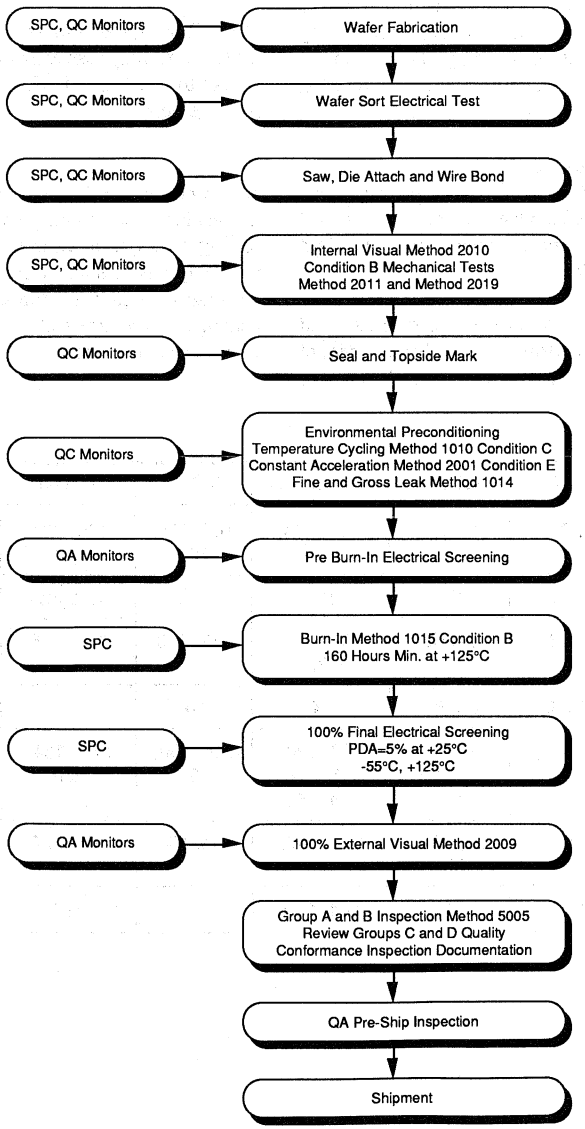
	ATL4	ATL10	ATL20/20C	ATL40	ATL60	ATL130	ATL160
CPGA	64, 68	84, 100	124, 144	144, 155, 180	180, 223, 224	256	299
CLDCC	64, 68	84	132	132	132, 224	224	340, 224
CLCC	44, 52	84, 52	52, 84, 132	132, 148	148, 196		
PLCC	28, 44, 68	68, 84	84	84			
PQFP	44, 68	68, 80, 100, 120	100, 120, 128, 136, 144, 160	144, 160, 184	160, 184, 208	232 208	232
PPGA	68	84, 100, 120	120, 132, 144	144, 180	180, 224	224	224
TAB	68	128	144, 160	180	224	256	360

Military and Aerospace

Atmel's ATL series gate arrays and standard packages are designed for use in military (MIL-STD-883) and commercial aerospace applications. The company is pursuing QPL listing for the ATL series gate arrays and anticipates this activity will be completed in 3Q91. Atmel's domestic wafer fab, assembly and test facilities are configured to support MIL-M38510. Atmel is committed to supporting military products, including SF1411 cost and pricing proposals. In the past decade the company has delivered over 3 million units for DoD programs.

Military Product Flow Chart

ATL Series Gate Array MIL-STD-883 Class B



ATL Series Gate Array 1.0µ CMOS Cell Library

Introduction

The ATL series gate arrays use a library of highly accurate cells implemented on an advanced 1.0µ (drawn) CMOS process. The cell library contains over 110 hard-wired cells which have been characterized through SPICE modeling at the transistor level. The cells have also been verified through measurements made on test arrays over commercial and military temperature and voltage ranges. The 1.0µ CMOS process is under strict statistical process control to ensure that the simulations will accurately predict the performance of the fabricated gate arrays.

The cell library contains both standard and high drive cells. Also included are scan cells, and all the cells required to implement IEEE 1149.1 (JTAG) boundary scan architecture as well as other testability schemes. New cells are being added to the library on a regular basis. Check with your Atmel sales representative for the latest list.

AT22000 CMOS Wafer Process

Feature	AT22000
Drawn Gate Length	1.0 µ
Effective Gate Length	0.8 µ
Metal Levels	2
First Metal Pitch	3.0 µ
Second Metal Pitch	3.4 µ
Silicide Process	Yes
Supply Voltage	+5.0 V, +3.3 V

Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0V; Input Rise and Fall Times = 1ns; Process = Nominal)

Macrocells in alpha-numeric order

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
ADD3	1-Bit Adder	P	1.273	0.106	1.275	0.087
		Q	0.574	0.097	0.651	0.068
		CI	0.564	0.090	0.691	0.065
AND2	2-Input AND	A, B	0.494	0.057	0.522	0.045
AND3	3-Input AND	A - C	0.689	0.058	0.572	0.046
AND4	4-Input AND	A - D	0.806	0.063	0.642	0.043
AOI22	2-Input AND into 2-Input NOR	A - C	0.402	0.103	0.324	0.056
AOI222	Symmetric 2-Input AND into 2-Input NOR	A - D	0.608	0.105	0.517	0.065
AOI222H	Symmetric 2-Input AND into 2-Input NOR (high drive)	A - D	0.406	0.036	0.428	0.032
BUF1	1 x Buffer	I	0.372	0.054	0.450	0.040
BUF2	2 x Buffer	I	0.461	0.026	0.512	0.021
BUF2T	Tristate Bus Driver w/High Enable	I	0.436	0.047	0.537	0.036
		E	0.144	0.063	0.160	0.037
BUF2Z	Tristate Bus Driver w/Low Enable	I	0.431	0.046	0.550	0.036
		E	0.167	0.061	0.282	0.032
BUF3	3 x Buffer	I	0.495	0.020	0.547	0.019
BUF4	4 x Buffer	I	0.549	0.016	0.624	0.014
BUF8	8 x Buffer	I	0.557	0.007	0.636	0.006
BUF12	12 x Buffer	I	0.565	0.005	0.643	0.004
BUF16	16 x Buffer	I	0.545	0.004	0.618	0.003
CLA7X	7-Input Carry Lookahead	A - G	0.919	0.165	0.604	0.088
DEC4	2:4 Decoder	S0, S1	0.523	0.056	0.589	0.063
DEC4N	2:4 Decoder w/Low Enable	S0, S1	1.043	0.055	0.790	0.064
		E	0.710	0.055	0.935	0.064

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
DEC8N	3:8 Decoder	S0, S1, S2	1.380	0.055	1.392	0.085
	w/ Low Enable	E	0.795	0.058	1.242	0.087
DFF	D Flip-flop	CLK	1.009	0.058	0.934	0.048
DFFBCPX	D Flip-flop	CLK	1.203	0.143	1.178	0.121
	w/ asynchronous	C	1.156	0.175	0.553	0.051
	Clear and Preset	P	1.151	0.175	0.687	0.043
DFFBSRX	D Flip-flop	CLK	1.189	0.119	1.216	0.113
	w/ Set and Reset	S	0.480	0.056	1.008	0.152
		R	0.623	0.057	1.092	0.154
DFFC	D Flip-flop	CLK	1.069	0.063	0.916	0.049
	w/ asynchronous CLEAR	C	—.—	—.—	0.896	0.048
DFFR	D Flip-flop	CLK	1.079	0.061	0.924	0.049
	w/ asynchronous RESET	R	—.—	—.—	1.215	0.050
DFFS	D Flip-flop	CLK	1.006	0.058	0.968	0.057
	w/ asynchronous SET	S	0.754	0.058	—.—	—.—
DFFSR	D Flip-flop	CLK	1.113	0.104	1.009	0.055
	w/ asynchronous	S	0.500	0.150	—.—	—.—
	SET/RESET	R	—.—	—.—	0.346	0.043
DSSB	Set Scan D Flip-flop	CLK	1.249	0.058	1.250	0.048
DSSBQ	Quad Set Scan D Flip-flop w/ Enable	CLK	1.501	0.058	1.503	0.048
DSSBXQ	Quad Set Scan D Flip-flop w/ Controls	CLK	1.650	0.069	1.650	0.055
INV1	1 x Inverter	I	0.250	0.055	0.193	0.045
INV1D	DUAL 1 x Inverter	I0, I1	0.250	0.055	0.193	0.045
INV1Q	Quad 1 x Inverter	I0 - I3	0.250	0.055	0.193	0.045
INV1TQ	Quad Tri-state	I0 - I3	0.199	0.107	0.225	0.064
	Inverter	E0, E1	0.450	0.107	0.558	0.064
INV2	2 x Inverter	I	0.238	0.030	0.168	0.026
INV2D	DUAL 2 x Inverter	I0, I1	0.238	0.030	0.168	0.026
INV3	3 x Inverter	I	0.227	0.022	0.154	0.020
INV4	4 x Inverter	I	0.214	0.017	0.153	0.016

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
INV10	10 x Inverter	I	0.895	0.005	0.858	0.004
JKF	JK Flip-flop	CLK	1.067	0.057	0.981	0.047
JKFC	JK Flip-flop	CLK	1.125	0.063	0.947	0.048
	w/Asynchronous Clear	CLR	–·–	–·–	0.970	0.047
LAT	LATCH	D	0.712	0.058	0.844	0.048
		H	0.905	0.058	0.777	0.048
LATBG	LATCH	D	0.948	0.057	0.954	0.047
	w/ Complementary	G	1.192	0.059	1.198	0.048
	Outputs and Inverted Hold					
LATIQ	Quad Inverting	D0 - D3	0.414	0.054	0.347	0.046
	LATCH	H	1.009	0.055	1.233	0.043
LATR	LATCH w/ Reset	D	0.843	0.102	0.875	0.047
		H	1.012	0.102	0.794	0.047
		R	–·–	–·–	0.352	0.043
LATS	LATCH w/ Set	D	0.058	0.751	1.169	0.053
		H	0.911	0.058	0.961	0.055
		S	0.839	0.058	–·–	–·–
LATSR	LATCH	D	0.751	0.058	1.169	0.053
	w/ Set and Reset	H	1.019	0.102	0.971	0.056
		S	1.000	0.500	—·—	—·—
		R	—·—	—·—	0.352	0.042
MUX2	2-Input MUX	I0, I1	0.664	0.058	0.786	0.049
		S	0.611	0.058	0.613	0.048
MUX2I	2-Input MUX	I0, I1	0.200	0.204	0.293	0.047
	w/ Inverterd Output	S	0.585	0.053	0.538	0.041
MUX2N	2-Input MUX	I0, I1	0.736	0.103	0.803	0.050
	w/ Low Enable	S	0.688	0.103	0.636	0.048
		E	0.355	0.099	0.298	0.044
MUX2NQ	Quad 2-Input MUX	S	1.194	0.106	1.139	0.049
	w/ Low Enable	E	0.813	0.105	0.767	0.047
		I	0.780	0.104	0.895	0.048
MUX2Q	Quad 2-Input MUX	I	0.6615	0.058	0.799	0.049
		S	1.059	0.056	1.065	0.050
MUX4	4-Input MUX	I0 - I3	1.091	0.065	1.324	0.059
		S0, S1	1.107	0.067	1.100	0.061

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
MUX4X	4-Input MUX w/ T-gate Data Inputs	I0 - I3 S0, S1	0.777 0.788	0.059 0.057	0.813 0.896	0.049 0.041
MUX8	8-Input MUX	I0 - I7 S0 - S2	1.588 1.717	0.072 0.072	1.862 1.726	0.070 0.070
MUX8N	8-Input MUX w/ Low Enable	I0 - I7 E S0 - S2	1.753 0.349 1.637	0.110 0.102 0.108	1.833 0.290 1.700	0.075 0.044 0.069
NAN2	2-Input NAND	A, B	0.343	0.055	0.305	0.061
NAN2D	DUAL 2-Input NAND	A0, A1, B0, B1	0.343	0.055	0.305	0.061
NAN2H	2-Input NAND (high drive)	A, B	0.341	0.028	0.300	0.032
NAN3	3-Input NAND	A - C	0.394	0.051	0.403	0.080
NAN3H	3-Input NAND (high drive)	A - C	0.377	0.027	0.405	0.040
NAN4	4-Input NAND	A - D	0.429	0.054	0.578	0.101
NAN4H	4-Input NAND (high drive)	A - D	0.433	0.027	0.579	0.051
NAN5	5-Input NAND	A - E	0.717	0.056	0.937	0.046
NAN6	6-Input NAND	A - F	0.791	0.053	1.085	0.046
NAN8	8-Input NAND	A - H	0.942	0.055	1.316	0.047
NOR2	2-Input NOR	A, B	0.345	0.100	0.290	0.044
NOR2D	DUAL 2-Input NOR	A0, A1, B0, B1	0.345	0.100	0.290	0.044
NOR2H	2-Input NOR (high drive)	A, B	0.371	0.046	0.276	0.025
NOR3	3-Input NOR	A -C	0.477	0.151	0.312	0.044
NOR3H	3-Input NOR (high drive)	A -C	0.490	0.070	0.300	0.024
NOR4	4-Input NOR	A - D	0.736	0.196	0.342	0.045
NOR4H	4-Input NOR (high drive)	A - D	0.757	0.094	0.330	0.025
OAI22	2-Input OR into 2-Input NAND	A - C	0.396	0.088	0.331	0.063
OAI222	Symmetric 2-Input OR into 2-Input NAND	A - D	0.477	0.097	0.513	0.068

Cell Name	Cell Description	Input Signal	Output Rising Base (ns)	Output Rising Load Factor (ns/FO)	Output Falling Base (ns)	Output Falling Load Factor (ns/FO)
OAI23	2-Input OR into 3-Input NAND	A - D	0.455	0.076	0.467	0.076
ORR2	2-Input OR	A, B	0.495	0.055	0.607	0.047
ORR3	3-Input OR	A - C	0.498	0.056	0.836	0.052
XNR2	2-Input Exclusive NOR	A, B	0.406	0.100	0.401	0.062
XOR2	2-Input Exclusive OR	A, B	0.575	0.099	0.592	0.064

I/O cells

Sample of buffers composed of modular I/O building blocks

I/O Options
Input, Output, Bidirectional, Tristate Output and Internal Clock Driver
P&N Drive Value Programmable from 2 mA to 48 mA in 2 mA increments with Slew Rate Control
CMOS or TTL Operation
Schmitt Trigger (Bidirectional, Input)
Testable NAND Gate on Input (Bidirectional, Input)
Inverting Input Buffer (Bidirectional, Input)
Pullup Register - 10K Ω to 320K Ω
Pulldown Register - 7K Ω to 280K Ω

Note: All propagation delays and setup and hold times are in ns.

Soft Macros

Cell Name	Cell Description	Similar to MSI Part Number
STAP	TAP (Test Access Port Controller)	
SALU4	4 BIT ALU	74S381
SALU16	16 BIT ALU	74S381
SROT4	4 BIT Rotator	
SROT16	16 BIT Rotator	
SPG9	9 BIT Parity Generator	74S280
SREG8	8 BIT Register	74S374
SCOMP9	9 BIT Comparator	
SCD8	8 BIT Counter Down	
SCU/D8	8 BIT Up/Counter Down	
SPSR16	16 BIT Parallel Serial Register	
SCU3	3 BIT Counter Up	
SCU4	4 BIT Counter Up	
SCU7	7 BIT Counter Up	
SCU8	8 BIT Counter Up	
SPPWD	Programmable Pulse Width Discriminator	

ATMEL

Contents

Section 10

CMOS Analog

Features

- High Accuracy Programmable Gain Amplifiers
  - ± 0.02 dB Accuracy (Typical)
  - 31.5 dB Range in 0.5 dB Steps
- Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines
- High Dynamic Range - over 90 dB
- On-Chip Anti-Aliasing Filters
- Microcomputer Interface with Serial Data Port
- Three Convenient Clock Options
  - 11.0592 MHz
  - 3.6864 MHz
  - 2.4576 MHz (or 2.56 MHz)
- Operates from +/- 5 V Supplies
- Low Power Standby Mode - 100 µA (Typical)
- TTL and CMOS Compatible Digital Interface
- Economical 16-Lead Package
- Full Military, Commercial and Industrial Temperature Ranges

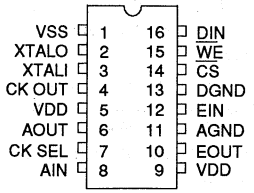
CMOS Programmable Amplifier

Delay Equalizer

Description

The AT76C10 integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a 7-bit configuration code which can be programmed in real time. The AT76C10 is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10 employs sampled-data techniques, and external filters are not required for most applications.

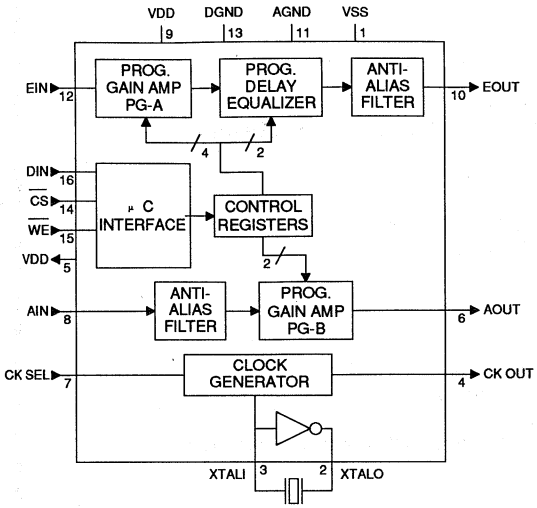
Pin Configuration



Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	VDD	Connect to VDD.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

Block Diagram



Device Operation

The AT76C10 is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10 are controlled by a serial 7-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which controls the power down mode. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
Option Select	Control Code				Address	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10 can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10 provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10s can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$ and $\overline{WE}$ and serial data input DIN allow the AT76C10 to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last 7 input data bits are latched into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10 provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10 can be reactivated by writing a "1" into the power-down register. It should be noted that upon pow-

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 KHz (160 KHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 KHz
DGND	3.6864 MHz	153.6 KHz
VSS	2.4576 MHz	153.6 KHz
VSS	2.56 MHz	160.0 KHz

Group Delay Characteristics (Microseconds)

Fs=153.6 KHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	1	Updates Control Registers
0	1	1	
1	0	1	
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

Table 4. Programmable Gain Amplifier, PG-B

Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

X = Don't Care

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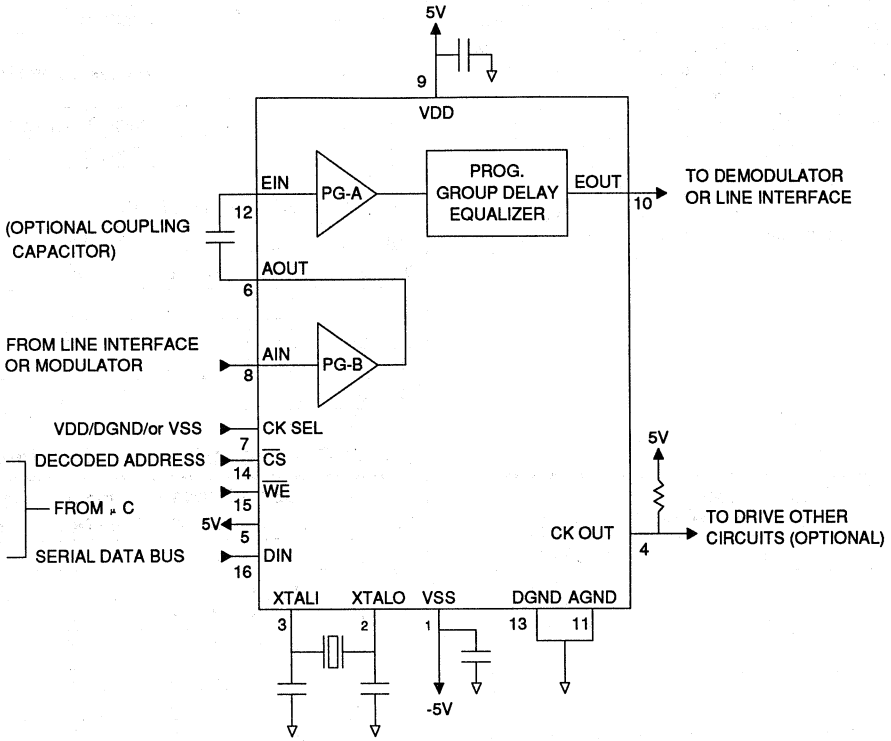
Sample Connection for Typical Application



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6V to VDD + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and A.C. Operating Range

	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5V / -5V ±10%
Industrial	-40° C - 85° C	5V / -5V ±10%
Military	-55° C - 125° C	5V / -5V ±5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	µA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	µA
R_{IA}	Input Resistance at AIN		100			Kohm
R_{IE}	Input Resistance at EOUT	F_S=153.6 KHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	Kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL=20 Kohm	VSS		VDD	Volts
V_N	Output Noise	BW=F_S/2			200	µVrms
THD	Total Harmonic Distortion	RL=20 Kohm V_O=8Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		KHz
V_{FT}	Clock Feedthrough				5	mVpp

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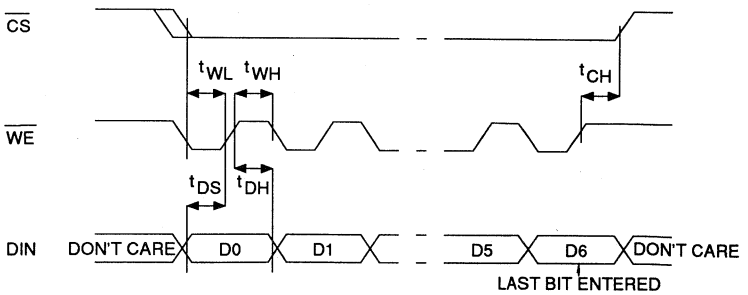
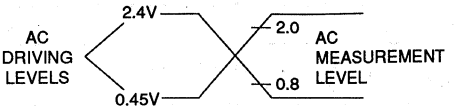
Configuration Code Write Waveform



Digital Timing Parameters

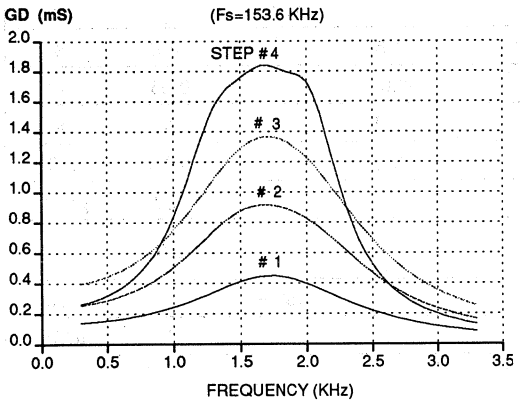
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

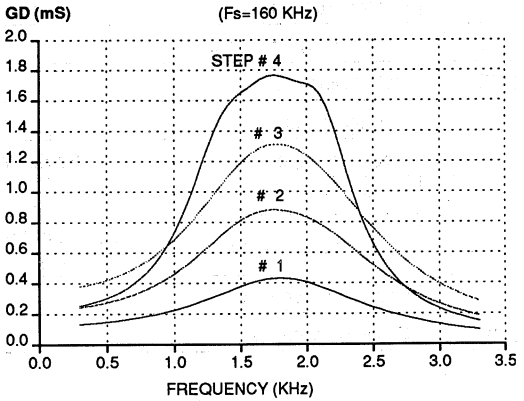


t_R, t_F < 20ns (10% to 90%)

Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10-PC AT76C10-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10-PI AT76C10-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- High Accuracy Programmable Gain Amplifiers
  - ± 0.02 dB Accuracy (Typical)
  - 31.5 dB Range in 0.5 dB Steps
- Software Programmable Group Delay Equalizer For Leased and Dial-Up Lines
- High Dynamic Range - over 90 dB
- On-Chip Anti-Aliasing Filters
- On-Chip E²PROM Configuration Code Memory
- Microcomputer Interface with Serial Data Port
- Three Convenient Clock Options
  - 11.0592 MHz
  - 3.6864 MHz
  - 2.4576 MHz (or 2.56 MHz)
- Operates from +/- 5 V Supplies
- Low Power Standby Mode - 100 µA (Typical)
- TTL and CMOS Compatible Digital Interface
- Economical 16-Lead Package
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT76C10E integrates two Programmable Gain Amplifiers and a Programmable Telephone Line Group Delay Equalizer on a monolithic substrate. It is fabricated in a state-of-the-art, low power CMOS process. The Gain and Group Delay steps are controlled by a 7-bit configuration code which can be programmed in real time and can also be stored permanently in on-chip E²PROMS. The AT76C10E is implemented in an advanced switched-capacitor technology and is designed to provide precise Gain and Group Delay compensation for low bit-error-rate data transmission over dial-up and leased lines. Anti-alias and clock filters are included on-chip as the AT76C10E employs sampled-data techniques, and external filters are not required for most applications.

CMOS E²PROM Programmable Amplifier Delay Equalizer

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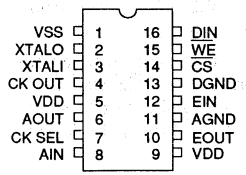
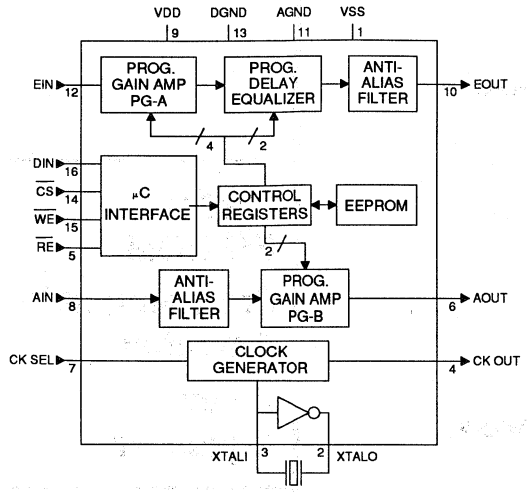
Pin Configuration



Pin Definitions

No.	Pin Name	Function
1	VSS	Negative Power Supply. Nominal -5 Volts.
2	XTALO	Crystal Oscillator Output.
3	XTALI	Crystal Oscillator Input.
4	CK OUT	Sampling Clock Output. (Open Drain)
5	$\overline{RE}$	Recall Enable Input. Loads Configuration into Control Registers from On-Chip E²PROM.
6	AOUT	PG-B Analog Signal Output.
7	CK SEL	Clock Select. Selects one of the 3 recommended Clock frequencies.
8	AIN	PG-B Analog Signal Input.
9	VDD	Positive Power Supply. Nominal +5 Volts.
10	EOUT	Delay Equalizer Analog Signal Output.
11	AGND	Analog Ground.
12	EIN	Delay Equalizer Analog Signal Input.
13	DGND	Digital Ground.
14	$\overline{CS}$	Chip Select Control Input.
15	$\overline{WE}$	Write Enable Control Input.
16	DIN	Serial Data Input.

Block Diagram



Device Operation

The AT76C10E is designed for use in the signal paths of a modem or voice/data phone to minimize the bit-error-rate over dial-up and leased lines. Gain and Group Delay response of the AT76C10E are controlled by a serial 7-bit configuration code. D1 and D0 of the configuration code are the address bits which select one of the three control registers. Bits D2 to D5 set the gain and delay equalizer steps. D6 is an option bit which determines whether the configuration code will update one of the control registers only, or also be stored in on-chip non-volatile memory (E^2PROM) of the AT76C10E. All the functions associated with the configuration code are summarized in Tables 1 to 4.

Configuration Code Format

D6	D5	D4	D3	D2	D1	D0
Option Select	Control Code				Address	

This chip can be used as part of an adaptive equalizer for medium to high speed modems (1200 bps to greater than 19.2K bps). The configuration code is loaded into the chip at a serial data input port and updated in real time. It can also be stored permanently in on-chip E^2PROMS and updated periodically. The high performance Atmel E^2PROM process together with redundancy circuits allows over 10E6 write cycles. The amplitude response of the equalizer is nominally at 0 dB with negligible ripple. The AT76C10E can also be used as a fixed compromise delay equalizer.

PROGRAMMABLE GAIN AMPLIFIER: The AT76C10E provides two high dynamic range amplifiers for maximizing signal-to-noise ratio. Amplifier PG-A offers 16 programmable gain steps from 0 dB to 7.5 dB in 0.5 dB steps. Amplifier PG-B provides -8 to 16 dB of gain in 8 dB steps. The two amplifiers can be cascaded to provide 31.5 dB range of programmable gain in 0.5 dB steps. The Programmable Amplifiers can be used as an Automatic Gain Control Circuit or as a fixed gain adjustment.

PROGRAMMABLE GROUP DELAY EQUALIZER: The Group Delay Equalizer is designed to provide programmable compromise group delay compensation to achieve low bit-error-rate data transmission. Four group delay responses are provided to accommodate the majority of conditioned as well as unconditioned lines. The first three responses are recommended for line types C2 and C1, while the fourth response can be used for 3002-type lines. Two or more AT76C10Es can be cascaded to obtain additional group delay compensation.

CONTROL REGISTERS: Four control registers are used to store the configuration codes for the gain steps of PG-A and PG-B, the delay steps of the Delay Equalizer, and the control bit for the power-down mode. All the control bits, except the power down-bit, can also be programmed into on-chip non-volatile memories of the AT76C10E.

MICROCOMPUTER INTERFACE: Control inputs $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ and serial data input DIN allow the AT76C10E to be easily interfaced with most popular microcontrollers. All digital I/Os are TTL as well as CMOS compatible. For stand alone operation, $\overline{CS}$ should be tied to VDD while $\overline{WE}$, $\overline{RE}$ and DIN should be tied to ground.

WRITE OPERATION: To program a configuration code into a particular control register, the voltage at $\overline{CS}$ has to be brought low while the data bits appearing at DIN are strobed in at the rising edge of $\overline{WE}$. At the rising edge of $\overline{CS}$, the last 7 input data bits are latched into the control registers. Therefore, if the first bit of an update byte is a "start bit," it will be ignored. If a "0" was inserted at D6 of the input code, the configuration code will also be immediately written into on-chip E^2PROM of the AT76C10E. As all timing signals and programming voltages are generated internally, writing the E^2PROM is transparent to the user. However, while the E^2PROM is being programmed, which takes 1.5 mS, any further attempt to initiate programming will be ignored until the first operation is completed.

RECALL OPERATION: A RECALL operation can be initiated any time during operation by bringing both $\overline{CS}$ and $\overline{RE}$ low simultaneously. The configuration codes which have been preprogrammed in the E^2PROM of the AT76C10E are loaded into the control registers.

POWER-DOWN MODE: To minimize power consumption for battery powered applications and in certain linecard applications, the AT76C10E provides a low power standby mode of operation. In the power-down mode, the analog outputs go into a high impedance state. The power-down mode is initiated by writing a "0" into the power-down register. Once in the power-down mode, the AT76C10E can be reactivated by writing a "1" into the power-down register or performing a RECALL operation. It should be noted that upon powering up the AT76C10E for the first time, it automatically goes into the normal active mode of operation.

CRYSTAL OSCILLATOR: Internal timing of the chip is generated either by connecting a crystal across pins XTALI and XTALO of the on-chip oscillator, or by applying an external clock at pin XTALI. In the latter case, pin XTALO should be left unconnected. To accommodate different applications, three clock options: 2.4576 MHz, 3.6864 MHz and 11.0592 MHz, can be selected via control pin CK SEL. For applications in a linecard environment, a 2.56 MHz clock can be used instead of the 2.4576 MHz clock. The 153.6 KHz (160 KHz with 2.56 MHz clock) sampling clock is available as an open drain output at CK OUT for synchronization or driving other circuits, e.g. the transmit or receive filters, or A/D and D/A converters.

CK SEL	Recommended XTAL Frequency	CK OUT
VDD	11.0592 MHz	153.6 KHz
DGND	3.6864 MHz	153.6 KHz
VSS	2.4576 MHz	153.6 KHz
VSS	2.56 MHz	160.0 KHz

Group Delay Characteristics (Microseconds)

Fs=153.6 KHz

Frequency (Hz)	Step #1	Step #2	Step #3	Step #4
300	158	278	416	284
600	188	336	502	386
900	237	463	681	680
1200	325	671	985	1360
1500	431	890	1330	1791
1700	462	938	1382	1838
1900	435	897	1305	1810
2100	372	777	1144	1510
2400	266	542	808	683
2700	181	361	534	342
3000	136	250	368	213
3300	102	182	267	148

Table 1. Option Selection

Address D1	Address D0	Option Bit D6	Function
0	0	0	Writes Control Code into E^{2}PROM and updates Control Registers
0	1	0	
1	0	0	
0	0	1	Updates Control Registers Only
0	1	1	
1	0	1	
1	1	0	Power Down Mode
1	1	1	Active Mode

Table 2. Equalizer Selection

Address D1	Address D0	Control Code D5	D4	D3	D2	Equalizer Step No.	Recommened Line Condition
0	0	X	X	0	0	1	C2
0	0	X	X	0	1	2	C1
0	0	X	X	1	0	3	C1
0	0	X	X	1	1	4	3002

Table 3. Programmable Gain Amplifier, PG-A

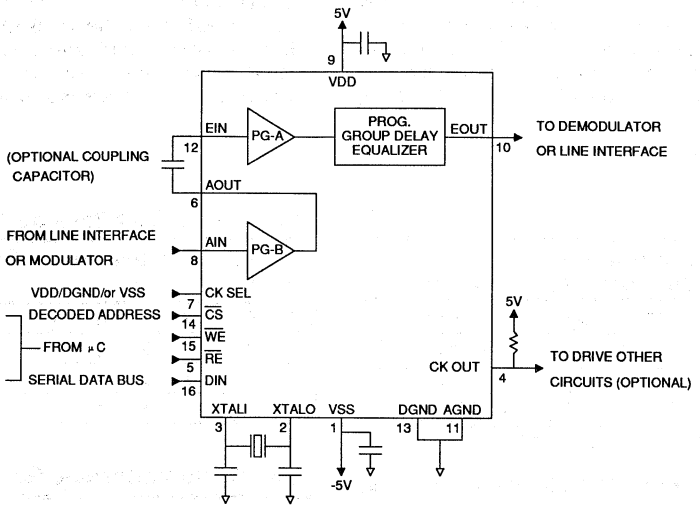
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-A Step No.	PG-A Gain (dB)
0	1	0	0	0	0	1	0.0
0	1	0	0	0	1	2	0.5
0	1	0	0	1	0	3	1.0
0	1	0	0	1	1	4	1.5
0	1	0	1	0	0	5	2.0
0	1	0	1	0	1	6	2.5
0	1	0	1	1	0	7	3.0
0	1	0	1	1	1	8	3.5
0	1	1	0	0	0	9	4.0
0	1	1	0	0	1	10	4.5
0	1	1	0	1	0	11	5.0
0	1	1	0	1	1	12	5.5
0	1	1	1	0	0	13	6.0
0	1	1	1	0	1	14	6.5
0	1	1	1	1	0	15	7.0
0	1	1	1	1	1	16	7.5

Table 4. Programmable Gain Amplifier, PG-B

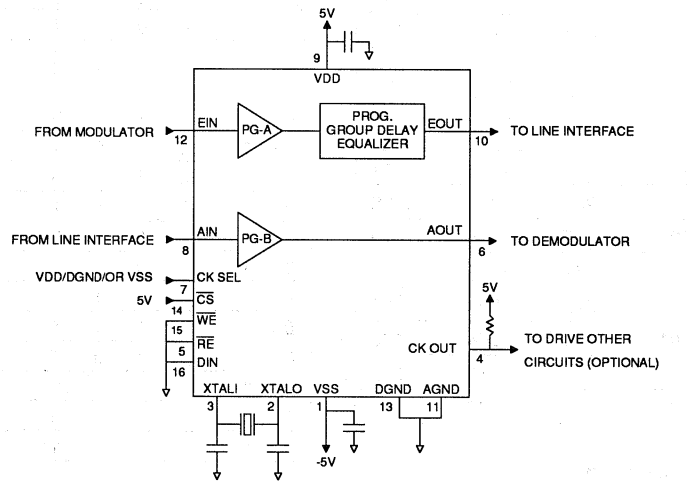
Address D1	Address D0	Control Code D5	D4	D3	D2	PG-B Step No.	PG-B Gain (dB)
1	0	X	X	0	0	1	0.0
1	0	X	X	0	1	2	8.0
1	0	X	X	1	0	3	16.0
1	0	X	X	1	1	4	-8.0

X = Don't Care

Sample Connection for Typical Application



Stand Alone Operation Example



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
Voltage on Pins AGND and DGND with Respect to VSS	-0.6 V to 6.25 V
All Voltages with Respect to VSS	-0.6V to VDD + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

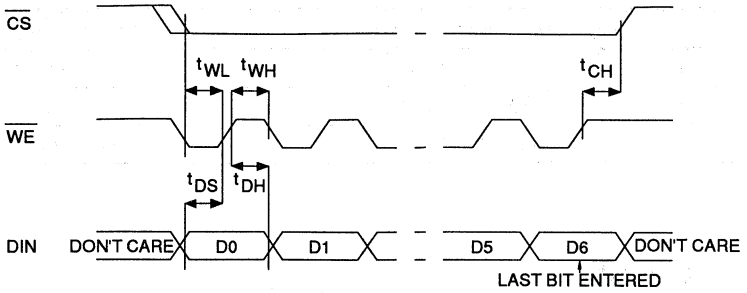
D.C. and A.C. Operating Range

	Operating Temperature (Case)	VDD / VSS Power Supplies
Commercial	0° C - 70° C	5V / -5V ± 10%
Industrial	-40° C - 85° C	5V / -5V ± 10%
Military	-55° C - 125° C	5V / -5V ± 5%

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DDO}	VDD Quiescent Current (active mode)			3	6	mA
I_{SSO}	VSS Quiescent Current (active mode)			3	6	mA
I_{DDP}	VDD Quiescent Current (power-down mode)			100	500	µA
I_{SSP}	VSS Quiescent Current (power-down mode)			100	500	µA
R_{IA}	Input Resistance at AIN		100			Kohm
R_{IE}	Input Resistance at EOUT	F_S=153.6 KHz	1			Mohm
C_I	Input Capacitance				20	pF
ROA	Ouput Resistance at AOUT				1	Kohm
ROE	Ouput Resistance at EOUT				200	ohm
F_O	Center Frequency			1700		Hz
DT	Group Delay Tolerance		-1.5		+1.5	%
GT	Gain Tolerance		-0.05		0.05	dB
G_O	Insertion Loss		-0.15		0.15	dB
V_O	Output Voltage	RL=20 Kohm	VSS		VDD	Volts
V_N	Output Noise	BW=F_S/2			200	µVrms
THD	Total Harmonic Distortion	RL=20 Kohm V_O=8Vpp		0.1	0.5	%
F_S	Sampling Frequency			153.6		KHz
V_{FT}	Clock Feedthrough				5	mVpp

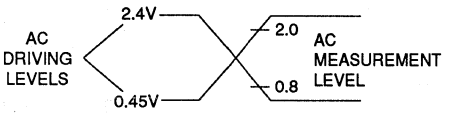
Configuration Code Write Waveform



Digital Timing Parameters

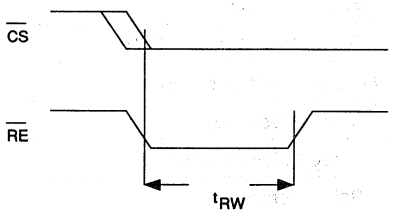
Symbol	Parameter	Min	Max	Units
t_{WL}	Write Enable Low	50		ns
t_{WH}	Write Enable High	50		ns
t_{CH}	$\overline{CS}$ Hold Time	100		ns
t_{DS}	Data Setup Time	40		ns
t_{DH}	Data Hold Time	40		ns

Input Test Waveform

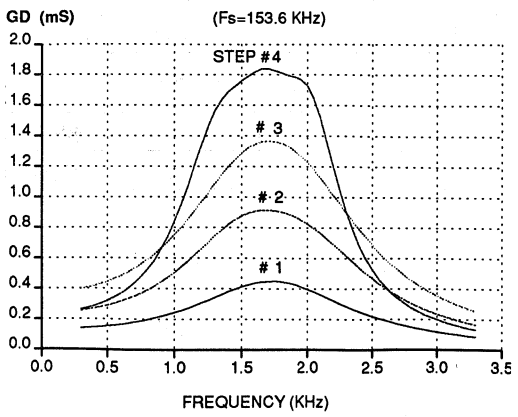


t_R, t_F < 20ns (10% to 90%)

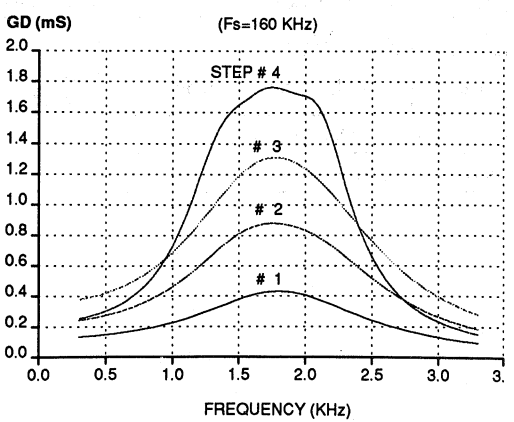
Configuration Code Recall Waveform



Typical Group Delay Response



Typical Group Delay Response



Ordering Information

Delay (ms)	Gain (dB)	Power Supply	Bandwidth (KHz)	Ordering Code	Package	Operation Range
1.8	31.5	±10%	4	AT76C10E-PC AT76C10E-SC	16P3 16S	Commercial (0°C to 70°C)
				AT76C10E-PI AT76C10E-SI	16P3 16S	Industrial (-40°C to 85°C)
1.8	31.5	±5%	4	AT76C10E-DM	16D3	Military (-55°C to 125°C)

Package Type	
16D3	16 Lead, 0.300" Wide Non-Windowed, Ceramic Dual Inline Package (Cerdip)
16P3	16 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
16S	16 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- **Monolithic Dual-Channel 16/18-Bit A/D Converters**
  - **On-Chip Sample/Hold**
  - **Automatic Linearity Error Correction**
- **High Conversion Rates to 96K Samples Per Second at 18 Bits for Each Channel**
- **Capable of Single or Continuous Conversions**
- **Operates from a Single 5V +/- 10% Supply**
- **High Signal-to-Noise Ratio: 90 dB**
- **Single Multiplexed Serial Data Output**
- **High Reliability CMOS Technology**
- **Full Military, Commercial and Industrial Temperature Ranges**

CMOS Dual-Channel 16/18-Bit A/D Converters

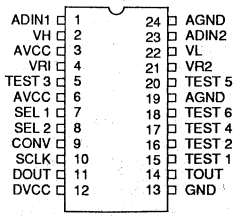
Description

The AT76C120 provides two complete Analog-to-Digital (A/D) Converters integrated on a monolithic substrate. It is designed for Digital Audio and Signal Processing applications as well as Industrial Control and Datacommunication. The Sample/Hold function is incorporated in both A/D channels. Each channel can independently perform 96K 18-Bit conversions per second. The AT76C120 needs a minimum of external components and provides a simple and cost effective solution for applications requiring high resolution A/D conversion.

The AT76C120 is fabricated in a state-of-the-art, low power CMOS process and operates from a single 5V supply. A modified successive approximation algorithm is used to optimize conversion speed. The AT76C120 can perform a single conversion at random or continuous conversions. Linearity errors caused by tap weight variations are automatically compensated by adding a correction factor to each A/D conversion result. The optimum correction factors are factory programmed into each individual chip. The digital output code is presented serially, in 2's complement format.

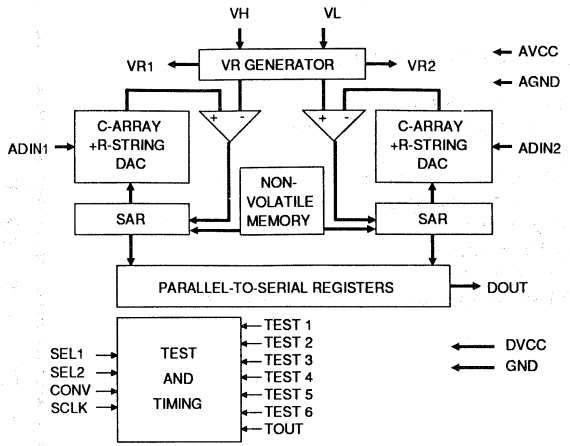
10

Pin Configuration



Pin Name	Function
AGND, GND	Analog Ground, Ground
ADIN1	Analog Input for Channel-1
ADIN2	Analog Input for Channel-2
AVCC	+5V Analog Supply Input
DOUT	Digital Data Output
DVCC	+5V Digital Supply Input
CONV	Convert Clock Input
SCLK	System Clock Input
SEL1	DOUT Mode Select Input
SEL2	16/18-Bit Mode Select Input
TEST 1,2,3,4,5,6	Test Inputs
TOUT	Test I/O
V_H,V_L	Reference Voltage Inputs
VR1,VR2	Channel-1,-2 Reference Voltage Outputs

Block Diagram



Device Operation

Each analog input to the AT76C120 is sampled and held simultaneously once every CONV clock period. As shown in the Block Diagram, the AT76C120 uses a combination of binary ratioed double-polysilicon Capacitor Arrays and Resistor String networks to generate the analog decision levels (or tap weights). The Capacitor Arrays also provide the internal Sample-and-Hold function. A high-gain auto-zeroed Comparator is used to compare an analog input with the decision levels. The Vr Generator supplies internal reference voltages equal to (VH + VL)/2 used by the comparators.

A/D conversion is accomplished through 18-bit Successive Approximation Registers (SAR's). An improved successive approximation scheme is used to optimize conversion speed. The A/D output codes are stored in Parallel-to-Serial Shift Registers and are available at a single multiplexed serial data output port.

System Clock input, SCLK, provides the internal timing reference and the Convert Clock, input CONV, initiates an A/D conversion. The Test and Timing circuits shown in the Block Diagram generate all the timing control signals from SCLK and CONV for sample-and-hold, A/D conversion and tap weight error correction during normal operation as well as tap weight error calibration at the factory.

A minimum of 64 SCLK clock cycles are required for one A/D conversion. The maximum SCLK clock frequency is 6.144 MHz. The minimum 18-bit conversion time for each channel is 10.4 µs, which corresponds to a maximum conversion rate of 96 KHz, making 2X sampling in Digital Audio applications possible.

To minimize overall system cost while achieving high resolution, the AT76C120 compensates for linearity errors caused by tap weight variations by adding a correction factor to each A/D conversion result. This operation is done automatically without the intervention of the host processsor. The optimum correction factors are factory programmed into on-chip non-volatile storage.

The AT76C120 requires only a single 5V supply for operation.

System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the highest performance possible with the AT76C120, critical signal paths, power supply lines and ground planes on the circuit board should be laid out carefully to minimize noise coupling or aliasing into sensitive analog paths. As illustrated in the diagram showing a Sample Connection for Typical Application, a separate AVCC line decoupled to AGND with a tantalum capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C120. Similarly, a separate analog ground return, AGND, which is connected to the most quiet point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath pins 1 to 6 and pins 19 to 24.

High frequency noise on the power and ground lines can be aliased into the passband by the sampling action of the AT76C120. If a switching power supply has to be used, both AVCC and AGND need to be isolated from the system supplies with inductors of appropriate values.

ANALOG INTERFACE: Due to the high sampling rate of the AT76C120, little if any anti-alias filtering is required for most industrial applications. For high performance Digital Audio applications, external Anti-Alias Lowpass or Bandpass Filters, shown as AAFs' in the Sample Connection diagram, should be used to eliminate signals outside the desired passband. Low noise op amps with low output impedances should also be used to supply the analog inputs.

The A/D full-scale range is determined by the voltage applied across pins VH and VL, i.e. (VH - VL). VL is normally connected to the analog ground, AGND, while VH should be supplied by a stable voltage reference.

The internal reference voltage appearing at output pins VR1 and VR2 is nominally (VH + VL)/2.

If the voltage of the input signal can swing below ground, it is necessary to apply an offset to the input to make the AC ground correspond to the mid point of the full scale range, (VH + VL)/2. Outputs VR1 and VR2 provide the AC ground reference as shown in the diagram for Sample Connection.

SYSTEM TIMING: Internal and output data timing of the AT76C120 are synchronized with the system clock, SCLK. To avoid possible synchronization and aliasing problems, deriving the convert clock, CONV, by dividing SCLK by 64 is recommended.

The AT76C120 samples both analog inputs, ADIN1 and ADIN2, once every CONV period. Both inputs are sampled simultaneously, i.e. in-phase. The AT76C120 then performs an A/D conversin on both samples and returns the two resulting 18-bit codes at the serial data output pin, DOUT, during the following CONV clock period.

The convert clock, CONV, is used inside the AT76C120 to initiate sample-and-hold and can also be used by the host processor to latch in the serial 16-bit or 18-bit wide output data.

DIGITAL INTERFACE: The AT76C120 uses a single multiplexed serial data output pin, DOUT. CH-1 and CH-2 data bits are synchronized with SCLK and are available during either the "High" or the "Low" period of convert clock, CONV. A logic "1" at DOUT Mode Select, SEL1, results in the AT76C120 returning the A/D output of CH-1 during the CONV "Low" period, and CH-2 output during the CONV "High" period. A logic "0" at SEL1 results in CH-1 output during the CONV "High" period and CH-2 output during the CONV "Low" period.

The convert clock, CONV, if equal to SCLK divided by 64, makes a transition from "High" to "Low" or vice versa after the LSB is shifted out of DOUT. This allows the serial data to be easily latched into most popular D/A converters or digital signal processors by using CONV rising or falling edges. To further enhance digital interface compatibility, DOUT Mode Select Input, SEL1, allows the user to choose either CONV transitions for both channels.

The AT76C120 allows the user to choose either 16-bit wide or 18- bit wide A/D outputs in 2's complement format. A logic "1" at 16/18 Mode Select Input, SEL2, returns two 18-bit codes at DOUT, while a logic "0" results in 16-bit output codes at CONV rising or falling edges as shown in Input/Output Timing diagram.

In Digital Audio and many signal processing applications, the A/D outputs are further processed by a digital filter. The 18-bit output mode provides better dynamic range and resolution than 16- bit outputs. However, for applications with a 8-bit or 16-bit host microprocessor, 16-bit wide data are more convenient to manage.

SINGLE CONVERSION MODE: When using the AT76C120 in a single conversion mode, please note that the first 15 SCLK periods in each CONV cycle is used for internal sample-and-hold for both channels CH-1 and CH-2. Since the AT76C120 returns the digital conversion results in a subsequent CONV cycle, two CONV periods are in general required to perform a random A/D conversion.

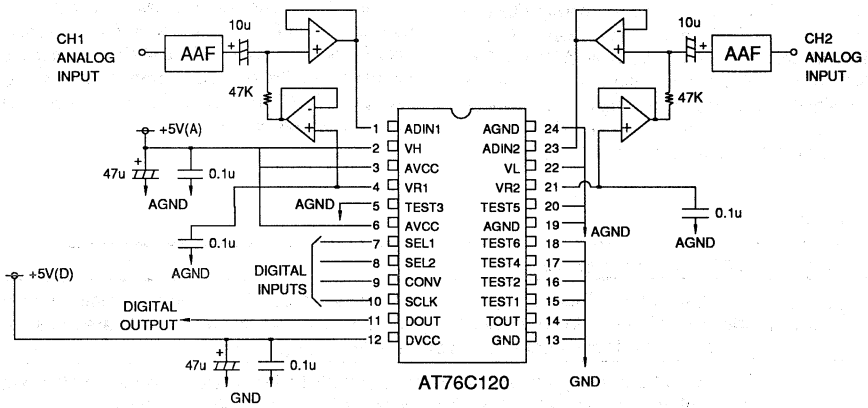
Pin Definitions

	Symbol	Functional Descriptions
Analog Interface	ADIN1 ADIN2	Analog Inputs for Channel-1 (CH-1) and Channel-2 (CH-2). The Sample/Hold function is provided on-chip for both channels. The analog inputs at ADIN1 and ADIN2 are sampled in-phase. Each A/D conversion takes at least 64 SCLK periods.
	V_L V_H	Reference Voltage Inputs. V_L and V_H are normally tied to Analog Ground and the desired full-scale voltage respectively. The full scale range is given by (V_H-V_L). The maximum full-scale voltage can be as high as AVCC.
	VR1 VR2	Reference Voltage Outputs for CH-1 and CH-2. The nominal value at these pins is (V_H+V_L)/2.
Digital Interface	CONV	Convert Clock Input. CONV is normally obtained by dividing the system clock SCLK by 64. The internal Sample/Hold pulse and A/D data output are synchronized with CONV.
	DOUT	Serial Digital Output. DOUT returns two 18-bit serial outputs for CH-1 and CH-2 in 2's complement format. The output data bits are synchronized with SCLK. Please refer to DOUT Timing Diagram for detailed timing relationship with CONV and SCLK.
	SCLK	System Clock Input. The maximum frequency for 18-bit operation is 6.144 MHz. This corresponds to a minimum conversion time of 10.4 µs.
	SEL1	DOUT Mode Select Input. i) SEL1 = "1", CH-1 data output during CONV "Low" CH-2 data output during CONV "High" ii) SEL1 = "0", CH-1 data output during CONV "High" CH-2 data output during CONV "Low"
	SEL2	16/18-Bit Mode Select. i) SEL2 = "1" selects 18-bit A/D mode, ii) SEL2 = "0" selects 16-bit A/D mode.

Pin Definitions (cont'd)

	Symbol	Functional Descriptions
Test Interface	TEST1 TEST2 TEST3 TEST4 TEST5 TEST6	Test Inputs. Normally tied to Ground for TEST 1, 2, 4, 6 and to AGND for TEST 3, 5. These inputs are used for testing and calibration at the factory and are not required for normal A/D operations.
	TOUT	Test I/O. Normally tied to Ground. Like the Test Input pins, this pin is not used for normal A/D operations.
Power Supply	AVCC	Analog Power Input. Nominal 5 Volts. AVCC should be connected to a filtered system supply and kept separate from the Digital Supply.
	DVCC	Digital Power Input. Nominal 5 Volts.
	AGND	Analog Ground. AGND should be kept separate from the digital Ground.
	GND	Digital Ground.

Sample Connection for Typical Application



Notes: 1. AVCC, AGND, +5V (A)— analog supply
2. DVCC, GND, +5V (D)— digital supply
3. Use high quality 0.1µF ceramic chip capacitors.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to AGND and GND	-2.0V to 7.0V(1)
Power Dissipation	1W
Reference Current	10mA
Analog Input Current	10mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is AVCC/DVCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

D.C. and A.C. Operating Range

		AT76C120-1	AT76C120-2	AVCC/DVCC Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.	-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.	-55° C -125° C	-55° C -125° C	5V +/- 5%

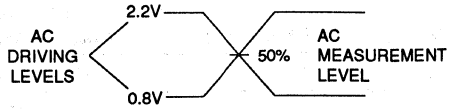
D.C. Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
I_{LI}	Digital Input Load Current	V_{IN}=-0.1V to DVCC+0.1V		10	µA
I_{LO}	Digital Output Leakage Current	V_{OUT}=-0.1V to DVCC+0.1V		10	µA
I_{CCD}	Digital Supply Current			40	mA
I_{CCA}	Analog Supply Current			10	mA
I_{REF}	Reference Input Current			5	mA
V_{IL}	Digital Input Low Voltage		-0.5	0.8	V
V_{IH}	Digital Input High Voltage		2.2	DVCC+0.5	V
V_{OL}	Digital Output Low Voltage	IO=5mA		0.4	V
V_{OH}	Digital Output High Voltage	IO=-5mA	2.4		V
V_{AIN}	Analog Input Voltage		V_L	V_H	V
V_H	Analog Input Voltage at V_H Pin		AVCC-0.5	AVCC	V
V_L	Analog Input Voltage at V_L Pin		0.0	0.5	V

Analog Characteristics (AVCC=DVCC=5V, Ta=25° C)

Symbol	Parameter	Conditions	AT76C120-1 Min	AT76C120-1 Typ	AT76C120-1 Max	AT76C120-2 Min	AT76C120-2 Typ	AT76C120-2 Max	Units
RES	A/D Resolution			18			18		Bits
ILE	Integral Linearity Error				±0.006			±0.01	% FSR
Fs	A/D Sampling Frequency	18-Bit Mode			96			96	KHz
FSE	Full Scale Error				±0.15			±0.15	% FSR
THD	Total Harmonic Distortion	0dB, 1KHz Input			0.01			0.02	%
		-20dB, 1KHz Input			0.02			0.04	%
		-60dB, 1KHz Input			2			4	%
S/N	Signal-to-Noise Ratio				90			84	dB

Input Test Waveforms



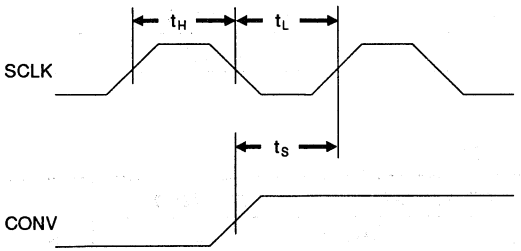
Notes: 1. tR, tF < 30 ns (10% to 90%)
2. Input timing reference is at 1.5V

Digital Output Codes vs. Analog Inputs

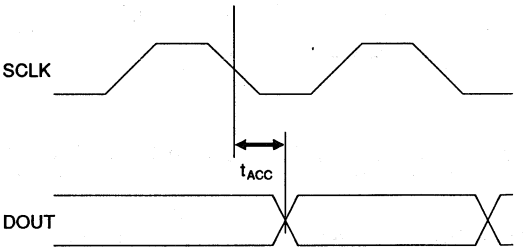
Analog Input	Digital Output Codes MSB...																	...LSB
V_H	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
V_H - 1 LSB[1]	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
.									.									
.									.									
(V_H + V_L) / 2 + 1 LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
(V_H + V_L) / 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
(V_H + V_L) / 2 - 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.									.									
.									.									
V_L + 1 LSB	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
V_L	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: 1. 1 LSB = (V_H-V_L)/262, 144 in 18-bit mode.

Digital Input Waveforms



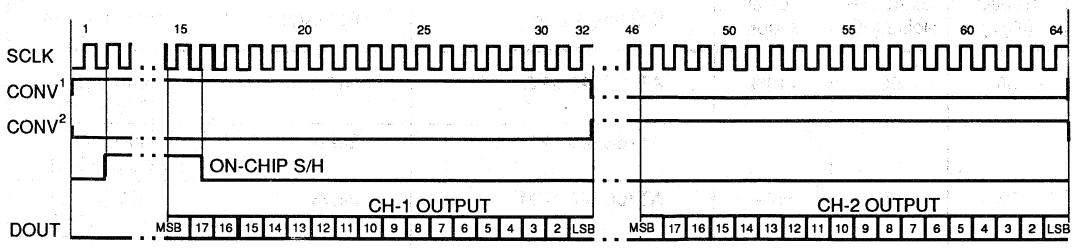
Digital Output Timing Waveforms



Digital Timing Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t_R	Input Rise Time			30	ns
t_F	Input Fall Time			30	ns
t_H	SCLK High Width		50		ns
t_L	SCLK Low Width		50		ns
t_S	CONV Setup Time		40		ns
t_{ACC}	DOUT Access Time	C_{LOAD}=30pF		50	ns
T_{CONV}	CONV Period		10.4		µs
T_{SCLK}	SCLK Period		162		ns

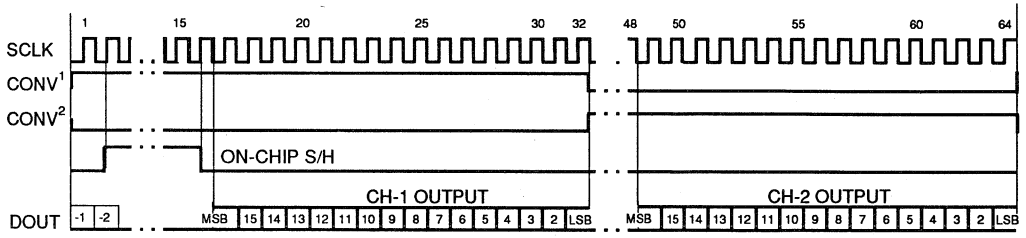
Input/Output Timing for 18-Bit Mode (SEL2="1")



i) SEL1 = "0", CONV [1]
ii) SEL1 = "1", CONV [2]

Notes: CONV = Fs (96KHz Max)
SCLK = CONV x 64

Input/Output Timing for 16-Bit Mode (SEL2="0")



i) SEL1 = "0", CONV [1]
ii) SEL1 = "1", CONV [2]

Notes: CONV = Fs (96KHz Max)
SCLK = CONV x 64

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Ordering Information

Speed (KHz)	Signal-to-Noise (dB)	Power Supply	Ordering Code	Package	Operation Range
96	90	±10%	AT76C120-1PC	24P6	Commercial (0°C to 70°C)
			AT76C120-1PI	24P6	Industrial (-40°C to 85°C)
96	90	±5%	AT76C120-1DM	24D6	Military (-55°C to 125°C)
96	84	±10%	AT76C120-2PC AT76C120-2RC	24P6 24R	Commercial (0°C to 70°C)
			AT76C120-2PI AT76C120-2RI	24P6 24R	Industrial (-40°C to 85°C)
96	84	±5%	AT76C120-2DM	24D6	Military (-55°C to 125°C)

Package Type	
24D6	24 Lead, 0.600" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
24R	24 Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)

Features

- Personal System/2* and VGA* Compatible
- Pixel Rates to 66 MHz
- Triple 6-Bit DACs Display 256K Possible Colors
- Pixel Word Mask and Composite Blank on All Three Channels
- 18-Bit Wide Color Palette Stores 256 Colors
- RGB Video Outputs Drive 37.5 Ohm Loads Directly
- Low Power, Low Glitch Operation
- Asynchronous MPU Read/Write to All Internal Registers
- Available in Standard 28 Pin DIP and 32 Pin LCC
- Full Military, Commercial and Industrial Temperature Ranges

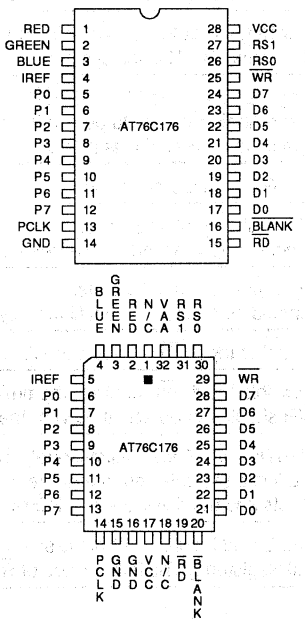
CMOS Triple Video DAC Color Palette

Description

The AT76C176 is a second generation color palette DAC which provides direct drives for RGB color displays. The AT76C176 integrates three high performance 6-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176 supports the RS170 video standard and graphics controllers compatible with the VGA standard. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176 provides composite blank outputs on all three channels. Additional advanced features include on-chip pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette.

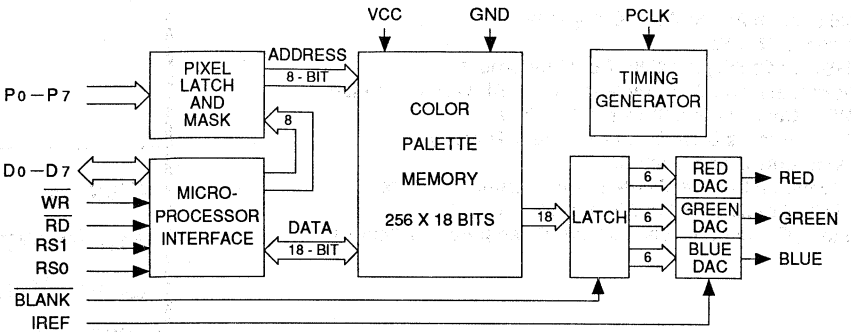
Pin Configurations



Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
GND	Ground
$\overline{RD}$	Read Enable Input
$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	GND	Ground. GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocesssor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, Green second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value Read or Write operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

Device Operation

COLOR PALETTE: The AT76C176 provides an 18-bit wide by 256 word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The 8-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176 achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is 3 PCLK periods.

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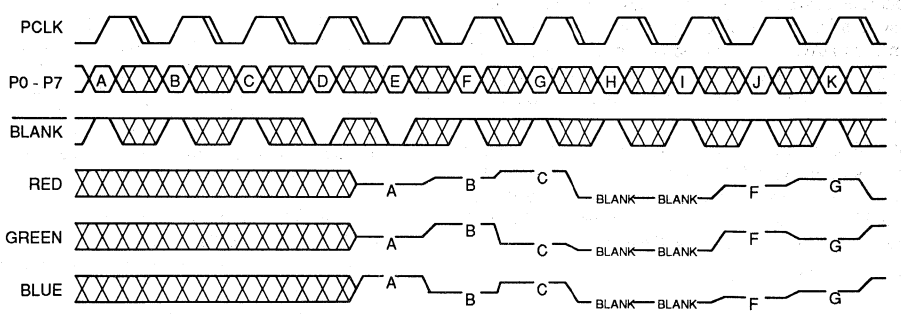
Video Pipeline Timing Diagram



MPU INTERFACE: The AT76C176 provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last 6 LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only 3-byte transfers at D7-D0.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176 consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce a 0.7 Volt peak white level when driving a doubly terminated 75 ohm load with IREF=-8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$

BLANKING: The AT76C176 supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after 3 PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176 features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7.0V(1)
Power Dissipation	1.5W
Reference Current	-15mA
Analog Output Current	45mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is VCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

D.C. and A.C. Operating Range

		AT76C176-66	AT76C176-50	AT76C176-40	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5V +/- 5%
			0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.			-55° C -125° C	5V +/- 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	40MHz Max	50MHz Max	66MHz Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+0.1V		10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC} + 0.1V		10	10	10	µA
I_{CC}	Power Supply Current	IO=21mA Digital Outputs Open		160	170	190	mA
I_{REF}	Reference Current		-7	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IO=5mA		0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO=-5mA	2.4				V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V

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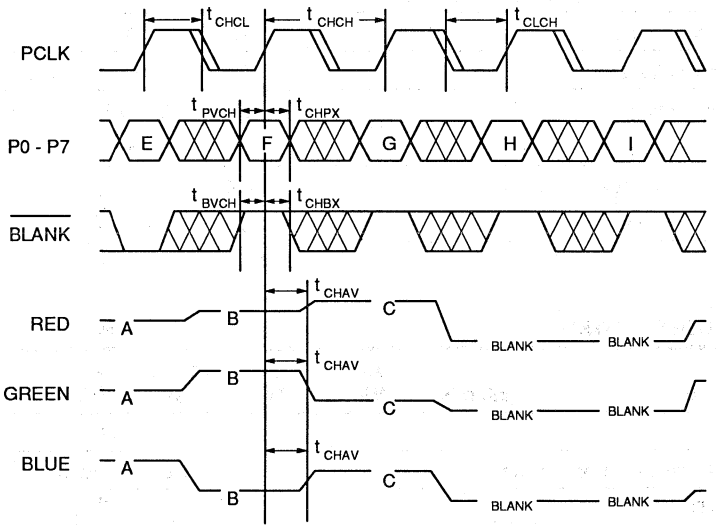
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	40MHz Max	50MHz Max	66MHz Max	Units
RES	Resolution		6					Bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75				pVsec
IO	Output Current	VO<1V		18.6	21	21	21	mA
VO	Output Voltage	IO<21mA		0.7	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	8	6	ns
t_{DF}	Full Scale Settling Time	Notes D, E, F			25	20	15	ns

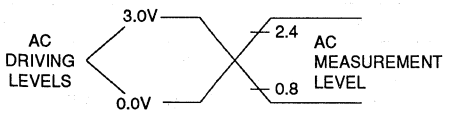
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	40MHz Min	50MHz Min	66MHz Min	Units
t_{CHCH}	PCLK Period (τ)		10000	28	20	15	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH}=\tau$	±2.5				%
t_{CLCH}	PCLK Low Width		10000	9	6	5	ns
t_{CHCL}	PCLK High Width		10000	7	6	5	ns
t_{PVCH}	Pixel Word Setup Time			5	4	3	ns
t_{CHPX}	Pixel Word Hold Time			5	4	3	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			5	4	3	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			5	4	3	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2				ns
t_{CC}	Pixel Clock Transition Time		50				ns

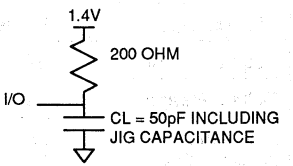
Video Timing Waveforms Diagram



Input Test Waveforms



Digital Input/Output Load



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5V.

MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	40MHz Min	50MHz Min	66MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		15	10	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		15	10	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		15	10	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		15	10	10	ns
t_{DVWH}	Write Data Setup Time			15	10	10	ns
t_{WHDX}	Write Data Hold Time			15	10	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	5	ns
t_{RLQV}	Read Enable Access Time		40				ns
t_{RHQX}	Output Hold Time			5	5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20				ns
t_{WHWL1}	Successive Write Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHRL1}	Write Followed by Read Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHRL1}	Successive Read Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHWL1}	Read Followed by Write Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHWL2}	Write After Color Write	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHRL2}	Read After Color Write	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHRL2}	Read After Color Read	τ=PCLK Period		7τ	7τ	7τ	ns
t_{RHWL2}	Write After Color Read	τ=PCLK Period		7τ	7τ	7τ	ns
t_{WHRL3}	Read After Read Address Write	τ=PCLK Period		7τ	7τ	7τ	ns
t_{WREN}	Read/Write Enable Transition Time		50				ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE=\left[\frac{VO-2.1\times IREF\times R_{Load}}{2.1\times IREF\times R_{Load}}\right]\times 100\%$

Note D: Z_{Load}=37.5 ohm + 30pF, IREF=-8.88mA

Note E: This parameter is sampled and not 100% tested.

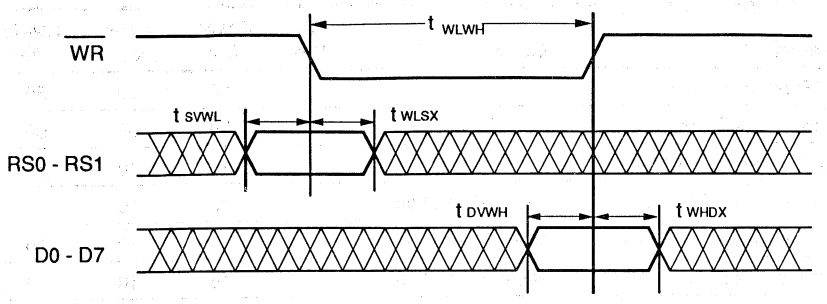
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output half way between successive output values.

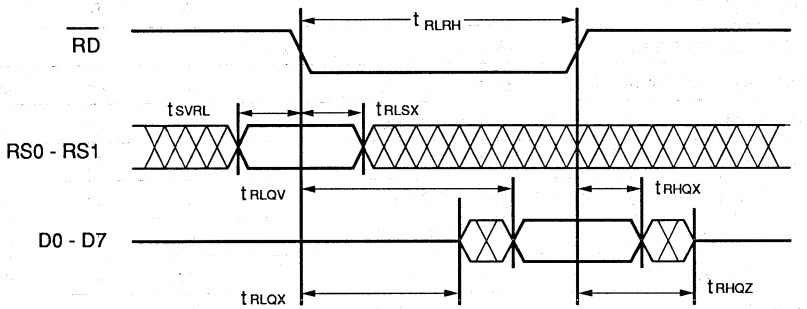
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200mV from steady state output values.

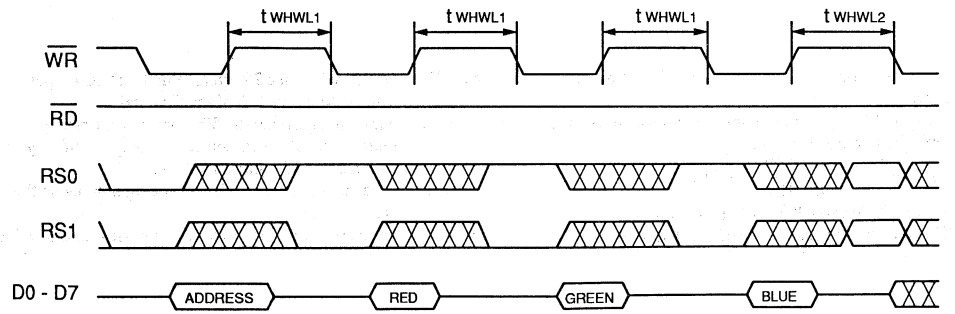
Write Operations Waveforms



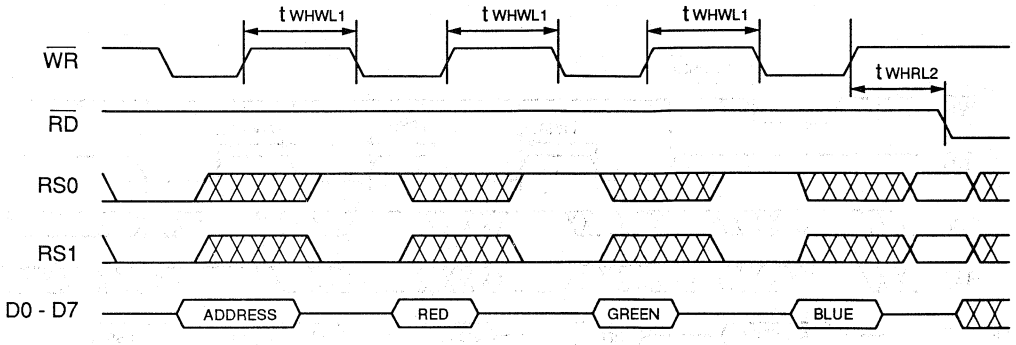
Read Operations Waveforms



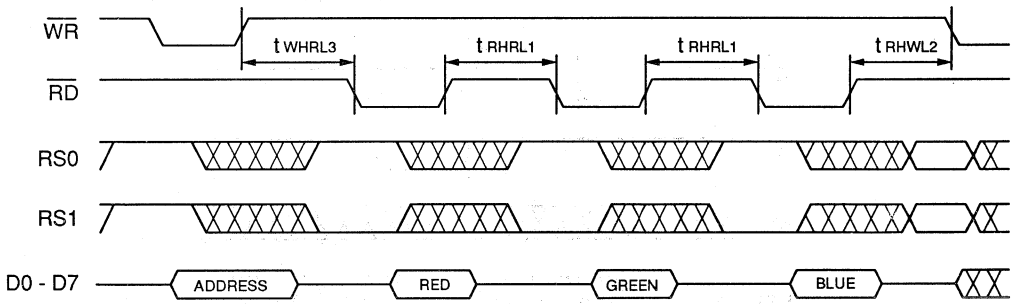
A.C. Waveforms for Color Value Write Followed by Any Write



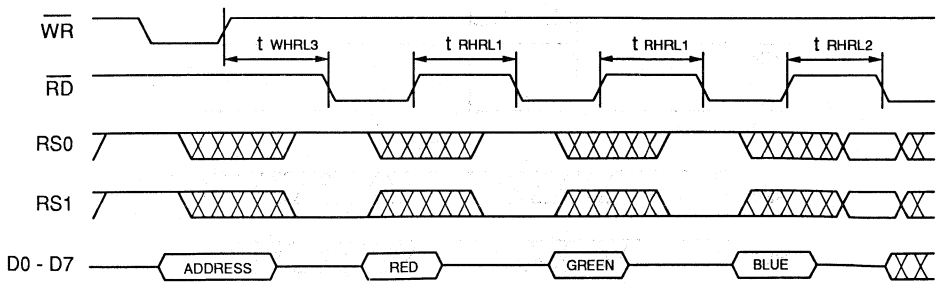
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write



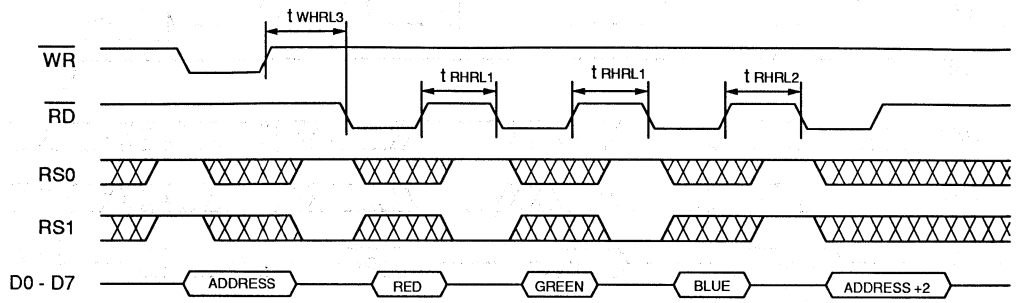
A.C. Waveforms for Color Value Read Followed by Any Read



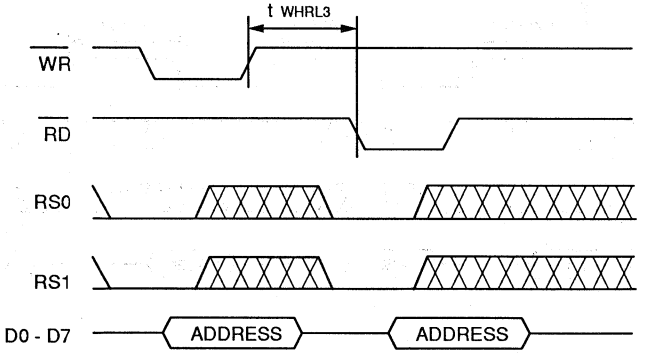
10

A.C. Waveforms for Color Value Read

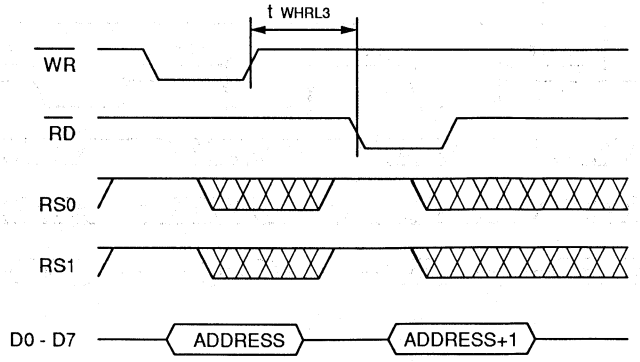
Followed by Pixel Address (Read Mode) Read



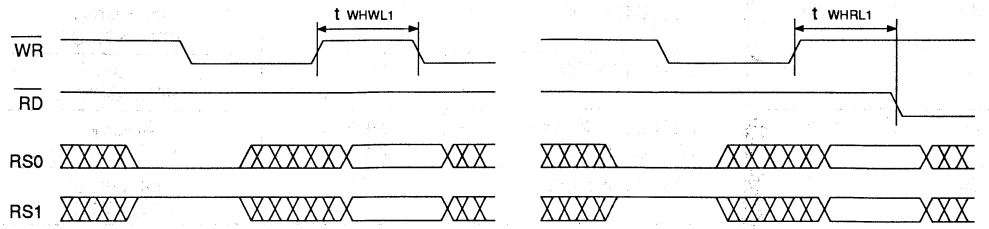
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



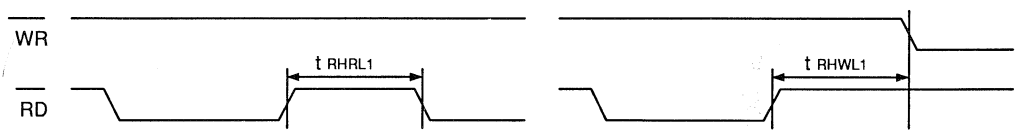
A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back



A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read Followed by Any Read or Write



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
40	±10%	AT76C176-40PC	28P6	Commercial (0°C to 70°C)
		AT76C176-40PI	28P6	Industrial (-40°C to 85°C)
40	±5%	AT76C176-40DMB AT76C176-40LMB	28D6 32L	Military (-55°C to 125°C)
50	±10%	AT76C176-50PC	28P6	Commercial (0°C to 70°C)
		AT76C176-50PI	28P6	Industrial (-40°C to 85°C)
66	±5%	AT76C176-66PC	28P6	Commercial (0°C to 70°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Features

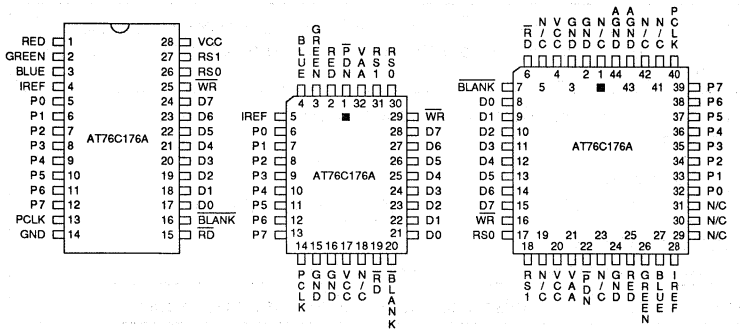
- Personal System/2*, 8514/A, and VGA* Compatible
- High Pixel Rates to 110 MHz
- Supports High Resolution 1280 x 1280 Pixels Color Graphics Displays
- Low Standby Current Less than 100µA
- Anti-Sparkle Circuitry
- Triple 6-Bit DACs Display 256K Possible Colors
- Pixel Word Mask and Composite Blank on All Three Channels
- 18-Bit Wide Color Palette Stores 256 Colors
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Available in Standard 28 Pin DIP, 32 Pin LCC, and 32 and 44 Pin Plastic LCC
- Full Military, Commercial and Industrial Temperature Ranges

Description

The AT76C176A is a second generation color palette DAC which provides direct drives for high resolution RGB color displays with resolutions up to 1280 x 1280 pixels. The AT76C176A integrates three high performance 6-bit video DACs (Digital-to-Analog Converters), an advanced 256 x 18 Color Palette (Color Look-up Table) and a versatile microprocessor interface on a monolithic substrate.

The AT76C176A supports the RS170 video standard and graphics controllers compatible with the VGA and extended VGA standards. This device allows 256 colors to be displayed out of a total of 262,144 colors. The AT76C176A provides composite blank outputs on all three channels. Additional advanced features include on-chip anti-sparkle circuitry and pixel mask logic which allows displayed colors to be modified in a single write cycle rather than by altering the contents of the color palette. For lap-top computers and other battery powered applications, the AT76C176A provides a low power standby mode of operation.

Pin Configurations



Pin Name	Function
RED GREEN BLUE	Analog Video Outputs for R,G,B Guns
IREF	Reference Current Input
P0-P7	Pixel Address Inputs
PCLK	Pixel Clock Input
AGND	Analog Ground
GND	Ground
$\overline{RD}$	Read Enable Input

$\overline{BLANK}$	Video Blanking Input
D0-D7	Program Data I/O
$\overline{WR}$	Write Enable Input
RS0,RS1	Register Select Inputs
$\overline{PDN}$	Power-Down Input
VCC	+5 Volts Supply Input
VAA	+5 Volts Analog Supply Input
N/C	No Connect

* Personal System/2 and VGA are registered trademarks of IBM Corporation.

110 MHz Monolithic CMOS Hi-Res Video Color Palette

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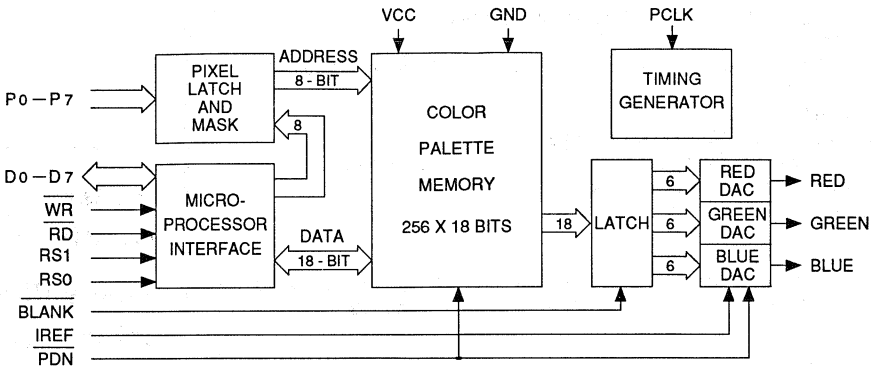
Block Diagram



Pin Definitions

	Symbol	Functional Descriptions
Video Interface	RED GREEN BLUE	Analog Video Outputs. These are the outputs of the triple video DACs. The 18-bit wide color palette output and the $\overline{\text{BLANK}}$ input drive the DAC inputs.
	IREF	Reference Current Input. The Reference Current sets the full scale current sourced by each DAC.
	P0-P7	Pixel Address Inputs. The 8-bit Pixel Address is logically AND'ed with the Pixel Mask value before it is used to select a stored 18-bit color value from the palette.
	PCLK	Pixel (or Dot) Clock Input. The rising edge of PCLK samples the Pixel Address and $\overline{\text{BLANK}}$ inputs. PCLK is the system clock for the palette DAC pipeline.
	$\overline{\text{BLANK}}$	Blanking Input. A logic "0" at $\overline{\text{BLANK}}$ input overrides the current color value and forces the Analog Video Outputs to the zero (or Blank) level. The Color Palette can be updated while Blanking is active.
Power Supply	AGND GND	Ground. Both AGND and GND should be connected to a solid ground plane in the system.
	VCC	Digital Supply. Nominal 5 Volts. VCC should be bypassed to GND with a high-frequency capacitor.
	VAA	Analog Supply. Nominal 5 Volts. VAA should be connected to a filtered system supply.
Microprocessor Interface	$\overline{\text{RD}}$	Read Enable Input. $\overline{\text{RD}}$ controls the timing of microprocessor Read operations.
	$\overline{\text{WR}}$	Write Enable Input. $\overline{\text{WR}}$ controls the timing of microprocessor Write operations. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ should not be active (low) at the same time.
	D0-D7	Program Data I/O Ports (Bidirectional). The rising edge of $\overline{\text{WR}}$ latches Program Data at D7-D0 into the selected internal register. The falling edge of $\overline{\text{RD}}$ enables D7-D0 as outputs and the rising edge of $\overline{\text{RD}}$ returns D7-D0 to a high impedance state.
	RS0, RS1	Register Select Inputs. Control the selection of internal registers. (See description on Internal Registers.) The falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ latches in the value at RS1, RSO.
	$\overline{\text{PDN}}$	Power-Down Input. A logic "0" at $\overline{\text{PDN}}$ input powers down the video DAC and Color Palette circuits for low power standby mode operation. The Color Palette can still be read or updated if PCLK is active. $\overline{\text{PDN}}$ should be held at logic "1" for normal operation.

Internal Registers

RS1	RS0	Bits	Register Name	Functional Description
0	0	8	Pixel Address (Write Mode)	The Pixel Address Register is accessed via Register Address (0,0) or (1,1). Reading the Pixel Address value from (0,0) is the same as reading from (1,1). A pixel address value is normally written to Pixel Address Register at (0,0) before one or more color values are written to the Color Palette. A pixel address value is normally written to Pixel Address Register at (1,1) before one or more color values are read from the Color Palette.
1	1	8	Pixel Address (Read Mode)	
0	1	18	Color Value	The Color Value Register acts as a buffer between the 18-bit wide Color Palette and the 8-bit microprocessor interface. Each READ and WRITE at (0,1) consists of three byte transfers in the order of RED first, Green second and BLUE last. Only the LSBs D5-D0 of each byte are used, the two MSBs are set to "0" when a color value is read. The Pixel Address Register automatically increments after each 18-bit color value Read or Write operation. Each color value READ or WRITE operation overrides the pixel stream for one PCLK period.
1	0	8	Pixel Mask	The Pixel Mask value is bitwise AND'ed with the Pixel Address value at P7-P0. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Address supplied via the microprocessor interface is not affected by the Pixel Mask.

Device Operation

COLOR PALETTE: The AT76C176A provides an 18-bit wide by 256 word deep color palette static RAM array for storing the desired color intensity values. Each word is divided into three fields for the RED, GREEN and BLUE video DACs respectively. The 8-bit wide Pixel Address is decoded and used to select a particular location in the RAM array. The color value retrieved from that location is then used as inputs to the three video DACs which convert the digital color code into analog color intensity values.

The AT76C176A achieves low power, high speed operation by using an advanced pipelined palette DAC architecture. Delay from Pixel Address to color intensity value out is 3 PCLK periods.

MPU INTERFACE: The AT76C176A provides a standard microprocessor interface which allows the host display controller to access the Color Palette RAM and all internal registers of the AT76C176A. MPU READ and WRITE operations are internally synchronized with the video pipeline and therefore can take place asynchronously from the normal pixel mapping operation. An on-chip address counter allows the MPU to READ or WRITE the Color Palette in a Block Mode.

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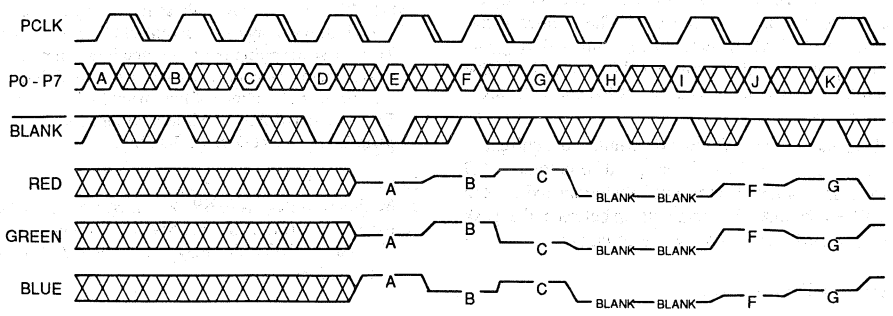
Video Pipeline Timing Diagram



COLOR PALETTE READ AND WRITE: Four MPU operations are required to write (i.e. store a Color Value) to a specific location in the Color Palette RAM. The desired RAM address is first written into the internal Pixel Address register by executing a WRITE operation at register address (0,0). A new Color Value is next written into the internal Color Value register at register address (0,1) by three consecutive WRITE operations, with the RED color first, GREEN second and BLUE last. Only LSBs D5-D0 of each byte transferred are used. The new Color Value is then automatically written into the designated address in the Color Palette RAM.

Similarly, four MPU operations are required to read a Color Value from a specific location in the Color Palette RAM. The RAM address is written into the internal Pixel Address register by executing a WRITE operation at register address (1,1). The Color Value stored in that particular RAM location is automatically transferred to the internal Color Value Register. Three consecutive READ operations are then required to read the retrieved Color Value in three bytes, with the RED color first, GREEN second and BLUE last. Only the last 6 LSBs D5-D0 contain valid data, the two MSBs are set to "0".

BLOCK READ AND WRITE MODE: The on-chip Pixel Address Register automatically increments by one after each complete Color Value READ or WRITE operation. This useful feature allows an entire block of the Color Palette RAM to be accessed by simply writing the starting address into the Pixel Address register at the appropriate register address. Subsequent READ or WRITE operations require only 3-byte transfers at D7-D0.

ANTI-SPARKLE CIRCUITRY: The outputs of the Color Palette RAM drive the inputs of the video DACs via an 18-bit anti-sparkle register. Whenever a Read or Write is performed on the Color Palette through the MPU interface, the anti-sparkle register substitutes the latest pixel Color Value with the previous pixel Color value. Since the Color Value may be corrupted when the Color Palette is accessed during active display, this feature minimizes and often eliminates any visible sparkles on the video display. The anti-sparkle circuitry makes unrestricted access to the Color Palette RAM viable.

TRIPLE VIDEO DAC: Each of the three video DACs on the AT76C176A consists of an array of current sources tied to a common output. The current sources use an advanced current steering scheme to minimize glitch energy. The number of current sources in each DAC steered to the output during any PCLK period equals the value represented by the Color Value selected from the Color Palette. The rest of the current sources are steered to ground.

The input Reference Current (IREF) determines the current in each current source. Each DAC is designed to produce a 0.7 Volt peak white level when driving a doubly terminated 75 ohm load with IREF=-8.88 mA. The relationship between the peak white level and IREF is given by the equation:

$V_{Peak\ White} = 2.1 \times IREF \times R_{Load}$

BLANKING: The AT76C176A supports composite blanking at all three RED, GREEN and BLUE video outputs. The $\overline{BLANK}$ input is latched on the rising edge of PCLK and affects the analog video outputs after 3 PCLK periods. An internal pipelined delay circuit is used to synchronize the $\overline{BLANK}$ input with the normal pixel pipeline. A logic "0" at $\overline{BLANK}$ input overrides the current color value and forces the analog video outputs to the zero (or Blank) level. The $\overline{BLANK}$ circuit has no effect on the MPU interface and the Color Palette remains accessible via READ and WRITE.

PIXEL MASK: The AT76C176A features an advanced on-chip Pixel Mask which is very useful for cursor control, flashing objects, and animation. The Pixel Mask value stored in internal register (1,0) is bitwise AND'ed with the input Pixel Address value at P7-P0 to form the actual RAM address for the Color Palette. A "1" in a position of the Pixel Mask will not change the corresponding bit in the Pixel Address, while a "0" sets that bit to "0". Pixel Addresses supplied via the MPU interface are not affected by the Pixel Mask.

POWER-DOWN MODE: In PLCC packages, the AT76C176A provides an on-chip power-down feature for use in lap-top computers and other battery powered applications. During normal operation, pin $\overline{PDN}$ should be held as logic "1." A logic "0" at $\overline{PDN}$ powers down the video DAC and Color Palette circuits.

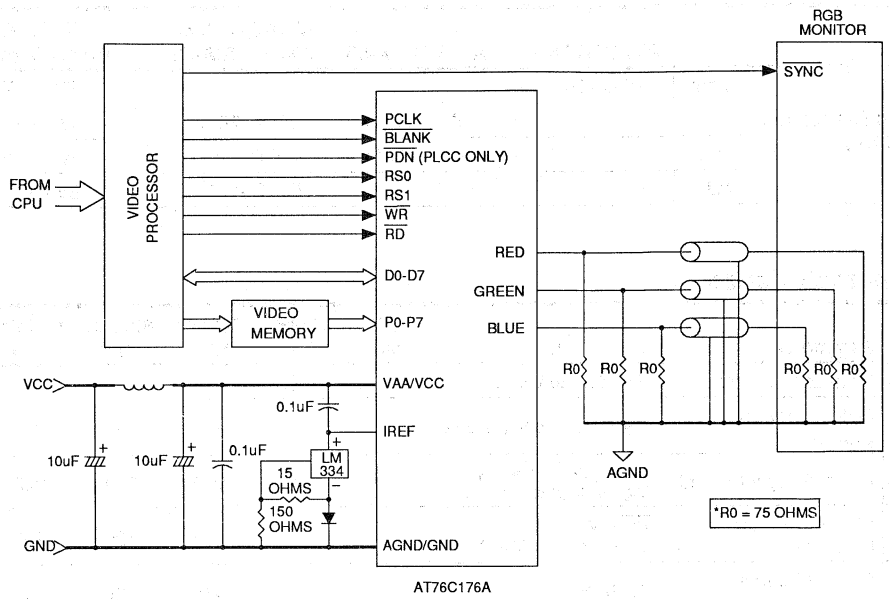
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7.0V(1)
Power Dissipation	1.5W
Reference Current	-15mA
Analog Output Current	45mA
DC Digital Output Current	25mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is VCC+0.75V DC which may overshoot to 7.0V for pulses of less than 20ns.

Sample Connection for Typical Application



System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the cleanest possible analog outputs from the AT76C176A, digital noise coupling into the analog signal paths needs to be minimized. The video data paths, power supply lines and ground planes on the circuit board should be laid out carefully to reduce noise coupling. As illustrated in the diagram showing a Sample Connection for Typical Application, a separate VAA line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C176A. Similarly, a separate analog ground return, AGND, which is connected to the lowest impedance point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath the AT76C176A. All video frequency signal traces should be kept as short as possible to minimize radiation and all decoupling capacitors should be placed as close to the AT76C176A as the layout rules permit.

Noise and transients on the power and ground lines can be coupled or aliased into the video circuits by the switching action of the AT76C176A. For applications at 66 MHz and above, it may be necessary to isolate both VAA and AGND from the system supplies with inductors of appropriate values.

CURRENT REFERENCE: The maximum full scale output of the video DACs is determined by the reference current supplied externally at pin IREF. An adjustable current source such as the LM334 is recommended to set the reference current at 8.88 mA for a full scale output of 0.7 Volt when driving a 37.5 ohm load. The video DACs employ current sources which are referenced to the positive supply voltage. A high quality 0.1 µF chip capacitor may be required to decouple IREF to VAA or VCC.

VIDEO INTERFACE: The Red, Green and Blue video outputs are designed to drive doubly terminated 75 ohm lines. To minimize ringing due to impedance mismatch, 75 ohm +/- 1% thin film resistors should be placed close to the AT76C176A on the PC board.

To comply with FCC RF emission regulations, ferrite beads can be inserted at the video outputs to limit the amount of high frequency emission. The AT76C176A is designed to produce very little high frequency digital feedthrough.

SYSTEM TIMING: The pixel clock, PCLK, controls the timing of the Color Palette and the Video DACs. To obtain the highest quality display possible with the AT76C176A, Setup and Hold time requirements with respect to PCLK should be strictly adhered to. The duty cycle limits of PCLK should also be met over the entire display.

DIGITAL INTERFACE: When the high impedance digital inputs of the CMOS AT76C176A are driven by low impedance sources, considerable ringing can occur, which may degrade high video rate operation. Impedance matching resistors of the order of 50 ohms can be inserted in series at the inputs to the Pixel Address and Blanking inputs to reduce ringing. This also minimizes the amount of high frequency emission due to excessively high slew rates at the video data inputs.

D.C. and A.C. Operating Range

		AT76C176A-11	AT76C176A-80	AT76C176A-66 AT76C176A-50	VCC/VAA Power Supplies
Operating Temperature Range(Case)	Com.	0° C - 70° C			5V +/- 5%
			0° C - 70° C	0° C - 70° C	5V +/- 10%
	Ind.		-40° C - 85° C	-40° C - 85° C	5V +/- 10%
	Mil.			-55° C -125° C	5V +/- 5%

D.C. Characteristics

Symbol	Parameter	Conditions	All Min	50MHz Max	66MHz Max	80MHz Max	110MHz Max	Units
I_{LI}	Input Load Current	V_{IN}=-0.1V to V_{CC}+0.1V		10	10	10	10	µA
I_{LO}	Output Leakage Current	V_{OUT}=-0.1V to V_{CC} + 0.1V		10	10	10	10	µA
I_{CC}	Power Supply Current	IO=21mA, $\overline{PDN}$ = V_{IH} Digital Outputs Open		170	190	210	240	mA
I_{SB}	Standby Supply Current	$\overline{PDN}$=V_{IL} Digital Inputs = V_{IH} / V_{IL}			100	100	100	µA
I_{ILP}	Current Sourced by Pin $\overline{PDN}$	$\overline{PDN}$=V_{IL}			20	20	20	µA
I_{REF}	Reference Current		-7	-10	-10	-10	-10	mA
V_{IL}	Input Low Voltage		-0.5	0.8	0.8	0.8	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	IO=5mA		0.4	0.4	0.4	0.4	V
V_{OH}	Output High Voltage	IO=-5mA	2.4					V
V_{REF}	Voltage at IREF Input		V_{CC}-3	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V

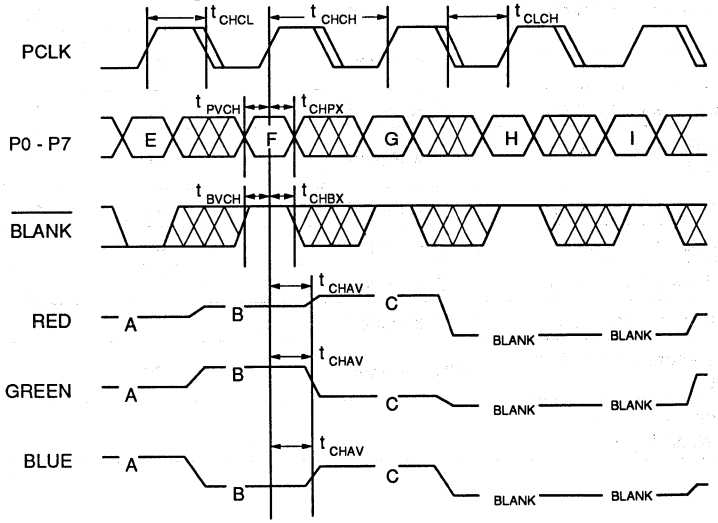
Video DAC Characteristics

Symbol	Parameter	Conditions	All Min	All Typ	50MHz Max	66MHz Max	80MHz Max	110MHz Max	Units
RES	Resolution		6						Bits
ILE	Integral Linearity Error	Note A			±0.5	±0.5	±0.5	±0.5	LSB
COR	DAC to DAC Correlation	Note B			±2	±2	±2	±2	%
FSE	Full Scale Error	Note C			±5	±5	±5	±5	%
DVT	Glitch Energy	Notes D, E		75					pVsec
IO	Output Current	VO<1V		18.6	21	21	21	21	mA
VO	Output Voltage	IO<21mA		0.7	1.5	1.5	1.5	1.5	V
t_{DR}	Rise Time (10% to 90%)	Notes D, E			8	6	6	5	ns
t_{DF}	Full Scale Settling Time	Notes D, E, F			20	15	12.5	9	ns

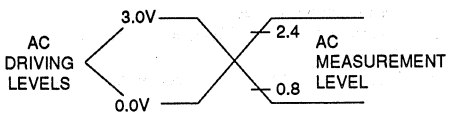
Video Timing Characteristics

Symbol	Parameter	Conditions	All Max	50MHz Min	66MHz Min	80MHz Min	110MHz Min	Units
t_{CHCH}	PCLK Period (τ)	Normal	10000	20	15	12.5	9	ns
Δt_{CHCH}	PCLK Jitter	$t_{CHCH}=\tau$	±2.5					%
t_{CLCH}	PCLK Low Width	Normal	10000	6	5	5	4	ns
t_{CHCL}	PCLK High Width	Normal	10000	6	5	5	4	ns
t_{PVCH}	Pixel Word Setup Time			4	3	3	3	ns
t_{CHPX}	Pixel Word Hold Time			4	3	3	2	ns
t_{BVCH}	$\overline{\text{BLANK}}$ Setup Time			4	3	3	3	ns
t_{CHBX}	$\overline{\text{BLANK}}$ Hold Time			4	3	3	2	ns
t_{CHAV}	PCLK to DAC Output Valid	Note G	30	5	5	5	5	ns
Δt_{CHAV}	Differential Output Delay	Note H	2					ns
t_{CC}	Pixel Clock Transition Time		50					ns

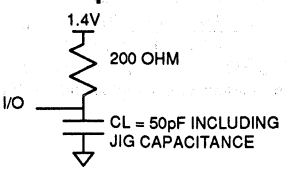
Video Timing Waveforms Diagram



Input Test Waveforms



Digital Input/Output Load



Notes: 1. t_R, t_F <3 ns (10% to 90%).
2. Input timing reference is at 1.5V.

10

MPU Interface Timing Characteristics

Symbol	Parameter	Conditions	All Max	66/50MHz Min	80MHz Min	110MHz Min	Units
t_{WLWH}	$\overline{WR}$ Pulse Width Low			50	50	50	ns
t_{RLRH}	$\overline{RD}$ Pulse Width Low			50	50	50	ns
t_{SVWL}	Register Select Setup Time	WRITE Operations		10	10	10	ns
t_{SVRL}	Register Select Setup Time	READ Operations		10	10	10	ns
t_{WLSX}	Register Select Hold Time	WRITE Operations		10	10	10	ns
t_{RLSX}	Register Select Hold Time	READ Operations		10	10	10	ns
t_{DVWH}	Write Data Setup Time			10	10	10	ns
t_{WHDX}	Write Data Hold Time			10	10	10	ns
t_{RLQX}	Output Turn-on Delay			5	5	5	ns
t_{RLQV}	Read Enable Access Time		40				ns
t_{RHQX}	Output Hold Time			5	5	5	ns
t_{RHQZ}	Output Turn-off Delay	Note I	20				ns
t_{WHWL1}	Successive Write Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHRL1}	Write Followed by Read Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHRL1}	Successive Read Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHWL1}	Read Followed by Write Interval	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHWL2}	Write After Color Write	τ=PCLK Period		4τ	4τ	4τ	ns
t_{WHRL2}	Read After Color Write	τ=PCLK Period		4τ	4τ	4τ	ns
t_{RHRL2}	Read After Color Read	τ=PCLK Period		7τ	7τ	7τ	ns
t_{RHWL2}	Write After Color Read	τ=PCLK Period		7τ	7τ	7τ	ns
t_{WHRL3}	Read After Read Address Write	τ=PCLK Period		7τ	7τ	7τ	ns
t_{WREN}	Read/Write Enable Transition Time		50				ns

Notes

Note A: Measured from best fit line through DAC transfer curve.

Note B: Measured from the mid point of the distribution of the three DAC transfer curves.

Note C: $FSE=\left[\frac{VO-2.1\times IREF\times R_{Load}}{2.1\times IREF\times R_{Load}}\right]\times 100\%$

Note D: Z_{Load}=37.5 ohm + 30pF, IREF=-8.88mA

Note E: This parameter is sampled and not 100% tested.

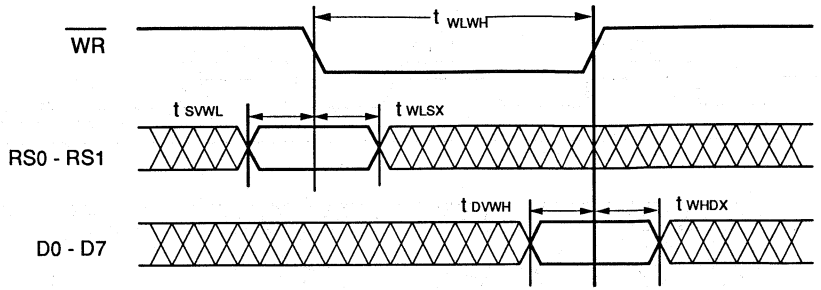
Note F: Measured from a 2% change in the DAC output voltage to within 2% of the final value.

Note G: Measured between the 50% point of the rising edge of PCLK and at the analog output half way between successive output values.

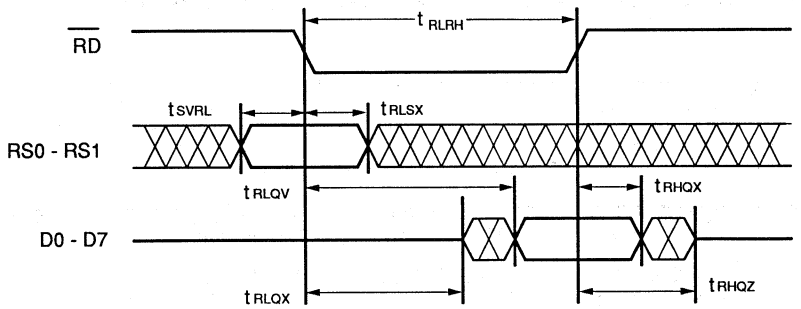
Note H: Measured between different analog outputs on the same device.

Note I: Measured at ±200mV from steady state output values.

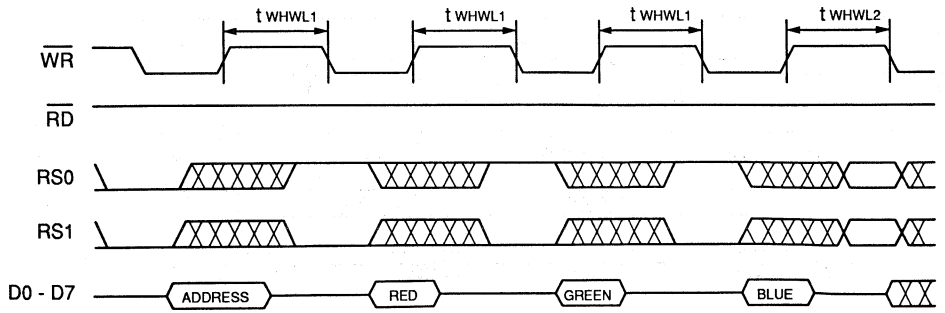
Write Operations Waveforms



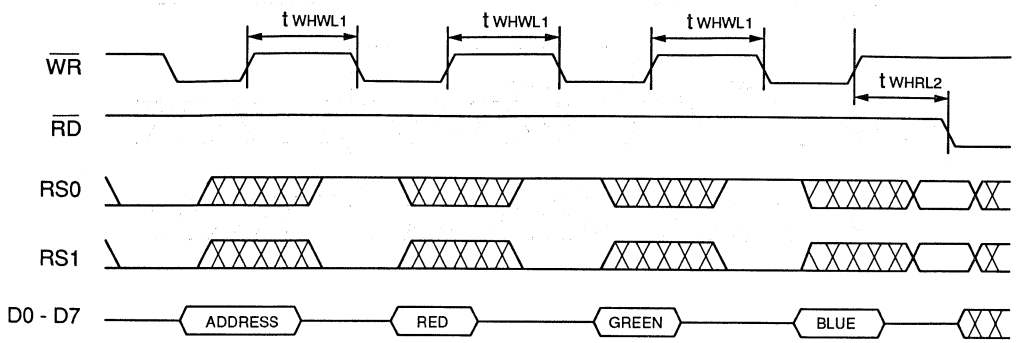
Read Operations Waveforms



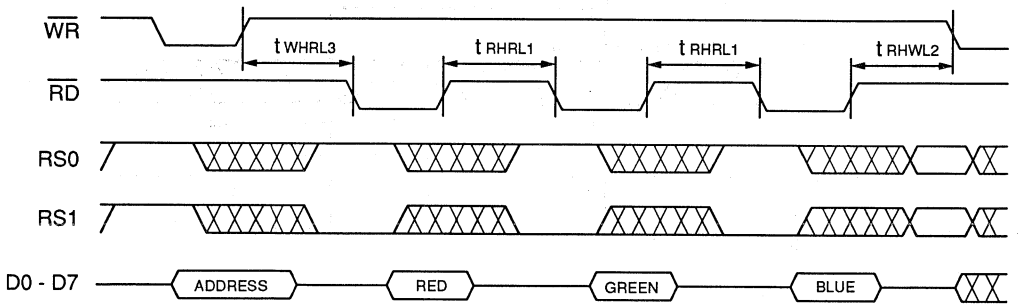
A.C. Waveforms for Color Value Write Followed by Any Write



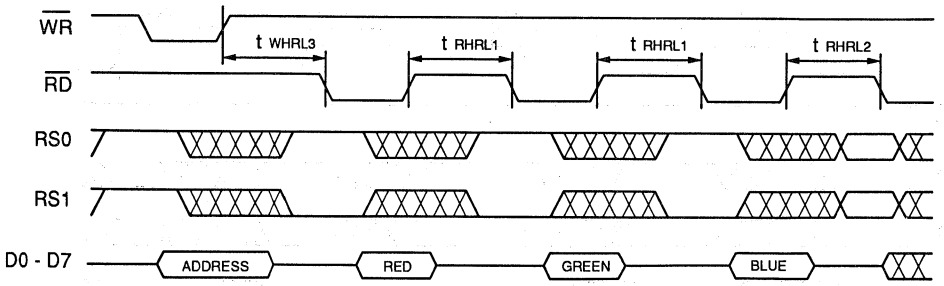
A.C. Waveforms for Color Value Write Followed by Any Read



A.C. Waveforms for Color Value Read Followed by Any Write

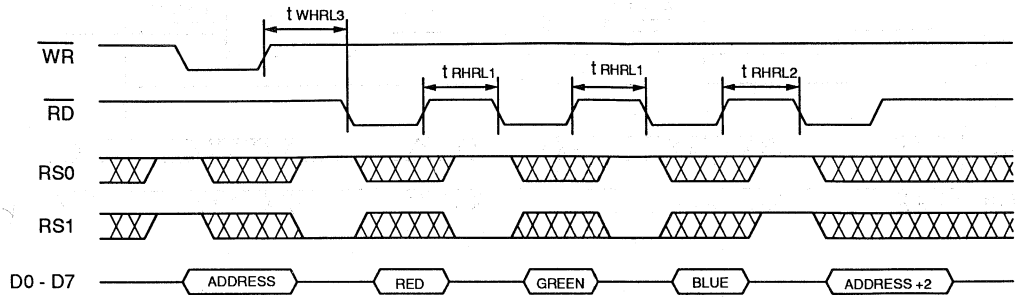


A.C. Waveforms for Color Value Read Followed by Any Read

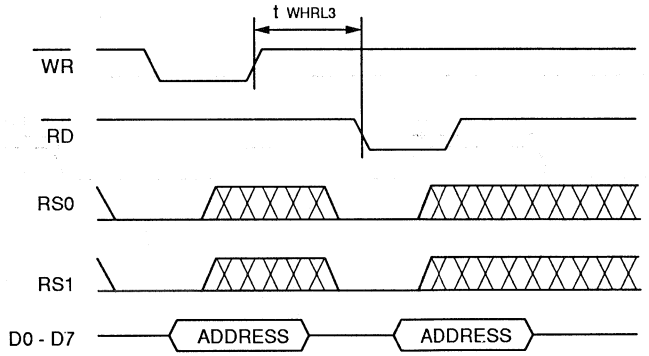


A.C. Waveforms for Color Value Read

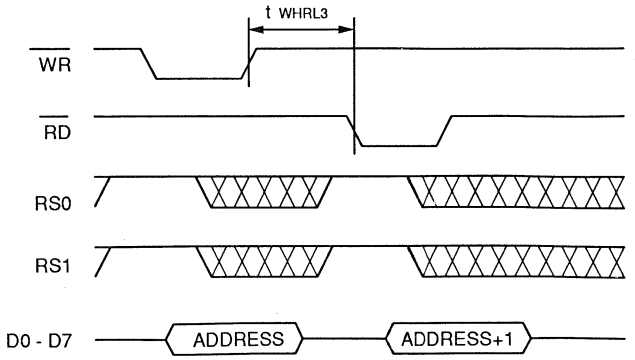
Followed by Pixel Address (Read Mode) Read



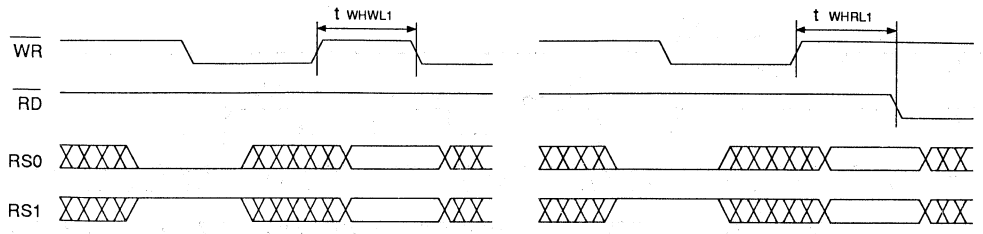
A.C. Waveforms for Pixel Address (Write Mode) Write and Read Back



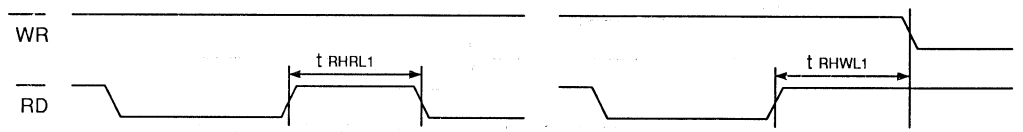
A.C. Waveforms for Pixel Address (Read Mode) Write and Read Back



A.C Waveforms for Pixel Mask Write Followed by Any Write or Read



A.C. Waveforms for Pixel Mask or Pixel Address Read Followed by Any Read or Write



Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
50	±10%	AT76C176A-50PC AT76C176A1-50JC AT76C176A2-50JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-50PI AT76C176A1-50JI AT76C176A2-50JI	28P6 32J 44J	Industrial (-40°C to 85°C)
50	±5%	AT76C176A-50DMB AT76C176A-50LMB	28D6 32L	Military (-55°C to 125°C)
66	±10%	AT76C176A-66PC AT76C176A1-66JC AT76C176A2-66JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-66PI AT76C176A1-66JI AT76C176A2-66JI	28P6 32J 44J	Industrial (-40°C to 85°C)
66	±5%	AT76C176A-66DMB AT76C176A-66LMB	28D6 32L	Military (-55°C to 125°C)
80	±10%	AT76C176A-80PC AT76C176A1-80JC AT76C176A2-80JC	28P6 32J 44J	Commercial (0°C to 70°C)
		AT76C176A-80PI AT76C176A1-80JI AT76C176A2-80JI	28P6 32J 44J	Industrial (-40°C to 85°C)
110	±5%	AT76C176A-11PC AT76C176A1-11JC AT76C176A2-11JC	28P6 32J 44J	Commercial (0°C to 70°C)

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Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Contents

Section 11

Packaging Services

Features

- **Capability to .004" Lead Pitch**
- **Superior Resistance, Capacitance and Inductance Compared to Wirebond**
- **Hermetic and Non-hermetic Options**
- **Customer Configurable Lead Frame Pattern**
- **Customer Configurable Package Footprint**
- **Proven Cryogenic Temperature Performance with Solder Bumps**

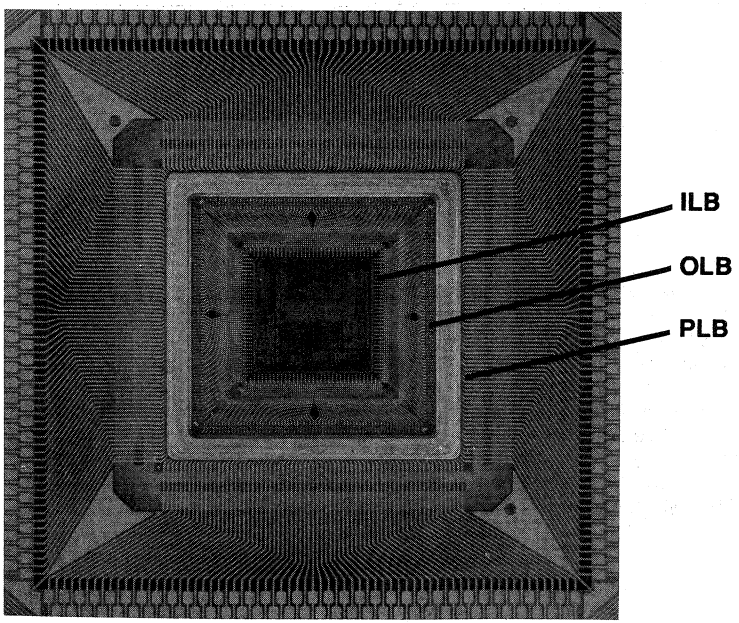
Wafer Bumping and Tape Automated Bonding Technology

Description

Tape Automated Bonding (TAB) is a surface-mount packaging technology for integrated circuits which provides the highest lead density and smallest footprint available for fully-tested die. A pattern of leads is formed in a thin sheet of copper which allows chip contact on the inside of the pattern, and contact to external circuits at the lead terminations on the outside of the pattern.

The hermetic package option requires the use of two lead frames, one for the connection of chip to inner package contacts and one for connection of outer package contacts to the circuit board. The non-hermetic package option requires only one frame, providing a continuous TAB lead frame connection between chip and either a circuit board or another package. These options in non-hermetic TAB make it suitable for custom pin-out requirements such as those necessary in modules. In addition, chip-on-tape (with no package) is also available.

The final configuration of the TAB package may conform to a standard product offering or may be customized to the electrical and mechanical requirements of the customer, allowing unprecedented flexibility in finished product design.



Bump/TAB Technology

The integrated circuit intended for TAB packaging must be appropriately prepared in wafer form. The application of solder or gold bumps to the chip's bond pads forms the contact medium between chip and lead frame. An additional masking step is required to accommodate the plating process necessary for bump formation on the wafer surface.

Inner Lead Bond (ILB) - To make the ILB connection, the TAB frame is attached to bumps formed on the chip in the wafer manufacturing process. In the solder bump process, bumps are reflowed in contact with the TAB lead, forming a resilient bond capable of withstanding the temperature extremes of cryogenic cycling. All bumps are reflowed at once allowing for high throughput. In addition, solder bumps are reworkable.

In the gold bump process, ILB connections are formed by gang bonding or single-point bonding, depending on die configuration.

Outer Lead Bond (OLB) - OLB connection (for hermetic packages) is secured by single-point welds of the circuit side of the lead frame to the internal package contacts. At this stage the package may continue in the TAB process for leaded designs or, for leadless configurations, may be sealed and submitted to finishing processes such as test.

Package Lead Bond (PLB) - The PLB connections (for hermetic packages) consist of attaching another TAB lead frame to the outer contact of the package body with a thermo-compression bond. This lead creates the final electrical contact to the external circuit.

Capabilities

Features	Description
Bump Metallurgies	Au, Pb/Sn, Au/Sn
Bump Configuration	Mushroom bumps in Au, Pb/Sn Straight wall bumps in Au
Bump Height	Au - 20 µ to 25 µ typical, or as specified Pb/Sn - 75 µ to 100 µ typical, or as specified
Bump Spacing	Au - 40 µ minimum Pb/Sn - 100 µ minimum
Bump Dimensions	Au - 50 µ x 75 µ Pb/Sn - Size 100 µ
Field Metal Deposition and Etching	Ti, TiW, Cu, Ni, NiFe, Pd, Au
Photolithography	Aqueous Photoresist Polyimide

Bump Mask Requirements

Wafer Size	Mushroom Gold or Solder	Straight-Wall Gold
4" Wafers	5" x 5" mask, 0.150" thick, dark field with no street openings	5" x 5" mask, 0.150" thick, light field with no street openings
5" Wafers	7" x 7" mask, 0.150" thick, dark field with no street openings	7" x 7" mask, 0.150" thick, light field with no street openings
6" Wafers	7" x 7" mask, 0.150" thick, dark field with no street openings	7" x 7" mask, 0.150" thick, light field with no street openings

Wafer Bumping Services

Wafers are readied for bumping by redefining the bond pads through the passivation layer. Titanium/Tungsten is sputtered on the wafer followed by a layer of nickel (for solder bumps), or layers of palladium and gold (for gold bumps). Another layer of titanium/tungsten is deposited for photoresist adhesion and seed-layer protection. After photoresist deposition, the layer of titanium/tungsten is etched from the bond pads. The bumps are then plated to the field metal on the bond pads, and solder bumps are reflowed or gold bumps are annealed. To complete the process, photoresist and field metals are stripped, and a final cleaning step is performed.

Atmel's bump process is compatible with all types of wafer processes, including GaAs. Ideally, passivated wafers are provided for bumping, however Atmel can provide masks and passivation in addition to the remainder of the bump process.

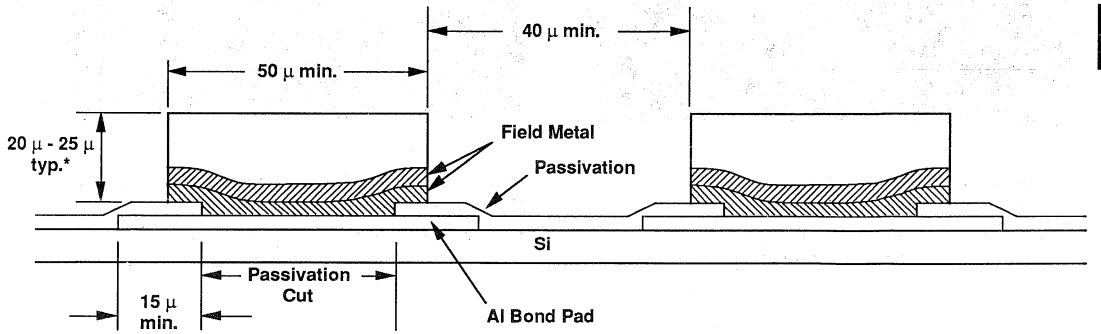
Services

- Complete wafer bumping processes or individual steps in the process.
- Design and generation of masks for the wafer bumping process.
- Experienced engineering staff and strict manufacturing processes monitored with Statistical Process Control.

Bump Design Rules

Feature	Gold	Solder
Passivation Opening Size	15 µ minimum from outside edge of bond pad	15 µ minimum from outside edge of bond pad
Passivation Opening Shape	Square or rectangle preferred	Round
Size of Bump Opening on Bump Mask	Minimum of .002" x .004" (50 µ x 100 µ) for rectangle or .003" x .003" (75 µ x 75 µ) for square	Minimum of .003" (75 µ) in diameter

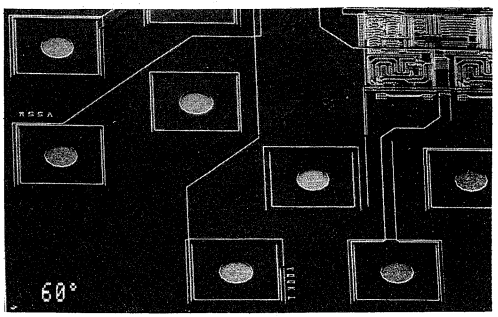
Straight Wall Gold Bump



*or as specified

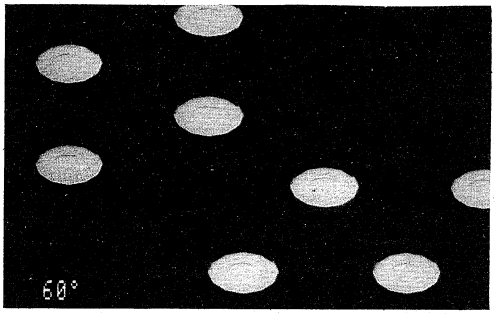
Atmel Solder Bump Process

Wafer Complete with Passivation Openings



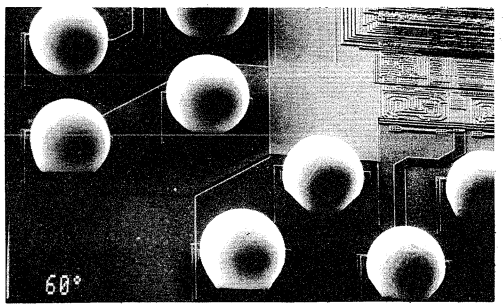
Normal square bond pads.
Small, circular openings define attachment cross-section.

Masked Wafer Ready for Bump Plating



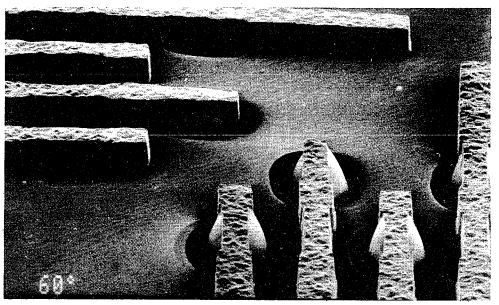
Somewhat larger opening defines base of bump.
Barrier material is photoresist.

Wafer with Bumps Plated on Bond Pads



Photoresist has been removed.
Bumps are approximately 120 µ wide.
Bumps are approximately 90 µ high.
Extraordinary uniformity of size and profile.

Lead Frame Attached to Single Chip



Solder bumps have been reflowed onto lead frame.
Kapton barrier protects chip.
Lead overhang provides mechanical stability.

Specifications

Inner Lead Bond		
Technologies	Thermocompression Thermosonic Au/Au and Au/Sn to peripheral or array bumped die Reflow Au/Sn and Pb/Sn to peripheral or array bumped die	
Lead Frame Media	Cu, Cu/Polyimide, Cu/Adhesive/Polyimide 35 mm/4 pitch to 70 mm/14 pitch Lead Pitch: .003" + (75 µ +) Lead Width Range: .001" to .004" (25 µ to 100 µ)	
Chip Configuration	Size Range (sq.): .073" to .600" (1.9 to 15.2 mm) Thickness Range: .015" to .030" (.37 to .75 mm) Bump Metalurgies: Au, Pb/Sn I/O Counts: 6 to 400+	
Product Handling	Chip Presentation Lead Frame ILB Component	Automatic magazine feed Manual Reel-to-reel Single-site chip carrier with magazine supercarrier Reel Single-site chip carrier with magazine supercarrier
Alignment Tolerance	+/-.0004" (10 µ)	

Frame Mount and Excise		
Equipment	35 mm, Super 35 mm 48 mm-70 mm Excise	Automatic cut, frame, load into magazines Manually operated cut and frame Tooling product-configurable per OLB, die attach requirements

Outer Lead Bond	
Technology	Single-point weld Cu/Au, Au/Au, solder Pitch Range: .008" (200 µ)
Mounting Media	Ceramic leaded or leadless package Plastic leaded or leadless package Various ceramic/glass, organic substrates

Package Seal	
Hermetic/Non-hermetic	Au/Sn kovar resistance and furnace seal Epoxy lid/package Epoxy coat

Package Lead Bond	
Technology	Thermocompression segment gang bond Au/Au Pitch range: .003"+(75 µ+)
Mounting Media	Ceramic leaded or leadless package

Performance

System designers have reduced system clock cycle times from well over 100 ns in early system generations to less than 20 ns in commercial systems in development. The significance of the allowance in the system clock cycle for signal edge quality degradation has become correspondingly greater. Since an allowance of between one and three nanoseconds may be required, this allowance as a portion of the system clock has risen from about two percent for early generations to roughly ten percent for systems currently in development. Packaged silicon integrated circuits do not typically provide a controlled environment for fast rise- or fall-time signals through the packaging medium, though PCB designs usually accommodate signal plane isolation through ground or supply-plane shielding. The emphasis on shielding allows the PCB designer to control inductance as an influence on signal quality in the PCB medium. In spite of this control in the PCB medium, the circuit implementation may still have difficulty accepting uncontrolled nodes at the integrated circuit interfaces. The geometry of the TAB package typically results in lower inductance than packages requiring wirebonds, as shown. Resistances are also lower since there are no thick-film conductor layers in the signal path of a non-hermetic TAB package and the straight-wire TAB conductor is usually made of copper. In performance oriented systems, a TAB package can provide a superior interface when compared to wire-bonded packages.

Thermal Shock Performance of Soft Solder Bump Process

The TAB assembly technology using soft solder bumps was initially qualified with thermal shock tests to establish its performance capabilities. These same tests are performed periodically throughout the life cycle of a product.

Atmel subjects TAB assembled product to thermal shock tests to determine the resistance of the device to sudden exposure to extreme temperature changes. This environmental test accelerates the effects of a mismatch in thermal expansion between different components of the packaging system. Such a mismatch can cause bond problems.

In the stress procedure, the devices are placed into a fluorocarbon bath heated to +100°C. After at least five minutes, the parts are quickly transferred to an adjoining chamber filled with liquid nitrogen at -195°C for an equal amount of time. The thermal shock readpoint tests, which consist of continuity electrical tests, are conducted after 50, 100, 150 and 200 cycles (the normal number of cycles for Method 1011 of MIL-STD-883C is 15 with a LTPD=15). The results of this extreme, stringent test showed zero failures on over 6500 total bumps tested.

The primary failure concern in TAB packaging is the inner lead bonding of the bumped circuit pads to the lead frame. The reliability testing, including extreme temperature ranges and a number of thermal shock cycles with zero failures, demonstrates the inherent quality of this Atmel process.

Features

- **Assembly and Screening to MIL-STD-883 Class B and Class S Levels**
- **Group A, B, C, D and E Testing**
- **Design Services for Multilayer Ceramic, Packages Including Multichip Modules**
- **Silver Glass and Eutectic Die Attach - Die Sizes to .600" Square**
- **10,000 Square Feet of Cleanroom Manufacturing Space**
- **Digital, Analog (including laser trimming), and Memory Testing Available**

Military Packaging Services

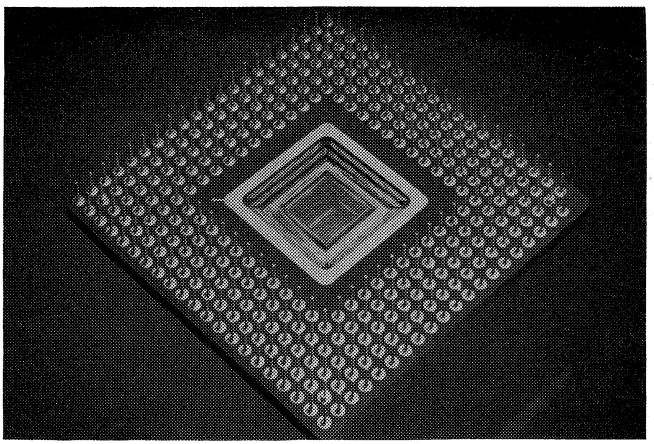
Description

Atmel offers package assembly and test on a MIL-STD-883 certified line. All manufacturing practices and procedures are based on MIL-M-38510, and are maintained and updated according to the latest revisions using that specification. The Company offers contract assembly, test and burn-in of die from any integrated circuit supplier. Other contract services range from test program development to custom package design to wafer preparation. In addition, the Company can saw not only silicon wafers, but also GaAs wafers, ceramics and other materials.

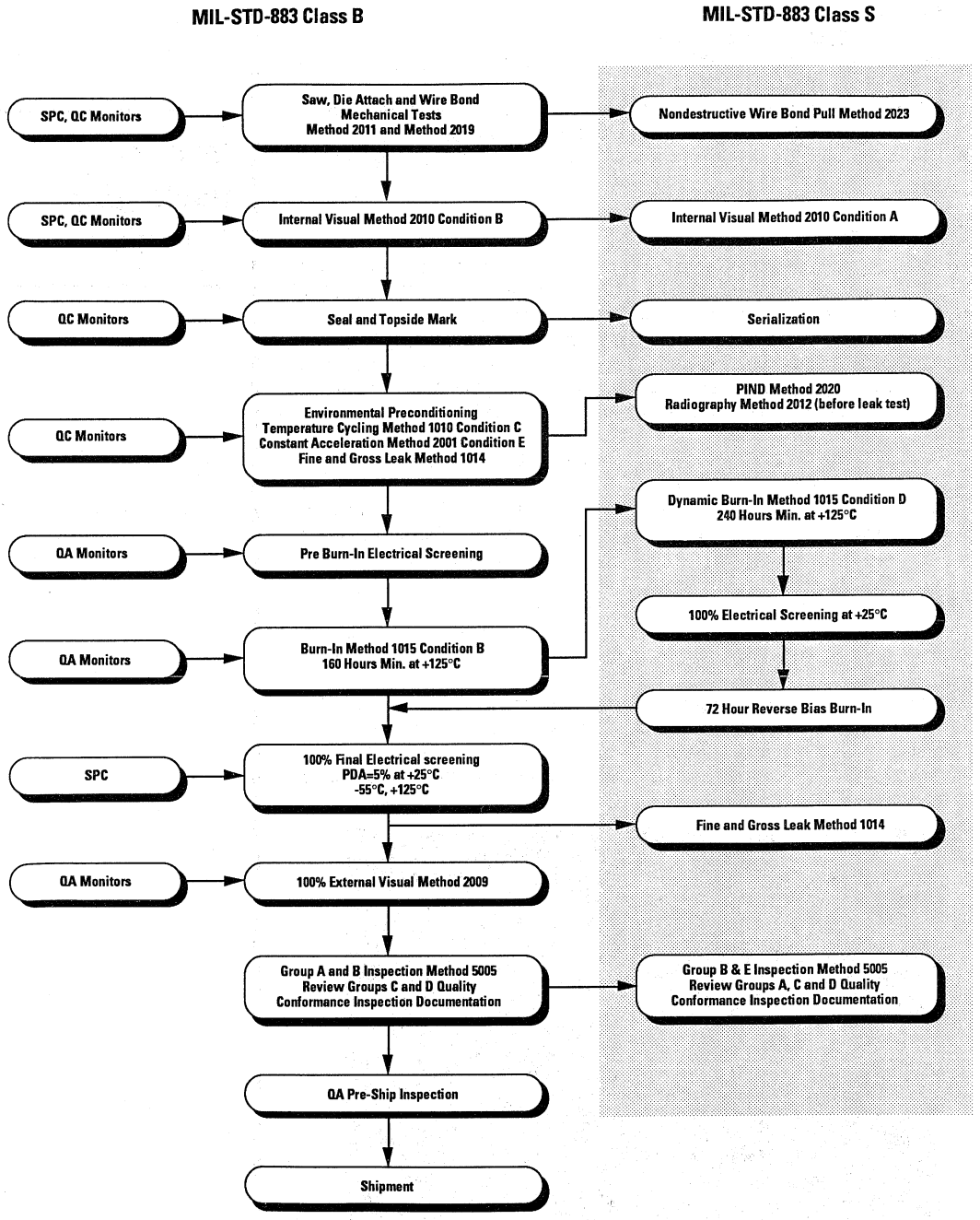
The Colorado Springs facility has production die attach capability using eutectic and silver glass epoxy. Wire bonding is available in either aluminum wedge or gold ball from one-mil to two-mil wire diameter. Tape automated bonding services can be provided, as well. Atmel's ceramic packaging is available in pin grid arrays, flat packs, leadless chip carriers, cerdips, side braze and custom designs.

The Company can provide MIL-STD-883 compliant Class B or S level assembly and screening. Atmel's in-house capability includes visual inspections, package seal, environmental preconditioning burn-in and Group A, B, C and D testing.

The packaging and assembly operation has a self-audit system following MIL-M-38510, Appendix A, which supports vendor and customer audits as well as continual auditing of production lines. Statistical Process Control (SPC) is implemented in the assembly and test areas to optimize quality and minimize variation.



Packaging Flow Chart



Maximizing Performance

When a standard, off-the-shelf package can't meet a customer's specific needs, Atmel can design a package to precisely fit the application. The Company develops a package design to optimize system performance for speed, size and power management using Auto CAD™ software.

Atmel's close working relationship with both domestic and foreign package suppliers insures first-pass design success. The Company has designed dozens of custom packages and successfully delivered production volumes, even to stringent Class S standards.

Thorough Testing

A broad range of test capability for both analog and digital products is available at Atmel. Devices can be screened to full military specification (-55°C to +125°C).

In addition, burn-in can be performed at temperatures up to 150°C with continuous output monitoring for products up to 512 pins.

Atmel's Ando™, Sentry™ and Teradyne™ testers are under Statistical Process Control with calibrations traceable to the National Institute of Standards and Technologies on all test manipulations. The Company can also develop a custom test program and tooling if required. If a proven functional simulation exists, Atmel can automatically generate a functional test program or convert an existing program using TDS™ software from TSSI™. This capability greatly reduces test development cycle time and cost.

In production, Atmel can perform full military final testing as well as QCI and CSI. In addition, handlers are available for high-volume DIP, LCC and PGA applications.

Test Capabilities

Tester	Max I/O Count	Max Speed	Features
Digital			
Ando 8034E	128	20 MHz	500 MHz Clock, 2 ns resolution
Ando 8034	256	20 MHz	500 MHz Clock, 2 ns resolution
Ando 8035	256	80 MHz	500 MHz Clock, 1 ns resolution
Ando 9035	256	100 MHz	500 MHz Clock, 100 ps resolution
Sentry 20	60	20 MHz	4K Memory
Sentry 20	120	20 MHz	4K Memory
Analog			
Teradyne A300	48	256 KHz Analog 10 MHz Digital	Mixed signal, laser trimming
Teradyne A360	48	256 KHz Analog 10 MHz Digital	Mixed signal, laser trimming
Sentry 80	48	256 KHz Analog 2 MHz Digital	Mixed signal, 2 meg memory
Memory			
Teradyne J386	28	40 MHz	16 timing edges, 1ns resolution, 256K cache RAM

Ando, Auto CAD, Sentry, TDS, TSSI and Teradyne may be registered trademarks of others.

Contents

Section 12

Application Notes

Using Atmel's CMOS E²PROMs

E²PROMs offer many features desired for present day memory systems. They are non-volatile, preserving data for years whether or not power is applied. They provide high density memory storage, with 1-megabit devices now available. They offer high speed reads and can be re-written on a byte or page basis.

5-volt only signals are used to operate the devices. When writing new data only the data bytes that are desired to be changed need be rewritten. No erasure steps are required before rewriting any memory location. Since all of Atmel's products are made with CMOS technology, the supply current required to operate Atmel E²PROMs is low. Other features such as $\overline{\text{DATA}}$ polling, internal error correction and software data protection, make Atmel E²PROMs the correct solution for many memory systems.

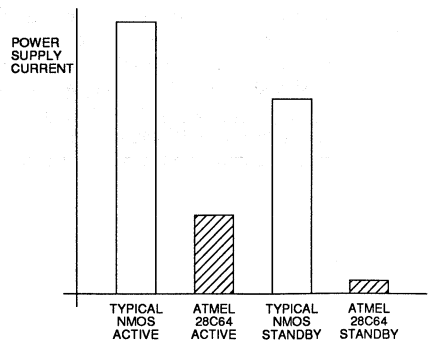
CMOS Versus NMOS E²PROMs

CMOS is quickly becoming the dominant MOS technology. Many systems however, have been designed without the use of CMOS products, and therefore do not have the benefits of this advanced process technology. The most obvious advantage of CMOS is in the power savings. Figure 1 shows a comparison of a typical 64K NMOS E²PROM current specification versus that of Atmel's AT28C64. The power advantage of CMOS is quite clear. The power savings actually does more than just reduce the drain on the power supply. The low power consumption helps to keep system temperatures lower, reducing the need for cooling and allowing for greater packing density on boards. With less internally generated heat, CMOS products can be more reliable than their NMOS counterparts.

The TTL and CMOS compatible inputs and outputs of Atmel's CMOS E²PROMs offer additional advantages. The input stages consume no active power when the input voltage is at ground or the positive supply level. Figure 2 shows the typical power consumption curve for an Atmel input stage versus input voltage. By using full CMOS input levels to the device, the active power consumption can be reduced below the specified levels.

The outputs of Atmel E²PROMs drive to the full limits of the supply voltage. When driving other CMOS input stages, this full swing drive capability can actually reduce the

Figure 1. Comparison of typical NMOS 64K E²PROM current consumption to that of Atmel's AT28C64.



power consumed by other devices within the system! Also, by driving to the high power supply limit, Atmel devices improve the noise margin of the high input level of the device they are driving as compared to typical NMOS devices which do not drive to the high supply level (see Figure 3).

Upgrading from NMOS to CMOS

It is generally quite easy to upgrade a system using NMOS devices to use CMOS parts. In most cases, NMOS E^2PROM devices organized from 512 by 8 to 32k by 8 may be directly replaced by an Atmel CMOS device of the same density and pinout. No hardware or software changes need necessarily be made when upgrading the system.

In some cases, power switching transistors have been used to power down NMOS E^2PROMs while the rest of the system remains active. In such a state, the DATA lines of the NMOS E^2PROM do not load the DATA bus of the system. A CMOS device in such a configuration may show substantial input current through the DATA pins if the DATA bus is higher than the E^2PROM's power supply input. To permit CMOS devices to work properly in such a system, it is recommended that the switching transistor be removed from the power supply of the E^2PROM. With the low power standby mode of Atmel'S E^2PROMs, the power switching is not necessary. The low power consumption of the CMOS device will not adversely affect the system power consumption and there will be negligible input leakage at the E^2PROM DATA pins. Additionally, the power consumption of the E^2PROM will be much lower when selected and, with the removal of the switching transistor, the number of devices in the system will be reduced.

Figure 2. Typical power consumption curve for Atmel input stage versus input level.

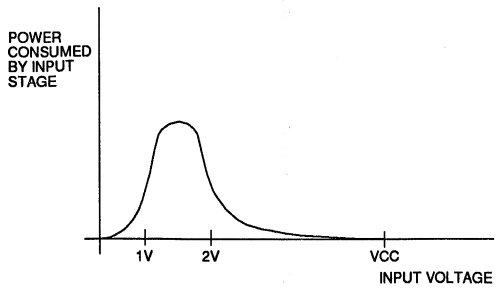
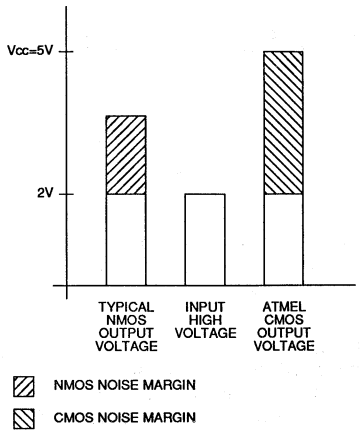


Figure 3. High input voltage noise margin comparison of typical NMOS output to Atmel CMOS output.



Read Cycle

The E^2PROM read cycle is controlled by the $\overline{CE}$ and $\overline{OE}$ signals. When $\overline{CE}$ and $\overline{OE}$ are both low, data is read from the device. The address inputs specify the memory location being read. The address and data lines are not latched during a read cycle; changing the address while $\overline{CE}$ and $\overline{OE}$ are low will result in the output of the device changing. If $\overline{CE}$ or $\overline{OE}$ is high, the outputs are put in a high impedance state. This dual line control allows for flexibility in avoiding buss line contention. There is no need for periodic refresh of the memory; E^2PROMs retain their data whether or not power is applied. Addresses may be randomly selected; there are no restrictions on address lines.

When $\overline{CE}$ is high, the internal power consumption of the device is greatly reduced; the device is said to be in the standby mode. The power reduction is achieved by turning off the internal circuits of the device. When $\overline{CE}$ is returned low, the internal circuits are again powered on and a new read is performed.

Atmel E^2PROMs are designed to provide the fastest access times available among like devices. They therefore may have large transient current requirements. It is recommended that each device be carefully decoupled. A decoupling capacitor across the power and ground line as close to the device as possible should be used. As with any high performance device, the integrity of the power and input signals can affect its operation in the system. Maintaining clean power and input signals will ensure the best performance of the device.

Byte Write Cycle

Writing to Atmel E²PROMs has been designed to minimize the time that the system must spend in issuing commands to the memory device. The write cycle is controlled by $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$. Initiating a write cycle is done with a short pulse on either the $\overline{WE}$ or $\overline{CE}$ input. With $\overline{OE}$ high and $\overline{CE}$ (or $\overline{WE}$) low, the address to be written is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred last). The data to be written is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred first). The latching of the address and data inputs allows the address and data busses to be used to access other devices while the write is in progress. During its write cycle, data may not be read from the E²PROM (the device may however be polled to see if the write is completed).

Internal to the E²PROM device, the write cycle can be divided into two steps. The first is to load the data into a temporary buffer; this operation can be done very quickly (measured in nanoseconds). The second step is to perform the nonvolatile storage. It takes considerably longer for this step (up to several milliseconds). After the nonvolatile storage is completed, a new read or write cycle may begin immediately.

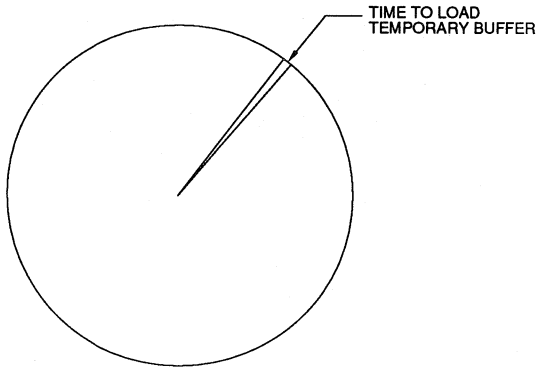
Page Write Cycle

To improve the effective write time when large sections of the memory are being rewritten, some Atmel E²PROMs provide a page write operation. The page write allows a group of bytes to be quickly loaded into the device's temporary buffer and then simultaneously written to the nonvolatile storage elements. Figure 4 is a pie chart showing the time needed for completely loading the temporary 64 byte page buffer of the AT28C256 as a portion of the write cycle time. Clearly, by utilizing the page write with minimum write load times, the write time can effectively be reduced by a factor approximately equal to the page width.

Similar to the writing of a single byte, address location and data to be written are latched on the falling and rising edges of $\overline{WE}$ or $\overline{CE}$. All bytes being written must have the same page address. The page address is determined by the higher order addresses and is specified in the data sheet of each particular device. The page address must be valid during each high to low transition of $\overline{WE}$ or $\overline{CE}$. The $\overline{OE}$ input must be high whenever $\overline{CE}$ and $\overline{WE}$ are low.

During write cycles, only the bytes that are specified to be written are altered; other bytes within the device are not rewritten or otherwise affected. A write cycle will only occur when requested; however, there may be conditions present during such times as power-up or power-down when a system might inadvertently initiate a write cycle. Atmel devices include many features to help prevent inadvertent write cycles. Users of E²PROMs should become familiar with these features.

Figure 4. Time to load 64 bytes to temporary buffer in AT28C256 as a portion of the write cycle time.



Additional Features

Atmel E²PROMs include other features to help ensure reliability and to improve overall system performance. The internal error correction incorporated into Atmel's E²PROMs protects against single bit data errors from appearing in the devices. The user does nothing to utilize the feature; whenever a write or read cycle is performed, parity generation or checking occurs internally to the E²PROM device to help ensure the integrity of the data.

The inputs and outputs of Atmel devices contain circuitry to protect the device from electrostatic damage. Even though the devices do have this protection circuitry, it is strongly recommended that safe handling procedures be used with these devices. All equipment and personnel that may come in contact with the devices should be well grounded. Other features such as $\overline{DATA}$ polling, READY/$\overline{BUSY}$ outputs or toggle bit are available and may be employed by users as required by their particular application.

E²PROM Data Protection

Advantages of E²PROMs

E²PROMs provide the memory solution wherever reprogrammable, nonvolatile memory is required. They are easy to use, requiring little or no support hardware such as refresh clocks or batteries. Each memory location can be selectively changed without impact on any other location; blanket erasure and rewriting of the entire device or a large section of it is not required.

E²PROMs made at Atmel were designed to provide the best features available. Atmel E²PROMs provide high speed read access times so that many applications can use them without inserting costly wait states. The page mode write operation of Atmel E²PROMs allows for the fastest effective write time available in E²PROM memories. Since all of Atmel's devices are made in CMOS, they offer the benefits of low operating and standby power.

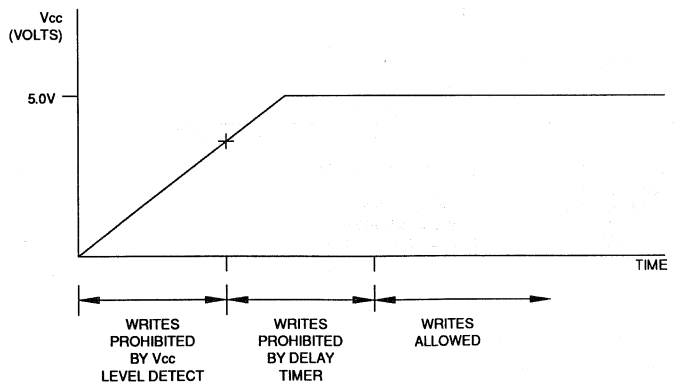
In order to take advantage of all of the benefits of Atmel E²PROMs, care must be taken to maintain the integrity of the data. While an E²PROM will retain its data for many years with or without power applied, improper operation of the device could result in data being inadvertently rewritten.

When is Data Susceptible to Corruption

In the use of any memory device, it is expected that the data stored in it is available as it is written. This is especially true of E²PROMs since their code often controls the operation of the system in which they are contained. Unlike most other memory types that are rewritten in systems, E²PROMs are often expected to retain their data for a period of many years, with or without power applied and during power transitions. For these reasons, added attention is given to avoid corrupting data in E²PROMs.

There are a number of situations in which data is particularly prone to corruption. These situations include powering on and off of the devices, noise spikes on the control lines and system glitches. Atmel E²PROMs include features to help protect against each of these potential sources of inadvertent writes. Atmel data protection features are broken down into two different types: hardware data protection features and software data protection features.

Figure 1.



CMOS E²PROM

Application Note

Atmel Hardware Data Protection Features

Atmel E^2PROMs include four different types of hardware data protection. These features provide protection against most inadvertent writes that might occur in a system. Atmel hardware data protection features include: three line write control, power level sense detector, power on delay timer and noise filters on $\overline{CE}$ and $\overline{WE}$.

Three Line Write Control: In order to write a device the $\overline{OE}$ signal must be high with the $\overline{CE}$ and $\overline{WE}$ signals low. Holding any of the three lines in the opposite state will prohibit a write cycle. For example, whenever the $\overline{OE}$ signal is low, a write to the device cannot be started.

Power Level Sense Detector: An active circuit in Atmel E^2PROMs monitors the level of the supply voltage to the device. If the supply is below 3.8 volts, typical, write cycles to the devices can not be activated.

Power On Delay Timer: As power is applied to Atmel E^2PROMs, the power level sense detector will issue an internal signal that indicates that the supply is above the sense level. At this time an internal timer is initiated that times out in typically 5 ms. During this time period, writes to the device cannot be performed. This delay period serves two purposes. First, it allows the supply level additional time to rise to within the standard operating region before writes are permitted. Secondly, it lets the system stabilize and present the correct levels to the control pins of the E^2PROM so that the E^2PROM doesn't react to its inputs before they are actually valid. Figure 1 shows the combined action of the power supply level detector and the delay timer upon writes to the device.

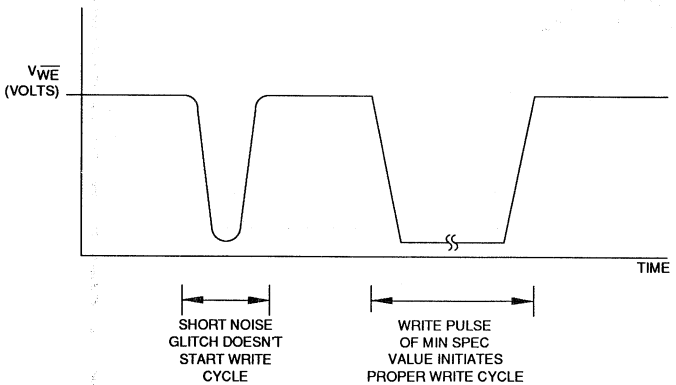
Noise Filters on $\overline{WE}$ and $\overline{CE}$: If brief noise pulses below V_{IH} occur on the $\overline{WE}$ or $\overline{CE}$ inputs to the device, a write cycle will not be initiated. Internal to the E^2PROM, a noise filter does not allow the short pulses to activate a write cycle. As shown in Figure 2, write pulses of sufficient length will still initiate writes but short noise spikes on the $\overline{WE}$ or $\overline{CE}$ control lines will not.

Atmel Software Data Protection Feature

Available on some Atmel E^2PROMs is a user selectable feature that requires a software sequence at the beginning of each write cycle in order for a write to be performed. To enable the software data protection feature, a series of three write commands to specific addresses with specific data must be performed. Once set, the same three byte code must begin each write request. (A separate write cycle to enable the software feature is not necessary; after any write that is preceded with the three byte code, the software data protection function will be enabled, see Figure 3.) The feature may be disabled by issuing a six byte code to the device as shown in Figure 4. After being set, the software data protection feature remains active until its disable command is issued. Power transitions will not reset the software data protection feature, but the feature will prevent against inadvertent writes during power transitions.

The software data protection feature protects data against various causes of inadvertent writes. Since it is active during power transitions it protects data when powering on or off the device. Noise spikes that occur on the control lines will be ignored since they will not show the correct address and data needed to start a write cycle. Even for system malfunctions, such as when write pulses of adequate length are given to the device, the software feature can prevent the corruption of the data in the E^2PROM. The address locations used for the software code are not sacrificed from the usable memory array. The device recognizes the software code and does not alter the data stored at the address locations of the code. Byte locations of code are still usable, and don't have to be rewritten.

Figure 2.



System Design Considerations

Designing systems with data integrity in mind can greatly reduce the chance of lost data. The amount of attention needed depends upon the nature of the design. Following are a few areas that might need special attention in certain designs.

External Power On Protection

Many systems will have a PON (power on) signal to control the operation of the system. Such a signal can be gated with the logic creating the $\overline{OE}$ signal to the E²PROM, holding $\overline{OE}$ low when the PON signal is false. Similarly, a PON type signal could be gated with the $\overline{WE}$ or $\overline{CE}$ logic, forcing $\overline{WE}$ or $\overline{CE}$ high when writes should not be allowed.

If the system does not include a PON type signal, one can be created from various programmable voltage reference devices. With such a device, the user can select the voltage supply level below which the device cannot be written. It should be noted that in many systems, using Atmel's E²PROMS with their internal power level detection and power delay timer, no additional power on circuitry is required for the device.

Multiple Power Supplies

In systems that utilize more than one power supply, extra care must be taken during power transitions to both the E²PROM and the devices controlling the inputs to the E²PROM. Power on rates of the different supplies are likely to vary. Using programmable voltage reference devices to detect the power level of both supplies and forcing the $\overline{OE}$ pin low when either line is below the desired level may be used in such situations to avoid inadvertent writes.

Memory Cards

Since memory cards are often pushed into and pulled out of systems that are already powered on, they have additional chances of inadvertent writes. If the edge connector is arranged such that power and control lines are not asserted in a prescribed manner, false writes to the device may occasionally occur depending upon how the card is inserted. To provide proper power on sequencing, a card could be designed with its control pins recessed from the edge of the card. Resistors would be placed on the card to connect $\overline{CE}$ and $\overline{WE}$ to V_{CC} and $\overline{OE}$ to ground. This arrangement insures that power is first applied to the device and that the control pins are not in the write state until each pin is being controlled by the host system. Variations of this technique may be used effectively in different systems; the basic idea is to guarantee systematic application of the power and control pins such that a write state is not entered upon insertion or removal of the card from the host.

Figure 3.

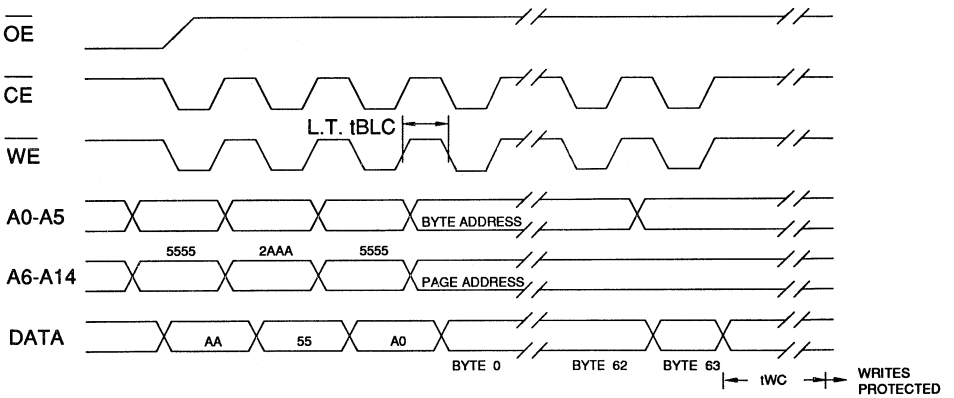
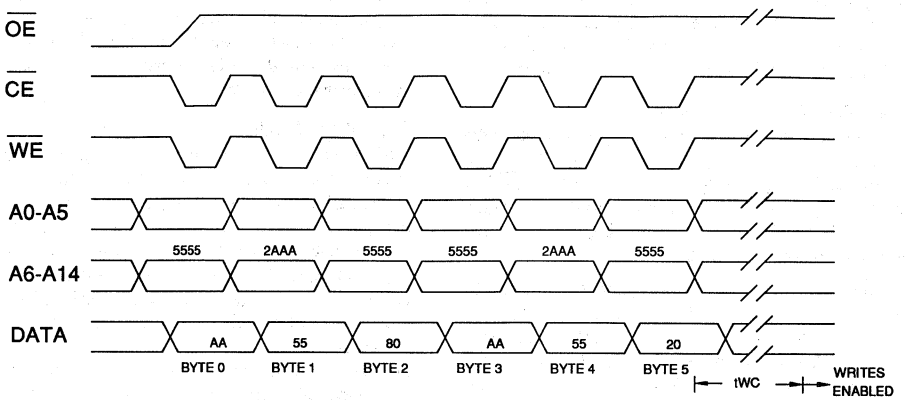


Figure 4.


OE
CE
WE
A0-A5
A6-A14
5555
2AAA
5555
5555
2AAA
5555
DATA
AA
55
80
AA
55
20
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
tWC
WRITES ENABLED

Programming Socket Adapter

As the market for nonvolatile memory parts in surface mount packages increases, so does the interest in simple, low cost programming socket adapters. These adapters allow users of standard programming equipment to program any package type including LCC (leadless), SOIC (Gull-wing), PLCC (J-Lead), and flat-pack. The adapter plugs into the programmer in place of a 600 mil or 300 mil DIP package of the same part. The surface mount part to be programmed then plugs into the socket on the adapter.

The two major disadvantages of building a socket adapter are:

- Little or no support from programmer manufacturers.
- Prolonged use of socket adapters using wire-wrap pins is not recommended due to spring tension loss damage of the programmer's zero insertion force sockets. That may degrade the reliability of the programmer when the adapter is not used.

The advantages are more obvious. Some manufacturers charge up to $500 for an adapter which slides or plugs into the programmer compared to about $100 for the hardware described here.

Assembly of a custom programming adapter is very simple. Table 1 describes the typical piece parts needed. Table 2 lists sockets and piece-part sources for different package configurations. The finished adapter is about 2 inches square and 1.5 inches high.

As listed in Table 2, Emulation Technology, Inc., (408) 982-0660, can supply the adapter sockets preassembled, but we recommend you order the parts as an UNSOLDERED KIT to facilitate attaching the decoupling capacitors. The additional wire shunts (not re-

Table 1. Piece-Part Descriptions (see Figure 1)

Item No.	Qty.	Description
(1)	1	Zero insertion force socket.
(2)	2	Wire wrap strips with 100 mils pin centers and about 500 mils long on the end which will plug into the programmer's socket and 200 mils long on the opposite end to attach to (5) below.
(3)	2	Wire wrap strips similar to (2) above except only 100 mils and 200 mils long to connect (4) and (5) below.
(4)	1	PC board to accept the socket (1) and run traces to the edge of the card connecting to (3).
(5)	1	PC board to run traces from the card edge (3) to the two strips (2) (usually separated by 600 mils).
(6)	20"	#16-18 insulated stranded copper wire.
(7)	1-2	0.1µF ceramic high-frequency decoupling capacitors.
(8)	1	(Recommended) Pin socket board to fit between (1) and (4) to allow easy replacement of the socket (1). (8) is soldered to (4) and (1) plugs into (8). Zero insertion force sockets wear out quickly so replaceability is a good feature to have.

quired if a -LN kit is ordered from ET) and capacitors are essential to reduce inductive noise effects during programming and to maintain adequate programming yield. It is necessary to "beef-up" all the power (V_{CC}, V_{PP}) and ground (Gnd) connections by adding short jumpers of wire (6) running from the socket (1), around the edge of the module and finally to the pins of item (2) on the bottom of the module. Bypass capacitors (7) must be soldered between Gnd and V_{CC} or V_{PP} (if applicable). The leads on the capacitors must be trimmed as short as possible and soldered as close to the socket (1) as possible (on the wide traces on the -LN board (4)). The other end of each capacitor will be connected to short stranded wires (6) running from the top, around the edge of the adapter, and finally soldered to the ground pin of item (2).

Assembly proceeds as follows (see Figure 1 and note that jumper wires (6) are not required if a -LN kit is used):

1) Trim the leads on the jumper wires (6) to about 3.0 inches. Solder capacitors (7) with shrink-wrap insulation on the cap leads, and jumper wires (6) under the socket (1) (or under (8) if socket replaceability is needed) in such a way that they do not interfere with attaching the socket (or (8)) to the board (4). (If a -LN kit is used, just solder the capacitors on the wide traces provided on board (4).)
2) Solder the socket (or item (8)) to the PC board (4) and trim the pins on the socket flush to the board (4).
3) Solder the shorter pin strips (3) to the outside of board (4) with the spacers on the side away from the socket (1).
4) Solder the longer pin strips (2) into the other PC board (5) such that the spacers stick out of the bottom of the adapter. These longer pins will be used to plug directly into the programmer socket. Trim the shorter leads of (2) flush with the board (5) after soldering.
5) Solder the PC board (5) to the short pins protruding below PC board (4).
6) (Omit this step if a -LN kit is used.) Connect all the V_{CC}, V_{PP} (if applicable) and Gnd wires which were connected in step (1) to their appropriate pins on item (2) on the underside of the assembly close to the protruding spacer in such a way that they will not interfere with plugging the completed module into the programmer DIP socket. Trim these shunt wires as short as possible to minimize inductance effects.

This application note has described how to build a simple and cheap programming adapter socket to support a wide variety of nonvolatile memory product packages available from Atmel.

Figure 1.

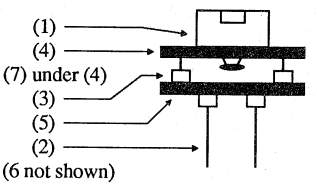


Table 2. Vendors / Part Numbers By Package Type

Package Type	Pin Count	Emulation Technology[1]	Socket Manufacturer	Part No.
LCC	28	AS-28-28-01-L6-LN	Textool[2,3]	228-4960
	32	AS-32-28-01-P6-LN	Yamaichi	IC51-0324-453
	32 (27C010)	AG-32-32-01-L6-LOW	Textool	232-5427
	44	AS-44-40-08-L6-LN	Textool	244-5292
	32 (27C010)	AG-32-32-01-P6-LOW	Textool	232-6917
PLCC	32	AS-32-28-01P-P6-LN	Yamaichi	IC51-0324-453
	44	AS-44-40-08-P6-LN	Textool	244-5292
JLCC	32	AS-32-28-01-K6-YAM	Yamaichi	IC5I-453-K510011
	32 (27C010)	AS-32-32-01-K6-YAM	Yamaichi	IC5I-453-K510011
	44	AS-44-40-08-P6-LN	Textool	244-5292
SOIC	28	AS-28-28-015-6-GANG	Enplas	FB-28-1-27-07
	28	Call Atmel	Yamaichi	IC51-937-K510369

Notes: 1. ET can also supply finished adapter sockets built per this application note or other customer requirements.
2. Made by 3M. Check with your local distributor.
3. Windowed LCC packages (i.e., EPROMs) require removal of the circular bumper in the Textool socket lid which snaps apart. Non-windowed packages (i.e., E^2PROMs, OTPs) do not require any socket adjustment.

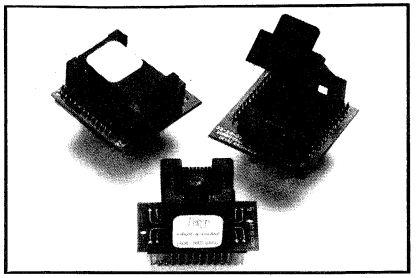
Figure 2.

LCC / PLCC / SOIC to DIP Adapter

ADAPT-A-SOCKET®

LCC / PLCC / SOIC to DIP

Prices from $67.00 to $148.00



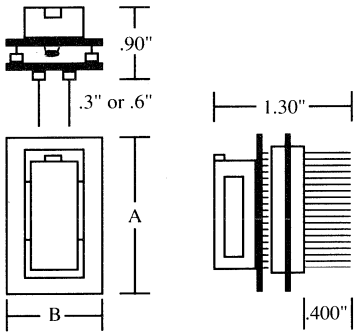
- For programming PROMS, PLDS, EPROMS, EEPROMS, PALS†
- Production ATE testing
- Test points provided for each signal
- Decoupling capacitors can be added.
- Available for LCC, PLCC and SOIC.
- Natural for prototype processing.
- Sturdy base contact pins.
- Saves development $$$.

† PAL is a registered trademark of Monolithic Memories, Inc.

When Your Equipment is Designed for DIPs

ADAPT-A-SOCKET converts your Dual-In-Line (DIP) sockets to ceramic Leadless Chip Carrier (LCC), Plastic Leaded Chip Carrier (PLCC) and Small Outline Integrated Circuits (SOIC) sockets in just seconds. Without having to purchase expensive equipment. Just plug ADAPT-A-SOCKET into your programmer socket, burn-in board or test head and you're ready to go.

Call Factory for *Cross Reference Guide*



Number of Top Pins	A	B
16	1.60 Max	1.45
20	"	"
24	"	"
28	"	"
32	1.65	1.60
32 AG*	1.70	.90
52	2.70	1.80

* AG-32-28-01P-6 is available for gang programmers

Specifications

- **SOCKET** (LCC, PLCC, SOIC, FLAT PACK)
  Body Material ..... Ryton
  Contact Material ..... BeCu
  Contact Plating ..... 30 Microinches of Gold over Nickel
- **PHYSICAL**
  Lids and latches are replaceable.
- **BASE** (DIP, PGA, LCC, PLCC)
  Body Material FR4
  Contact Material ..... BeCU
  Contact Plating ..... 30 Microinches of Gold over Nickel
- **ELECTRICAL**
  Contact Resistance ..... 25 MilliOHMs per Contact MAX.
  Insulation Resistance ..... 20 MegOHMs MIN. @50 VDC
  Capacitance ..... 2.0 Pico-Farads between any pair of isolated contacts
- **TEMPERATURE RATING** ..... -55°C to +125°C

Test Point Specifications

Insulator Material ..... Glass-filled nylon black, UL94V-0
Contact Material ..... Phosphor Bronze
Current Rating ..... 1 Amp
Voltage Rating ..... 300 VRMS
Dielectric Withstanding Voltage ..... 500 VRMS
Insulation Resistance ..... >1,000 MegOHMs
Temperature Rating ..... -55°C to 125°C

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FAX: (408) 982-0664 TLX: 981 866

EPROM Programming with V_{CC} = 5 Volts

UV Erasable CMOS EPROM

Application Note

Present day EPROMs use V_{CC} = 6-6.25 V during programming. This non-5-volt supply level occasionally presents a system design problem with applications where a commercially available programmer cannot be used. This application note will briefly address the issues associated with using a 5-volt V_{CC} supply during programming.

Modern EPROM programming algorithms can be divided into two sections namely, programming and verify (or read). The programming algorithm usually proceeds by selecting the desired voltage levels and address. A programming pulse is applied followed by a verify at the elevated V_{CC} used for programming.

During programming, the MOS threshold voltage (Vt) of a previously erased N-channel floating gate EPROM cell (Vt = 1.0-2.0 V) is raised to 6.5-9.0 V via the accumulation of electrons on the floating gate by hot electron injection. In normal read mode operation the address decoding circuitry in the chip selects the desired cell by pulling the gate voltage of the cell to V_{CC}. Since V_{CC} is typically 4.5-5.5 V, an erased cell with Vt = 1.5 V would be turned on while a programmed cell with Vt = 7.5 V would remain in an off state. If V_{CC} were raised above the threshold voltage for the programmed cell (i.e. V_{CC} > 7.5 V), the cell would begin to conduct and the programmed data would no longer be valid until V_{CC} was again lowered.

The V_{CC} voltage that causes data loss on a programmed EPROM is called the programming margin. During the programming algorithm the V_{CC} level is held at 6-6.25 V to make sure that each cell is guaranteed to have a programming margin at least to that level. This is verified by reading each byte twice, once during the initial programming section and again during a final read where all addresses are compared to the desired data.

The 0.5-V difference between the guaranteed programming margin and the 5.5-V V_{CC} maximum supply rating provides a reliability guardband for long term data charge retention and, more importantly, for system noise immunity. Poor programming margin can lead to EPROM memory chip instability which can cause apparently slower operation due to oscillations and false reading. This in turn makes the problem directly related to the specific system noise environment and will vary from application to application.

By lowering the V_{CC} voltage to 5.0 V during the programming algorithm two effects may occur. First, the part may not be able to program (i.e. programmed cell threshold = 5.0 V). Second, the part may not have enough programming margin to reliably work over worst case conditions over the lifetime of the part.

The first problem is rare since most manufacturers design their EPROM technology to provide a large programming margin guardband to account for statistical variations in the manufacturing process.

The second problem is also considerably reduced by the same margin guardband, but unlike the first problem which is easily detectable at the time of programming, the second problem may only occur later when the parts are in the field. The resulting field failure rate may still be acceptably small depending on the application.

The second problem may also result in a failure mode even when the nominal V_{CC} programming voltage is used. In that case standard accelerated reliability tests and statistical sampling techniques can be used to determine failure rates. But such test results only apply to parts with the same programming technique. Since those tests require great expenditure of labor, time, and units, significant reliability data for V_{CC} = 5 V programming is not readily available. Another way to get around the possible reliability problem is testing the parts in such a way so as to screen out any low margin parts. This specially tested group will

then have the same programming margin as parts programmed at the nominal V_{CC} even when they are programmed using $V_{CC} = 5$ V.

We have discussed general EPROM operation for most currently available EPROM chips on the market today including Atmel's EPROM line. Atmel's chips specifically do not have any programming problem "of the first kind" with $V_{CC} = 5$ V. This is due to the proprietary programming circuits used in Atmel EPROMs. That same programming circuitry also makes an Atmel EPROM quite insensitive (compared to other EPROM suppliers) to the level of V_{PP} voltage used during programming. However, just as with other EPROM suppliers, Atmel can guarantee the same product reliability for $V_{CC} = 5$ V programming as with nominal V_{CC} programming only if parts are specially tested.

New EPROMs Speed Programming

Introduction

In designing and manufacturing certain modern-day products, the methods used to build these products are often as important to the design engineer as the components themselves. This is true about programmable memory devices as well, especially EPROMs. Since many vendors use their own unique programming algorithm, which is based on the process used to make EPROMs, the design engineer needs to know about the algorithm during the system cycle to insure that the EPROMs can ultimately be programmed.

This application note will introduce the Atmel RAPID programming algorithm and briefly explain why this algorithm is superior to others. In addition, it will give an introduction to EPROM technology and the mechanics of programming. These should provide a basic understanding in the growing field of EPROMs.

Programming EPROM the RAPID Way

When Atmel reduced the geometry of some of its EPROM products recently from 1.5- to 1.2-μ linewidth, the Company adopted an entirely new programming algorithm for these devices. A reason for this algorithm change was to improve programming yields and lengthen long-term data retention. This was accomplished by using a shorter programming-pulse length during programming. The new RAPID algorithm reduces the 1-ms programming pulse width of the original FAST algorithm to only 100 μs, and it completely eliminates extra overprogramming pulses.

But higher yields and increased reliability aren't the only benefits the RAPID algorithm provides, it also takes less time to program these new devices. The RAPID algorithm can reduce the programming overhead costs by a factor of 40! Here's how it works:

If you program an AT27C512R, 512-K EPROM in a single-device programmer, using the FAST or any other type of 1-ms algorithm (1-ms initial pulse, plus 3-ms overprogramming pulse) the time spent programming will be:

524288 bits ÷ 8 bits/byte = 65536 bytes

65536 bytes x .004 seconds/byte = 262 seconds

Figure 1. Cross section of a typical EPROM cell.

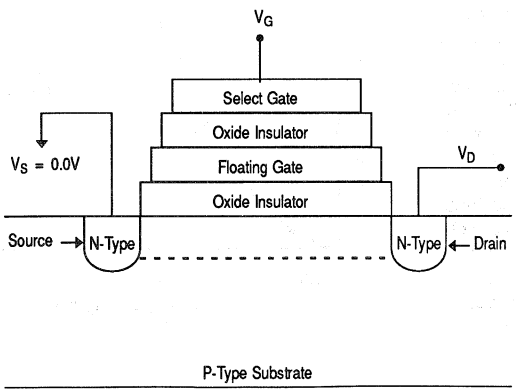
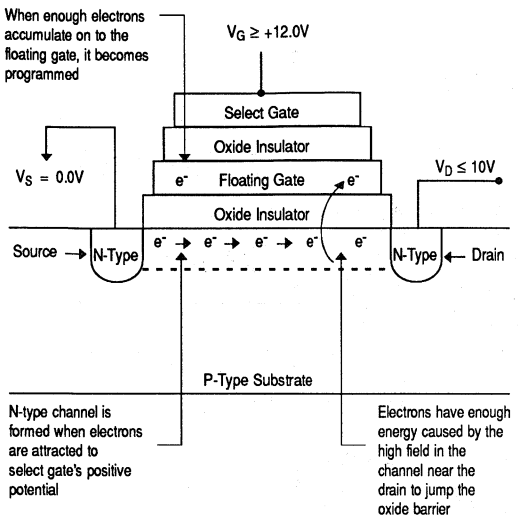


Figure 2. Process of hot-electron injection.



That's 262 seconds, or 4 minutes and 23 seconds. This works out to about a $0.75 programming cost, assuming an operator's rate of $10 per hour. Here's where the cost savings start: Since we cannot reduce the number of bits to program, we reduce the total programming time by shortening the programming pulse width. Using 100 µs per byte, this is what happens:

65536 bytes x .0001 seconds/byte = 6.5 seconds

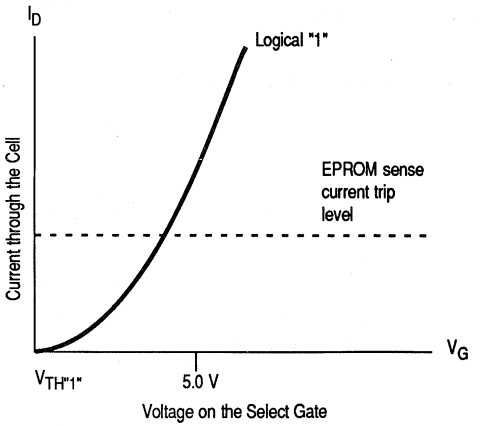
This amount of programming-time savings is what can be expected when using the RAPID algorithm. The big improvement is from reducing the total byte-programming time from 4 ms to 100 µs. With this example, total programming cost is about 3 cents. The RAPID algorithm can actually save up to $.72 per device. Imagine how much can be saved with 10,000 EPROMs!

There's more to the RAPID algorithm than shorter programming times and cost savings. It has a special way of checking that each cell is correctly programmed, and that cells are programmed with the required amount of charge. In fact, the RAPID algorithm even guarantees that the EPROM is correctly programmed. Programming algorithms of the FAST type, or their relatives, the QUICK-PULSE types, check each memory location for the programmed data immediately after programming that location. This check, which takes place before the final verify at the end of the programming cycle, is basically an "insurance" check, because it is performed at an elevated voltage, which is a worst-case condition. There is a flaw, however, in this type of programming algorithm: Memory locations that have been previously programmed can be partially erased by programming subsequent locations (due to the elevated voltage on the same row or column in the memory array) and marginally programmed cells will go virtually undetected. The question is, doesn't the programmer check each device during verify after programming? Wouldn't those failures be caught then? Not necessarily, because when parts are checked during the program verify mode, the voltage is not elevated as high as it was during programming.

The RAPID programming algorithm was designed to fix this oversight. First, it goes through the entire device and programs every cell without checking. Then it goes back to the beginning of the memory array and verifies the data in each cell at the elevated voltage. Once the device passes, another final verification is done at 5 V. The RAPID algorithm will do a better job at preventing any marginally programmed parts from passing the programmer than other algorithms.

An important fringe benefit of the RAPID algorithm, because of the way it guarantees successful programmability, is long-term data retention. Basically, long-term data retention is how long the EPROM stays programmed, which is typically greater than ten years. Although long-term data retention is not the same as device programmability, they are related in this way: programmability tells how well the electrons have accumulated on the EPROM's floating gate, long-term data retention tells how long the electrons will stay there. The programming algorithm has an overwhelming influence on programmability, making it an overwhelming influence on long-term data retention as well. Therefore, a poor programming algorithm, one that doesn't guarantee programmability, can be responsible for poor long-term data retention. The RAPID algorithm can add years of data retention to your parts, because of the way it checks for programmability. Marginally programmed parts just don't stand a chance of getting past the programmer.

Figure 3. Unprogrammed cell.



EPROM Programming, How it Works

Contemporary EPROM programming algorithms can be divided into two main sections, programming and verifying (or reading). Programming begins by selecting the desired voltage levels and byte address. It continues with a programming pulse applied to that byte, followed by a verify at the elevated V_{CC} used for programming. Verifying checks the data in two passes with the original data, with V_{CC} set to 5.5 V on the first pass, and 4.5 V on the second.

Basically, EPROMs are programmed through the accumulation of electrons on the floating gate of an N-Channel EPROM cell (see figure 1) by the process of hot-electron injection. Hot-electron injection is where electrons, flowing as a current between the drain and source of a saturated EPROM cell, gain enough energy from the high electric field to jump the oxide barrier between the channel and the floating gate (see figure 2). Before programming, the MOS threshold voltage, V_{TH} (otherwise known as the gate threshold voltage) of the erased floating-gate EPROM cell is about 1.0 to 2.0 V (see figure 3). After programming, its threshold voltage is about 6.5 to 9.0 V, due to the accumulated electrons on the floating gate. In read mode, the address decoding circuitry in the chip selects the desired cell by pulling the gate voltage of the cell to V_{CC}. Since V_{CC} is typically 4.5 to 5.5 V, an erased cell with a V_{TH}=1.5 V would be turned on (figure 3), while a programmed cell with a V_{TH} = 7.5 V would remain off (see figure 4). This floating-gate process is how a single MOSFET-like transistor can provide for the two logic levels used in digital circuitry.

If V_{CC} is gradually raised in voltage to a point near the threshold voltage of a programmed EPROM cell, the cell would just begin to conduct, and would no longer appear to be programmed. This point, where the programmed EPROM cell begins to look unprogrammed, is defined as the programming margin (see figure 5). The value of the programming margin

Figure 4. Programmed cell. Note how V_{TH} raises after electrons are accumulated on the EPROM floating gate from programming.

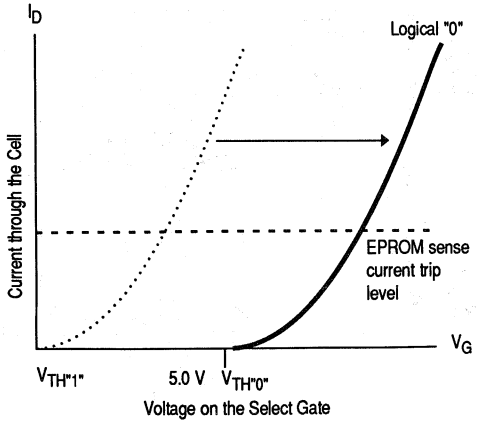
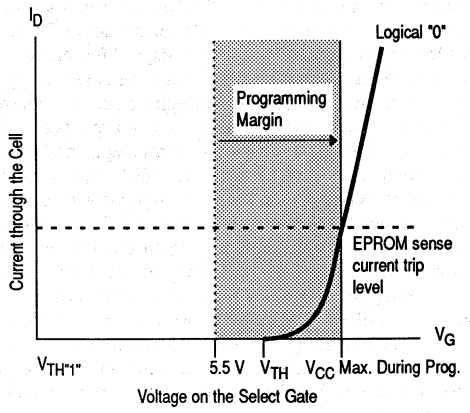


Figure 5. Programming margin. To find programming margin, increase gate voltage (V_{CC}) until the first "0" turns into a "1."



can, in some cases, be simply equal to the value of the V_{CC} voltage present during programming. This is why the RAPID algorithm holds the value of V_{CC} constant at 6.5 V during programming; to insure that each EPROM cell has a programming margin of at least that voltage. This margin is verified by reading each byte twice, once during the initial programming operation and again during the final read (or verify) operation, where the data from the EPROM is compared to the desired data. The difference between the value of V_{CC} during programming (the guaranteed programming margin) and the 5.5-V V_{CC} maximum supply rating (from the data sheet) serves as a reliability guardband for long-term data retention and, more importantly, for system noise immunity. Poor programming margin can reduce system noise immunity and lead to EPROM chip instability due to power-supply noise on the V_{CC} pin. This instability can cause oscillations and read-mode data glitching that can be a problem in even in the slowest and most noiseless of systems. Since power-supply noise is a somewhat random occurrence, data errors can happen non-reproducibly, which can undermine the reliability and integrity of the host system. These problems can be avoided by using the programming algorithm recommended by the EPROM chip vendor. The higher the guaranteed programming margin, the less likely any problems will occur.

Another important benefit of high-programming margin is that it extends the long-term data retention of the device. If the 6.0-V programming margin (FAST algorithm) on the EPROM gradually diminishes to 5.5 V over a 10-year time span, the randomly occurring noise spikes on the V_{CC} line can cause the EPROM to yield faulty data. On the other hand, given the same discharge rate (as a function of the silicon processing), an EPROM with a programming margin of 6.5 V (RAPID algorithm) would take over 20 years to reach the 5.5-V threshold that would lead to faulty data yield. All things being equal, better programming margin leads to longer data retention.

Guaranteeing Programmability

Most people might ask, "What's in a programming algorithm? Aren't they all the same?" That question would have been answered with a resounding "YES" 10 years ago when, quite frankly, they were the same. But it's not true today. There are over 35 manufacturers making EPROMs, and few of them use the same programming algorithm. Today, the programming algorithm is as important to EPROM testing as the actual device testing procedure. In fact, the device test procedures are often (if not always) based upon the programming algorithm. The programming algorithm has a direct effect on EPROM test yield, and manufacturers select their programming algorithms so they can obtain the highest yield possible. Additionally, the programming algorithm is directly responsible for the number of devices that pass the customers programmer, which is called programming yield. This is of vital importance to an EPROM manufacturer like Atmel, since the worst place for an EPROM to fail programming is in the customer's programmer. With this in mind, let's look at how the RAPID algorithm can guarantee better programmability than a common type of quick-pulsing algorithm.

We'll begin by comparing a common type of quick-pulsing algorithm with the Atmel RAPID algorithm. Examine figure 6, which is the flowchart for the QUICK-PULSE type of algorithm. If you look very closely you will see that the algorithm is broken up in to two major sections. The main part is the program/verify section, the other part is the final verify section. Basically, the first section starts at byte address 0000H, programs the eight EPROM cells at that address, and verifies that those cells contain the correct data with a verify at 6.25 V on V_{CC}. If the byte passes, it goes on to the next byte. If it fails, it repeats everything up to 25 times before it fails the device. The second section lowers the V_{CC} voltage to 5.0 V and checks if all address locations read with the correct data. Although the flowchart specifies a one-pass final verify at 5.0 V, many programmers verify in two passes, one with V_{CC} at 4.75 V and the other with V_{CC} at 5.25 V.

Now examine figure 7, the Atmel RAPID algorithm. It looks similar to the quick-pulsing type of algorithm, but with a slight difference. If you look closely you'll see that it consists of three sections instead of just two. The first section is the programming section, where the programmer programs every location in the EPROM without verifying. Next there is the verify/repair

Figure 6: QUICK-PULSE type.

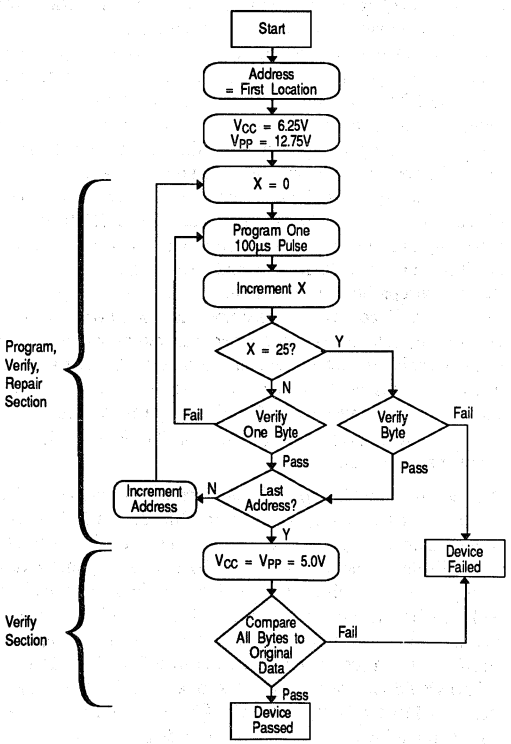


Figure 7: RAPID programming algorithm.

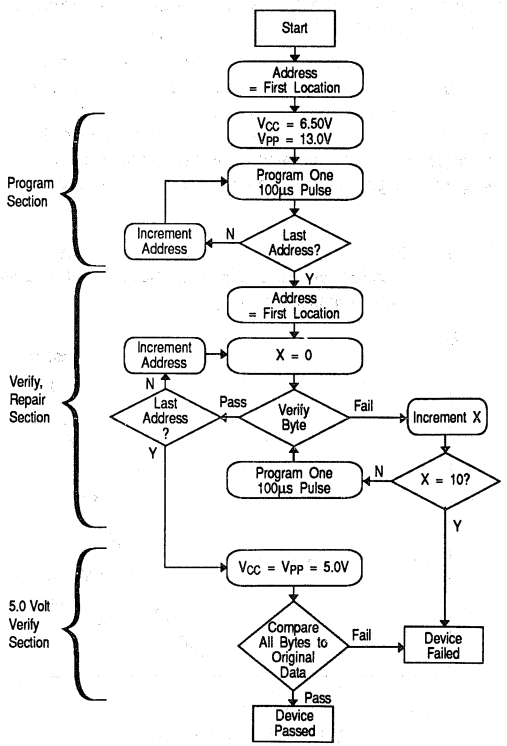


Figure 8: Row of EPROM cells from AT27C010. Note that the programming margin of each cell is 0, which allows each bit to read a "1".

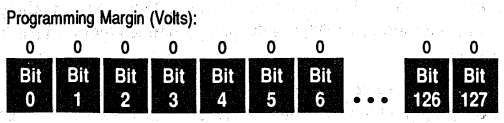


Figure 9: Bit 0 has been programmed, (QUICK-PULSE algorithm)

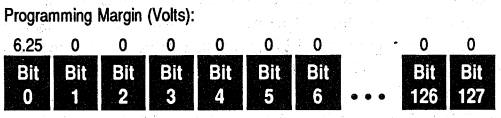
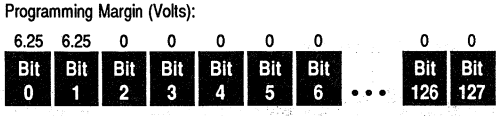


Figure 10: Bit 0 and bit 1 have been programmed.



section, where the programmer starts at the beginning of the EPROM and verifies every location for the correct data at 6.5 V. Any cells that don't pass are reprogrammed up to 10 times before the device is failed. The last section lowers V_{CC} to 5.0 V and does a final verify of the data (here again, most programmers verify in two passes, one with V_{CC} at 4.75 V and the other with V_{CC} at 5.25 V). This type of programming algorithm is called a two-pass algorithm, because it goes through the memory array twice during programming.

Well, this all sounds fine, but what difference can the programming algorithm possibly make? We can find the answer to that question in a particularly sneaky deprogramming mode that EPROMs can exhibit. We all know that EPROMs are erased by exposing them to short-wave ultraviolet light, right? Nothing more than applying Einstein's discovery of the photoelectric effect. But there is another erasure mode that can occur, one that people in the E^2PROM business know about. If you were to examine some EPROM cells in an electron microscope, you might find a few that have small, tooth-like projections (called asperities) on the top of the floating gate polysilicon. These projections won't affect the normal operation of the EPROM, but they could give you problems during programming. When you program a row of cells on an EPROM, cells that have been previously programmed still feel the full brunt of the high V_{PP} voltage on their gates when subsequent cells on the same row are programmed, because all of the cells on a row have their gates connected together. The combination of high voltage on the gate and ground on the drain and source causes an intense electric field in each previously programmed cell. If any one of the cells on that row have these tooth-like projections on their floating gate polysilicon, the resulting electric field in the oxide above the projections will be much more intense than normal. This intensified electric field can give some of the electrons on the floating gate enough energy to jump the oxide barrier, thereby partially erasing the EPROM cell. This unwanted effect, called programming erase, can be responsible for poor programming margins unless the programming algorithm takes this problem into account.

Before we continue, it's important to realize that this type of cell doesn't have a **reliability** problem, it has a **programmability** problem. This cell will have the same long-term data retention as any other cell in the device, even if it loses part of its programming charge. Although it is an EPROM, it has the same charge retention characteristics as many manufacturers' E^2PROM cells that use this type of erasure mode, and they all exhibit excellent long-term data retention. The challenge is to find these low-margin cells in the device with our programming algorithm, and to repair them so that the device functions normally.

Let's see what kind of impact a cell like this can have on programming margin by programming a row of EPROM cells from our AT27C010 1-megabit EPROM with both algorithms. The array geometry on the 1-megabit is 128 columns by 1024 rows, by 8 outputs. This means that a single row from a single output has 128 EPROM cells. Let's say that the second cell on this row, bit 1 (we'll call them bits and start with bit 0), has an asperity, just like the one mentioned above. When we go to program bits 2, 3, 4, etc., the voltage present on the gate of bit 1 causes the E^2PROM-like erasure mode. Given enough subsequent bits to program, bit 1 may lose enough charge to appear unprogrammed. Let's take a look at how the QUICK-PULSE type of algorithm will fail the device, or even worse, pass it with poor programming margin. Then we'll see how the RAPID algorithm will program it such that it works perfectly!

If we examine figure 8, we see the row of EPROM cells taken from our AT27C010 1-megabit device. Recall that bit 1 is the cell that's having the programmability problem, while the rest of the bits function normally. For the sake of example, let's say that for each subsequent bit after bit 1 that's programmed, bit 1 will lose 8 millivolts (mV) of programming margin. Let's also assume that the nominal programming margin for each cell is at least the value of V_{CC} present during programming, which is 6.25 V for QUICK-PULSE type algorithms and 6.5 V for the RAPID algorithm. Starting with the QUICK-PULSE type of algorithm at bit 0, we program it, verify it, and find that it passes (remember our flowchart from figure 6?) with the correct margin (see figure 9). We move to cell 1, program it, verify it, and it passes (see figure 10). Remember, bit 1 only loses voltage

Figure 11: Bits 0, 1 and 2 are programmed. Notice that bit 1 has been slightly erased.

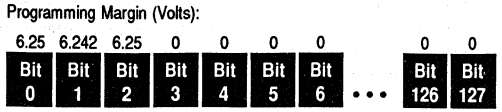


Figure 12: Bit 3 has just been programmed. Notice that bit 1 has been further erased.

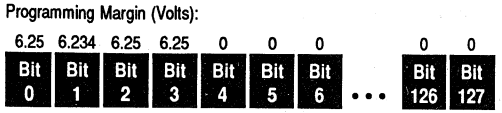
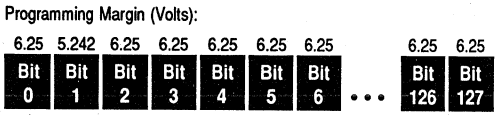


Figure 13: The entire row has been programmed. Notice how much bit 1 has been erased.



margin when subsequent cells are programmed. Now we move on to bit 2, program it, verify it, and in the process reduce bit 1's programming margin down to 6.242 V (see figure 11). Next we go to bit 3, program it, verify it, and in turn reduce bit 1's programming margin down to 6.234 V (see figure 12). This process continues until we get to bit 127. By this time bit 1 has experienced 126 subsequent cell programming cycles, and its programming margin will be reduced to 5.242 V (see figure 13). Since the QUICK-PULSE type of algorithm does its high-voltage verify immediately after programming, the algorithm has no way of knowing what has happened to bit 1, once it finishes programming it. Only when the algorithm does its final verify with V_{CC} set at 5.25 V could it detect that bit 1 is not fully programmed.

In this example we were able to detect bit 1 as being bad, and we would fail the device. But what if bit 1's erasure rate was slightly less than 8 mV per subsequent cell, say 7.7 mV? Bit 1's margin might be somewhere around 5.3 V, which would probably pass the 5.25-V verify check on our programmer. But remember the problem that we discussed earlier, about the power supply noise glitches messing up the operation of devices with low programming margin? A device with only 5.3 V of margin is a prime candidate for this type of problem. A small noise glitch occurring during data access on the V_{CC} line of this EPROM could easily change the output from a "0" to a "1". And, to make matters worse, this problem would probably occur randomly; the eventual diagnosis being that the device was intermittent. The unfortunate truth is that there is nothing wrong with the EPROM, it's the programming algorithm that's at fault.

So let's go back to our row of 128 EPROM cells, erase them, and reprogram them with the RAPID algorithm. Remember that with the RAPID algorithm the initial program and verify routines are located in different sections of the algorithm, they are not contained within the same loop. Starting at bit 0, we program it (to 6.5 V this time, see figure 14). Then move to bit 1, and program it (see figure 15). Next to bit 2, program it, and in turn reduce bit 1's programming margin to 6.492 V (see figure 16). Then on to bit 3, program it, and further reduce bit 1's programming margin to 6.484 V. We continue programming until we get to bit 127, and you'll find that the programming margin for all the cells looks similar to figure 8 (see figure 17). But wait, we're not finished yet. We move back to the beginning of the EPROM array, which is bit 0, and verify that it has 6.5 V of programming margin. Since we are verifying at

Figure 14: Bit 0 has just been reprogrammed (RAPID algorithm).

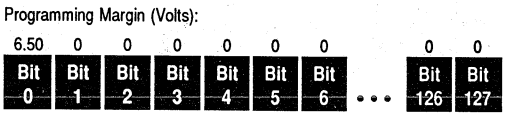


Figure 15: Bit 1 has just been programmed.

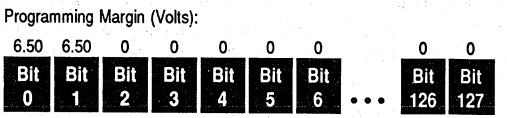
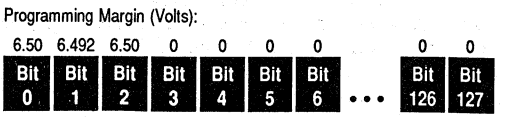


Figure 16: Bit 2 has just been programmed. Notice how bit 1 has been slightly erased again.



6.5 V, we pass it. We now move to bit 1 and notice that its programming margin is 5.492 V. This fails our 6.5-V verify, so we program it one more time and raise its margin back to 6.5 V, then pass it (see figure 18). Then we move to bit 2, and pass it, since its programming margin is also 6.5 V. Notice that we didn't deprogram bit 1 in the process of verifying bit 2. We only deprogram bit 1 when we program subsequent cells; reading or verifying (which is reading) doesn't generate the intense electric fields needed to deprogram EPROM cells. After verifying (and repairing) this row of cells, we return V_{CC} to 5.25 V, do a final data verify, then pass the row (see figure 18). Now compare figure 18 with figure 13. That's how the RAPID algorithm can guarantee programmability!

Well, you may ask, what if we had five problem cells on the same row? Wouldn't the additional programming pulses during the verify function deprogram previously programmed and verified cells? They probably would, but the maximum amount of deprogramming on the first bit (using this model) would be only 32 mV (4 x 8 mV). This gives us a programming margin of 6.468 V, which is still an excellent programming margin.

When you compare the quick-pulse type algorithms to the RAPID algorithm, there really is no comparison. The RAPID algorithm simply guarantees programmability, and we demonstrated this with the deprogramming bit example, which is one of the trickiest programming problems you can have. But the RAPID algorithm caught the problem, and repaired the bit so that the EPROM will function normally. That's why Atmel has changed its EPROMs programming algorithms over to the RAPID algorithm, and why all new devices will use this algorithm. You'll be glad we did!

Figure 17: The entire row has just been programmed. Notice how much bit 1 has been erased.

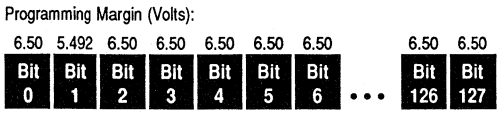
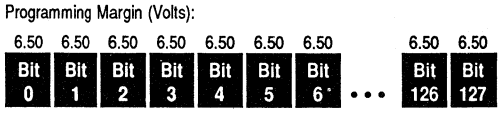


Figure 18: The entire row has just been verified at 6.50 Volts. Notice how bit 1 has been repaired, its margin being returned to 6.50 Volts using the RAPID algorithm.



12

The Atmel 3-Volt EPROM Family AT27LV256R, AT27LV512R, AT27LV010

Low Voltage UV Erasable CMOS EPROM

Application Note

- Why 3-volt operation?
- Does the whole system have to be operated at 3 volts?
- How do you program a 3-volt EPROM?
- What happens if you run a 3-volt device at 3.6 or 4 volts?

The Atmel AT27LVXXX series of EPROMs was designed to operate over a wide range of supply voltages from 3.0 to 5.5 volts. This offers the designer the opportunity to take advantage of either the greatly reduced power consumption at 3 volts or the ability to tolerate large power supply fluctuations.

The 3-volt series of EPROMs is specified to draw a maximum of 8.0 mA at 3.3 MHz when operated at 3.3 VDC. This is one fourth of the specified maximum current of a standard EPROM operating at 5.0 VDC. Because of the low supply voltage, the power savings calculations are even more dramatic: 26 mW for the LV series compared to 150 mW for standard 5-volt devices. That means much longer battery life.

The LV series has CMOS inputs and outputs specified for TTL levels and 3-volt CMOS levels (Rail-to-Rail). In other words, an LV device with V_{CC} = 3.0 VDC can drive standard 5-volt TTL logic devices on its data output lines making interface with 5-volt logic easy. The LV series of EPROMs can even be safely driven by 5-volt signals, even though their V_{CC} is at 3.0 VDC. The next question that comes to mind is "Why run just one EPROM at 3 volts while the rest of the system uses 5 volts?" One reason is if your system is on a very tight power budget, such as battery operated equipment, daughter boards or phone line powered products, the six times power savings might make significant difference. Of course your design might use more than one EPROM, for map memory, operating system, font storage or maybe smart cards. In this case the total power savings can be very large. Remember at 150 mW each, 8 EPROMs at 5 volts use 1.2 Watts instead of 210 mW for the 3-volt devices!

When the 3-volt devices are in a programmer they work just like their standard Atmel 5-volt counterparts. Absolutely no difference! Programming support is already in place and widely available on most programmers on the market today. Again they erase and program exactly the same as 5-volt devices.

The AT27LVXXX series of EPROMs are specified to operate from 3 to 5.5 volts. So what happens when the device is operated above 3 volts? It speeds up and draws more power, but never more than a standard EPROM. This feature offers the most flexibility for system manufacturers. The data sheets include a full set of curves that show speed and power variations versus power supply voltage.

The Atmel AT27CL010 Low-Power EPROM

Low Power UV Erasable CMOS EPROM

Application Note

The Atmel AT27CL010 1-megabit EPROM was designed for minimum current consumption over the range of supply voltage from 4.5 to 5.5 volts. This device is available in access times down to 150 nano-seconds, which gives the designer the best of both worlds— low current consumption and fast access times.

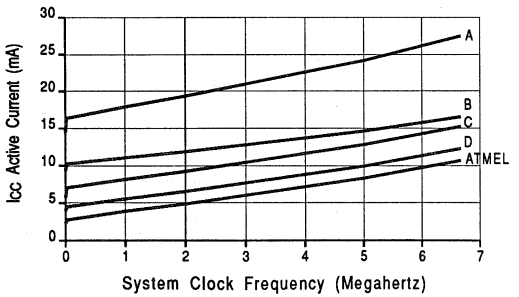
The AT27CL010 typically draws about 8 milliAmps at 5-MHz system clock rate. This is lower than most popular low-power 1-megabit devices currently on the market. In standby mode, the AT27CL010 typically draws only a few microamps of current, which is great news to anyone needing to operate their circuit on batteries. With only 5 to 10 microWatts (typical) of power dissipation in standby mode, you can bet your batteries will last a long time.

"Why is it so important to have a low-power EPROM for designs requiring batteries?" In applications such as cellular phones, mobile radios, personal paging systems, etc., the unit is never really shut off, it's just in a low-power or standby state. This is so it can turn itself back on when, say, an incoming call comes through. These are the sort of applications that can benefit from the low-power specifications of the AT27CL010. The extra milliamps saved in active mode— in some cases up to 17 milliAmps typical at 5-MHz system clock rate— coupled with the low current draw in standby mode, could mean from weeks to months in extended battery life.

"But what about programmer support, won't that take a while to get?" Not so, The AT27CL010 programs just like a standard Atmel 1 megabit device. As a matter a fact, if your programmer presently supports the Atmel AT27C010, you already have support for the AT27CL010! And as you would expect from Atmel, this low-power 1 megabit is available in a host of different packages; including ceramic and plastic DIP, ceramic and plastic J-leaded chip carrier, and ceramic leadless chip carrier.

Take a look at the graph below and compare the Atmel AT27CL010 to other low-power 1 megabit EPROMs on the market. Then try one in your circuit and stop wasting battery life today.

EPROM Active Icc Current Comparison
Atmel AT27CL010 vs. Other Popular 1 Megabit EPROMs



12

Using Programmable Logic Devices

Introduction

This Application Note covers three areas:

- Where and *why* do I use programmable Logic Devices (*PLDs*)?
- *How* do I use PLDs?
- Software and Hardware *support* for Atmel PLDs.

Where Do I Use PLDs?

Any digital logic design can be done using PLDs. If you normally begin your design by:

- Using AND and OR functions
- Thinking of 7400 series components
- Using truth tables, or
- State diagrams

you are already on the path to using PLDs.

Designing a microprocessor based system, with memory and I/O? How about all that "glue" logic you use to interface with the bus, provide chip selects, and any unusual signals required by special chips? Most of these functions are currently done with 7400 series TTL. *How about using a PLD instead?*

Designing a stand-alone PC board which uses a state machine to control multiple output signals? Using latches to synchronize signals? Using counters to divide down master clock frequencies? Converting parallel to serial and back again? All of these functions fit easily in modern PLDs. *Most anything found in your TTL Databook can be replaced with your own, PERSONALIZED, programmable logic device.*

PLD Applications

- **Glue Logic**
- **State Machines**
- **Synchronization**
- **Decoders**
- **Counters**
- **Bus Interfaces**
- **Parallel to Serial**
- **Serial to Parallel**
- **Subsystems**
- **and Many Others**

Why PLDs?

Maybe you have already heard all the wonderful reasons for using PLDs. Well, they're true! First, let's review some of the more important ones:

- **Increased Integration.** You can reduce the package count of your designs while simultaneously increasing the features offered by your product.
- **Lower Power.** CMOS and fewer packages combine to reduce power consumption.
- **Improved Reliability.** Lower Power plus fewer interconnections and packages translate into greatly improved system reliability.
- **Lower Cost.** PLDs reduce inventory costs, too.
- **Easier To Use!** Yes, believe it or not, once you get past the initial learning period, PLDs are easier to use than discrete logic functions.
- **Easier to Change.** Oops! Need to make a change? You won't need "blue wire" when you use a PLD— all changes are internal, and can be done quickly. ECNs are a snap— and system reliability is maintained!

UV Erasable Programmable Logic Device

Application Note

Let's Get Started!

Figure 1 describes the PLD design process. After having read the first part of this application note, you now have the perfect application for a PLD, right? So here you go!

How do you translate your idea into a working prototype? *First, you need a computer with an editor of some kind.* If you have a workstation with a schematic editor, you may input your design using familiar logic blocks. Otherwise, a line or full screen text editor, used in the non-document mode will do. An example of an ABEL™ text file is on the next page.

Next, turn the **logic compiler** loose on your design. First it will *check for typographical errors* and any inconsistencies in your specification. Most compilers then attempt to *reduce your logic* using standard logic reduction theory. Then, a **simulator** will check the test vectors you input, comparing your logic description against the predicted responses. This is an excellent way to verify your design. Check with the appropriate software manuals for more information.

At the end of the compilation process, a "**JEDEC**" file is output. This file is a standard format accepted by most programming hardware. Next *download this file* to your chosen programmer.

At this point you are ready to "build" your **prototype**. Make sure the programmer has the correct information to program the device you have chosen (an Atmel PLD, of course), plug in your device, and go! Most programmers will even functionally test your prototype for you if you include test vectors in your JEDEC file.

Take your configured PLD, and *plug it into your system.* If you find any errors, just use your editor to make the necessary changes, and repeat the process. It's easy!

Example Design

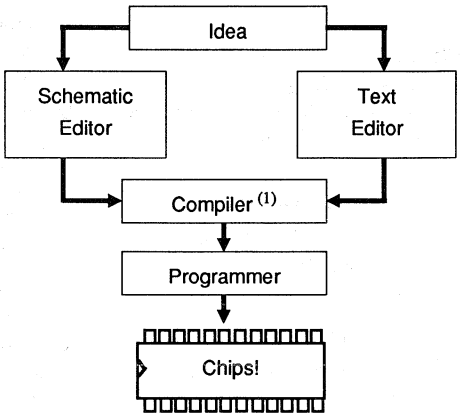
The following design is a simple example using ABEL™ to process the logic description file and an AT22V10 as the target device. The equations are on the next page, and are a direct reproduction of the actual ABEL input file.

Each of the three allowable input formats are shown. A truth table is used to describe a simple 2 to 4 decoder, as is often used to decode chip selects in a microprocessor system. Next, the state machine format is used to describe a divide by 4 counter. And finally, boolean equations are used to describe some random logic.

Note the test vectors used to test the device. The "c" nomenclature means that this pin has a low to high to low series of transitions for this vector. Each time this happens, the counter should increment. Also note that the counter starts in the reset condition, which is both outputs "1" for an active low output.

Now you're ready to go - Have fun!

Figure 1. PLD Design Process



Note: 1. Examples of compilers are ABEL™, CUPL™, and LOG/iC. Each of these products contains modules which allow simulation of your design. They also minimize your logic equations, which gives you flexibility in describing your design.

Software Support Versions

Atmel EPLD	Data I/O ABEL™	Logical Devices CUPL™	ISDATA LOG/iC	Atmel-ABEL™	PistoHI Pet100
AT22V10	1.3,2.0,3.0	2.0	2.3		1.XX
ATV750	3.0	2.15b	3.0	1.01	1.XX
ATV2500	3.2	3.2a		1.01	1.XX
ATV5000	4.02	-IST 1.0		4.02	

Example Abel™ Description File

```
module X3  flag'-r3';
title 'Example using 22V10 - KHG 1/6/88';
X310 device 'P22V10';
"
Clk,A12,A13              pin     1,2,3;
CE0,CE1,CE2,CE3          pin     20,21,22,23;
Q1,Q2,CarOut             pin     17,18,14;
CarEn,A,B,C,D            pin     6,7,8,9,10;
Out1,Out2                pin     15,16;
"
X , Z , c       =       .X. , .Z. , .C.;
"
"Counter States
State1   = ^b00;    State2   = ^b01;
State3   = ^b10;    State4   = ^b11;
"
"The following truth table defines the 2 to 4 decoder, which decodes
"   A13 and A12 into CE0, CE1, CE2, and CE3.
truth_table ([A13,A12] -> [CE0,CE1,CE2,CE3])
[ 0 , 0 ] -> [ 0 , 1 , 1 , 1 ];
[ 0 , 1 ] -> [ 1 , 0 , 1 , 1 ];
[ 1 , 0 ] -> [ 1 , 1 , 0 , 1 ];
[ 1 , 1 ] -> [ 1 , 1 , 1 , 0 ];
"The following state description defines the divide by 4 counter
state_diagram  [Q2,Q1]
State State1:   GOTO   State2;
State State2:   GOTO   State3;
State State3:   GOTO   State4;
State State4:   GOTO   State1;
"The following equations are general in nature to illustrate boolean input
"   format.  The CarOut equation uses state 4 above to produce a carry.
Equations
CarOut  =   Q2  &  Q1  &  CarEn;     "& = AND
Out1    =   A  &  B  +  C  &  D;   "+ = OR, AND takes precedence
Out2    =   A  &  C  +  B  &  D;
"The following are the appropriate test vectors
test_vectors
"
([Clk, CarEn, A13,A12, A, B, C, D]- > [CE0,CE1,CE2,CE3,Q2,Q1,CarOut,Out1,Out2]);
[ 0,  0 ,  0 ,  0 , 0,  0 , 0,   0  ] - >[ 0 , 1 , 1 , 1 , 1, 1,  0 ,  0 ,  0];
[ c,  0 ,  0 ,  1 , 1,  1 , 0 , 0  ] - >[ 1 , 0 , 1 , 1 , 0, 0,  0 ,  1 ,  0];
[ c,  0 ,  1 ,  0 , 1,  0 , 1 ,  0  ] - >[ 1 , 1 , 0 , 1 , 0, 1,  0 ,  0 ,  1];
[ c,  0 ,  1 ,  1 ,  0,  0 ,  1 ,  1  ] - >[ 1 , 1 , 1 , 0 , 1, 0,  0 ,  1 ,  0];
[ c,  0 ,  0 ,  0 ,  0 , 1 ,  0,  1  ] - >[ 0 , 1 , 1 , 1 , 1, 1,  0 ,  0 ,  1];
[ 0,  1 ,  0 ,  1 ,  1 , 1 ,  1,  1  ] - >[ 1 , 0 , 1 , 1 , 1, 1,  1 ,  1 ,  1];

end X3;
```

New Programmer Support Information

Company	Model	AT22V10 Version	Fam/Pin Code	ATV750 Version	Fam/Pin Code	ATV2500 Version	Fam/Pin Code	ATV5000 Version
Data I/O	Model 29B LogicPak 303A-011A	04	6528	05	650F			
	Model 60A	11	6528					
	Unisite	1.7	Menu	2.2	Menu	2.45	Menu	3.40
	2900	1.0	Menu	1.0	Menu	1.4	Menu	
Stag	Model ZL30,ZL30A	30A27	47070	30A30	47165			
PistoHI	PET100	PP61	Menu	PP61	Menu	PP62		
Logical Devices	AllPro40	1.49C	Menu	1.48C	Menu	1.49C		
	AllPro88	2.00D	Menu	2.00D	Menu	2.00D		
SMS	Sprint Plus	3.2H	Menu	3.2H	Menu			
	Sprint Expert	3.2K	Menu	3.2J3	Menu	3.2J3		
BP Microsystems	PLD-1100	1.11	Menu	1.12	Menu			
Advin Systems	Sailor-PAL	9.72	Menu	9.71	Menu			
	Pilot-U40	10.05	Menu	10.05	Menu	10.05		
System General	SGUP-85	2.1		3.1				
Inlab / Prog. Tech.	28A	10.03g		10.03g				
Owen	APII	1.73a						

Programming Software Companies

ACCEL Technologies, Inc.
6825 Flanders Drive
San Diego, CA 92121
(800) 433-7801

Data I/O Corporation (ABEL™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

ISDATA GmbH (LOG/IC)
Haid-und-Neu- Str. 7
D-7500 Karlsruhe 1
West Germany
0721 / 69309

800 Airport Rd.
Monterey, CA 93940
(408) 373-3607
(800) 777-1202

Logical Devices (CUPL™)
1201 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

PistoHI Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422
(800) 2PISTOHL

Programming Hardware Companies

Advin Systems, Inc.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 243-7000

BP Microsystems
10681 Haddington #190
Houston, TX 77043
(713) 461-9430

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

Inlab / Prog. Tech.
2150 IW 6th Ave
Broomfield, CO 80020
(800) 237-6759

Logical Devices
1201 N.W. 65 Place
Ft. Lauderdale, FL 33309
(305) 974-0967
(800) 331-7766

Owen Electronics GmbH
Ringstr. 11
Postfach 1104
D-6798 Kusel
Germany
(49) 6381-5085

PistoHI Electronic Tool Co.
22560 Alcalde Rd.
Cupertino, CA 95014
(408) 255-2422

SMS SPRINT International
Im Morgental 13
D-8994 Hergatz
Germany
(49) 7522-5018

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

System General
244 S. Hillview Drive
Milipitas, CA 95035
(408) 263-6667

Selecting Decoupling Capacitors For Atmel's EPLDs

Introduction

This application note provides a summary of information needed when selecting decoupling capacitors for Atmel Programmable Logic Devices. A .22 µF, multi-layer ceramic or plastic dielectric capacitor is recommended for such use. Either surface-mount (SMD) or radial-leaded devices should be used. Because of their high parasitic resistance and/or inductance, tantalum, aluminum electrolytic, and axially leaded capacitors are not recommended.

When Is a Capacitor Not a Capacitor

Unfortunately, capacitors are not the perfect charge storage devices we would like them to be. Their lead wires and internal construction create parasitic resistance and inductance in series with the capacitance. These parasitics are usually referred to as ESR (equivalent series resistance) and ESL (equivalent series inductance), respectively. As will be shown, these parasitics can seriously reduce the ability of many types of capacitors to decouple supply noise in high-speed systems. Table 1 gives typical ESR and ESL values for various types of capacitors.

As shown, ESR values range from 0.01 Ohm to as high as 9 Ohms. ESL varies from 2 nH for typical surface mount devices to 20 nH for electrolytic capacitors. These numbers are typical values, taken from data from several manufacturers. As expected, there is some variation between manufacturers. Also, worst case specification values will be significantly higher, especially for ESR values.

How ESR And ESL Can Affect High Speed Operation

The effects of these parasitics may be best illustrated by a simple example. Consider the case of a 22V10L. In the stand-by mode, Icc current is typically only 5 mA. When an input switches, Icc may temporarily go as high as 100 mA. This increase in current draws charge from the local decoupling capacitor. This capacitor current will create voltage drops across the ESR and ESL parasitic elements. To see how these voltage drops can cause problems in a system, look at a typical decoupling application.

In this example the design goal of the capacitor is to keep local supply noise below .2 volts, a reasonable expectation. This immediately sets an upper limit on ESR of 2 Ohms.

$$ESR_{max} = V_{noise} / I_{max}$$

Imax= Highest Expected Capacitor Current

The upper limit on ESL is determined by how quickly the capacitor's current must change, as well as how much supply noise will be tolerated during that change. For high-speed logic devices, Icc must be able to switch from stand-by to active levels within 2 to 3 nanoseconds.

$$ESL_{max} = V_{noise} \cdot I_{max} / \Delta t;$$

Δt = Time allowed for capacitor current to switch

In this example, an upper limit on ESL of 4 to 6 nH is set.

Consider what can happen if these limits are exceeded. If an axially leaded multi-layer ceramic capacitor with ESR of .15 Ohm is used, the resistance drop in our application

will not be significant (100 mA X .15 Ohm = 15 mV). However, the inductance will not allow the current to reach 100 mA in 6nsec. This can slow the logic device switching by several nanoseconds.

What Types To Use: Multi-layered Ceramic and Plastic Dielectrics

From this example, it is apparent that the parasitic elements on capacitors can easily limit their decoupling ability. Therefore, users of high-speed logic need to pick their capacitors with care. The data in Table 1 shows that the best bets are surface-mount, multi-layered ceramic (MLC) or plastic dielectrics. Of the leaded devices, only radial types are recommended.

Within the MLCs, there are different classes of dielectric. Class I has the best characteristics, but its small dielectric constant makes it impractical for decoupling values. Class II is highly recommended, as it has good temperature stability (% variation -55°C to 125°C) and aging characteristics (10% in 10 years). Class III, on the other hand, drops to less than 50% of its rated capacitance at 85°C, and to only 25% at -55°C. Class III dielectric also loses 20% of its rated value in 10 years. Therefore, Class III MLCs are only recommended for applications where temperature excursions are minimal.

Plastic dielectric capacitors in general offer performance as good as Class II MLCs. Among the dielectrics available today are polypropylene, polyester, polycarbonate, polystyrene and teflon. Capacitance variation with temperature depends on the particular material, but is generally less than +/-20% from -55°C to 125°C. Aging is minimal, usually less than 2% in 10 years. Unfortunately, not many manufacturers make surface mount plastic dielectric capacitors. That should change soon, as surface mount technology advances and becomes more common.

When using radial leaded cases, be sure to minimize lead lengths, as ESL increases quickly with longer leads. For example, if a capacitor has 6 nH of inductance with 2 mm leads, extending leads to 5 mm will increase ESL to 10 nH.

What Types Not To Use: Aluminum Electrolytic, Tantalum, And Anything Axial

The design example above together with the numbers given in Table 1 show that some types are not suitable at all for decoupling high-speed devices. Specifically, the high inductance of axially leaded capacitors puts them on the "don't use" list. Also, tantalum and aluminum electrolytic devices are generally not recommended, as they have high ESR and/or ESL, even in radial and surface mount configurations.

In Any Case, know Your ESL and ESR

ESR data is often found in catalogs. However, this will normally be only low-frequency data, and ESR is frequency dependent (dropping at higher f). ESL data is not usually given in catalogs. The best thing to do is get Z versus frequency data from the manufacturer. From such a graph (with frequency up to at least 10 MHz), you can extract high frequency ESR and ESL.

How Much Capacitance Do I Need

For decoupling Atmel's EPLDs a .22µF capacitor is recommended. In many cases, this will be overkill. However, determining how much less you could get by with for a particular application is dependent upon several factors. The number of PC board supply planes, the board's dielectric thickness and dielectric constant, the value (AND ESR AND ESL!) of power entry decoupling capacitors, among other things, will determine just how much is really needed. The best bet is to use a good .22 µF and be safe. Besides, the more decoupling is taken care of by local capacitors, the lower the board's HF emissions will be.

Summary

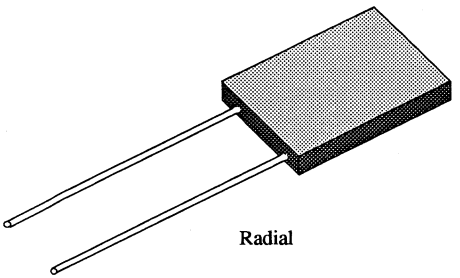
Choosing the right decoupling capacitor is an important part of high-speed circuit design. Choosing the wrong one can introduce supply noise that can slow down signal switching or even end up giving incorrect data. For decoupling Atmel EPLDs, .22 µF capacitors are recommended. These should be of either multi-layer ceramic or plastic dielectric type. Surface mount devices are best, with radial leaded cases also being acceptable.

Table 1. Capacitor Types and Recommendation Ratings

Dielectric	Body	L (nH,typ)	R (ohm,typ)	Rating	Comments
Ceramic II	SMD	2	.02	E	Highly recommended
	Radial	6	.07	G	Keep leads short
	Axial	12	.07	S	Axial always=Higher L
Ceramic III	SMD	2	.04	G	C loss hot/cold/old
	Radial	6	.15+	S	
	Axial	12	.15+	X	
Plastics	SMD	2	.03	E	Hard to find
	Radial	5+	.01+	G	Get R and L data
	Axial	12+	.01+	X	
Aluminum Electrolytic	SMD	13	9.0	X	Forget it
	Radial	15+	1.5+	X	
	Axial	20	1.5	X	
Tantalum	SMD	?	3.0	X	
	Radial	10+	1.0	X	
	Axial	15+	1.0	X	

Ratings code:
E Excellent; highly recommended
G Good; will perform well in most applications
S Satisfactory; be aware of specific vendor's device performance
X Not recommended

Axial



Radial

S.M.D.

Using a Programmable Logic Device As a System Controller In an I/O Bus Based System [1]

Summary

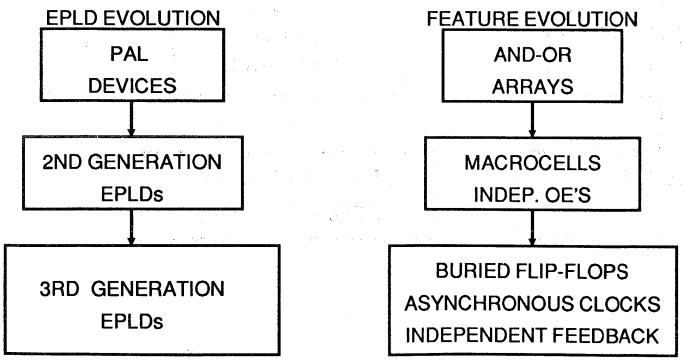
As PLDs (Programmable Logic Devices) become more complex, the amount of logic that can be placed in one device is rapidly increasing. Complete controllers and subsystems now fit into one or two PLDs. As a result, the PLD may now be connected directly to the system bus as an independent peripheral. First generation PAL® devices are difficult to use in these applications. However, recent innovations in PLD architecture enable them to be easily designed into bus-based systems.

PLD Evolution

The driving force behind PLD usage has been to integrate as much of the SSI (Small Scale Integration) logic on a packed PC board as possible. The first level of integration was made possible by the invention of the PAL device. First generation products were usually in 20-pin packages with a typical device having nine dedicated inputs and eight dedicated outputs. One input pin was a dedicated output enable, and one pin a dedicated, common clock for up to eight flip-flops. Making one of these devices work on an I/O bus was difficult and typically was used as little more than a simple latch.

In the mid-eighties, second generation devices appeared. These PLDs are generally in 24 or more pins, have independent output enable controls and "Output Macrocells." The macrocells allow the designer to configure each output independently as registered or combinatorial. However, there are still too few registers in these devices to allow the design of complex state machines. Also, these circuits lack independent feedback paths, which further reduce the usable number of registers. This also complicates the use of the output pins as true I/O structures.

Note: 1. This article originally appeared in Northcon '86
®PAL is the registered trademark of Monolithic Memories



Recently several third generation devices (such as the Atmel ATV750) have appeared. These devices are differentiated by the following features:

- **Extra Registers**

Up to twice the usual number. The ATV750 has 20 flip-flops.

- **Independent Feedbacks**

Feedback paths for the registers are independent of the output configuration. In addition, there are separate input paths from the I/O pads.

- **Asynchronous Clocks**

Product terms for each flip-flop's clock allows the designer to break up the registers into different functional blocks.

Control function outputs that have no other use than to manage the other resources inside the PLD need not be brought outside the device, allowing implementation of complex state machines internally.

As PLDs have evolved, so have the applications for them. Initially, PLDs could only integrate a few SSI functions. A typical application was a special-purpose decoder or encoder. With the introduction of more flip-flops, MSI (Medium Scale Integration) functions such as state machines could be designed. Third generation devices are the first true LSI (Large Scale Integration) devices, and are capable of integrating several of the previous generation devices into one package. Now state machines can be combined with an output decoder to control peripheral functions, and still have adequate resources to interface directly to the microprocessor.

System Application

The following example is an application of the Atmel ATV750 as a peripheral resource controller. The design required a state machine, a bus interface unit and a peripheral control interface. All 10 outputs of the ATV750 are used, most in the combinatorial mode. However, the 17 required flip-flops were still available to latch the address and data buses, provide a status register, and a two-bit counter. This design would require three second generation, 24-pin PLDs, or five first generation 20-pin devices and at least two other discrete devices. In all, more than 80 percent of the ATV750 is utilized. The number of gates alone integrated into the ATV750 in this application is more than other 24-pin PLD's have to offer.

- **The System**

The system described is a peripheral controller/bus interface for connecting a special-purpose, custom encryption / exponentiation chip to an 80186 microprocessor (Figure 1). The custom chip has a serial interface, and only one bi-directional pin to indicate its "busy" status. All chip functions are controlled with a set of single-purpose input pins. While simple, this interface is not directly compatible with a modern microprocessor, such as the 80186. The PLD system described not only combines the required glue logic, but also off-loads the parallel-to-serial conversion from the processor. This application note will only touch on the salient features of the design, and why a third generation device is so useful.

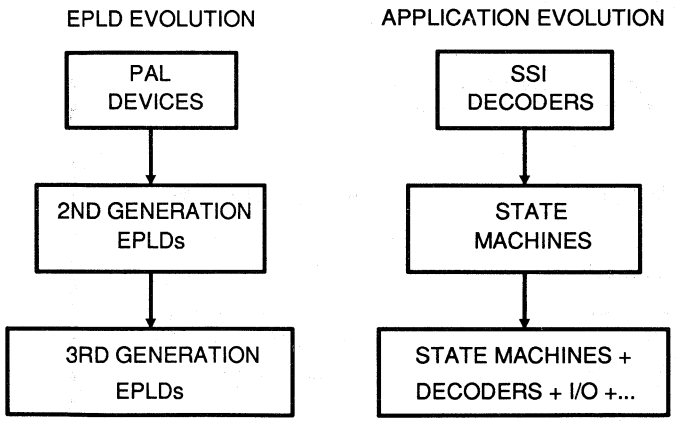
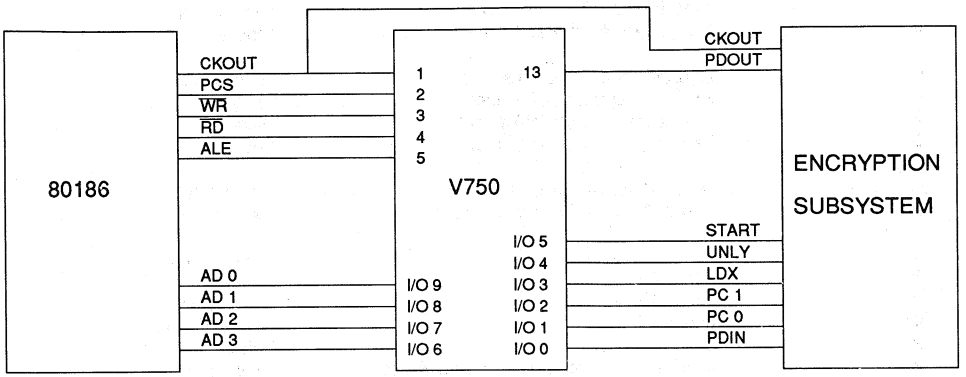


Figure 1. System Diagram



• The Microprocessor Bus

The 80186 uses a multiplexed address and data bus. Several control signals, such as ALE, $\overline{RD}$ and $\overline{WR}$ tell the system when to get what type of data from the bus. The 80186 also has some internally decoded chip selects, and one is used here for convenience. The system clock is an 8 MHz signal, which is appropriate for the encryption chip and well within this PLDs timing specification. The lower four bits of the address are latched into the PLD to define the upcoming operation, which then allows the PLD to output the requested data in one read cycle of the microprocessor. These address bits are decoded to define the instruction to be executed by the PLD subsystem.

• Tackling the I/O Bus

Using first and second generation PLDs, the equations for the I/O bus interface are shown in Figure 2. These equations consume 12 sum terms, 8 flip-flops, and 12 output pins. Since this requires two PLDs, another 10 input pins are required as well.

When rewritten for the ATV750, only four macrocells are required, and eight sum terms and flip-flops. No extra inputs are required, as the ATV750's I/Os are true input/output pins.

The equations for the ATV750 are in Figure 3. This compaction is possible for three reasons:

1. The individual product terms for OE permit the pin to be used as both an input and output.
2. The three feedback paths allow both registers to be used while the pin status is still available to the array.
3. The product term for the flip-flop clock means that the sum term for one of the flip-flops can be shared between the D input and the output pin. A single ATV750 macrocell can incorporate logic which would require up to three output pins and one input pin in other PLDs.

Figure 2.

```
ad0     =     adp0 & !pcs & !rd & ai0 & !ai2          "output data
        #     !pc0 & !pcs & !rd & !ai0 & !ai2         "status "
        #     yst & !pcs & !rd & !ai0 & !ai2;         "status unly

ad1     =     adp1 & !pcs & !rd & ai0 & !ai2          "output data
        #     !pc1 & !pcs & !rd & !ai0 & !ai2;        " status "

ad2     =     adp2 & !pcs & !rd & ai0 & !ai2          " output data
        #     xst & !pcs & !rd & !ai0 & !ai2          " status "
        #     !pc0 & !pcs & !rd & !ai0 & !ai2         " status  "
        #     !pc1 & !pcs & !rd & !ai0 & !ai2;        " status  "

ad3     =     adp3   & !pcs & !rd & ai0 & !ai2        "  output data
        #     startqb & !pcs & !rd & !ai0 & !ai2;     "  status "

adp0    :=    ad0 & !pcs & !wr                        "  load data
        #     pdout & !ystb                           "  circulate y"
        #     pdout & !xstb                           "  circulate x"
        #     pdout & !pcs0                           "  circulate load"
        #     pdout & !pcs1                           "  circulate load"
        #     adp0 & ystb & xstb & pcs0 & pcs1 & pcs  "  hold data"
        #     adp0 & ystb & xstb & pcs0 & pcs1 & wr;  "  hold data"

adp1    :=    ad1 & !pcs & !wr                        "  load data
        #     adp0 & !ystb                            "  circulate y"
        #     adp0 & !xstb                            "  circulate x"
        #     adp0 & !pcs0                            "  circulate load"
        #     adp0 & !pcs1                            "  circulate load"
        #     adp1 & ystb & xstb & pcs0 & pcs1 & pcs  "  hold data"
        #     adp1 & ystb & xstb & pcs0 & pcs1 & wr;  "  hold data"

adp2    :=    ad2 & !pcs & !wr                        "  load data
        #     adp1 & !ystb                            "  circulate y"
        #     adp1 & !xstb                            "  circulate x"
        #     adp1 & !pcs0                            "  circulate load"
        #     adp1 & !pcs1                            "  circulate load"
        #     adp2 & ystb & xstb & pcs0 & pcs1 & pcs  "  hold data"
        #     adp2 & ystb & xstb & pcs0 & pcs1 & wr;  "  hold data"

adp3    :=    ad3 & !pcs & !wr                        "  load data
        #     adp2 & !ystb                            " circulate y"
        #     adp2 & !xstb                            "  circulate x"
        #     adp2 & !pcs0                            "  circulate load"
        #     adp2 & !pcs1                            "  circulate load"
        #     adp3 & ystb & xstb & pcs0 & pcs1 & pcs  "  hold data"
        #     adp3 & ystb & xstb & pcs0 & pcs1 & wr;  "  hold data"

ai0     :=    ad0 & pcs                               "  idle state "
        #     ad0 & ale                               "  idle state "
        #     ai0 & !pcs & !ale;                      "  hold instruction"

ai1     :=    ad1 & pcs                               "  idle state "
        #     ad1 & ale                               "  idle state "
        #     ai1 & !pcs & !ale;                      "  hold instruction"

ai2     :=    ad2 & pcs                               "  idle state "
        #     ad2 & ale                               "  idle state "
        #     ai2 & !pcs & !ale;                      "  hold instruction"
```

Figure 3.

```
ai0.ck      =    clk2 & !ale; ai2.ck =   clk2 & !ale;    ".....clock instruction
ai1.ck      =    clk2 & !ale; ai3.ck =   clk2 & !ale;    ".....clock instruction

ai0         =    ad0 & !pcs & ale                        ".....load instruction"
            #    adp0 & !pcs & !rd & ai0 & !ai2          " .....output data
            #    !pc0 & !pcs & !rd & !ai0 & !ai2         ".....status "
            #    yst & !pcs & !rd & !ai0 & !ai2          " .....status unly

ai1         =    ad1 & !pcs & ale                        ".....load instruction"
            #    adp1 & !pcs & !rd & ai0 & !ai2          " .....output data
            #    !pc1 & !pcs & !rd & !ai0 & !ai2;        ".....status "

ai2         =    ad2 & !pcs & ale                        ".....load instruction"
            #    adp2 & !pcs & !rd & ai0 & !ai2          " .....output data
            #    xst & !pcs & !rd & !ai0 & !ai2          ".....status "
            #    !pc0 & !pcs & !rd & !ai0 & !ai2         ".....status  "
            #    !pc1 & !pcs & !rd & !ai0 & !ai2;        ".....status  "

ai3         =    ad3 & !pcs & ale                        ".....load instruction"
            #    adp3   & !pcs & !rd & ai0 & !ai2        " .....output data
            #    startqb & !pcs & !rd & !ai0 & !ai2;     ".....status "

enable ad0  =    !pcs & !rd;  enable ad2 =    !pcs & !rd;
enable ad1  =    !pcs & !rd;  enable ad3 =    !pcs & !rd;
(adp equations remain the same as before, but are now buried in the macrocell)
```

Figure 4.

```
!pc0        =    !clk22 & !pcs0;

!pc1        =    !clk22 & !pcs1;

!pcs0       :=   ai2 & ai0 & start
            #    !cn0 & count & !pcs0
            #    !cn1 & count & !pcs0

!pcs1       :=   ai1 & ai2 & start
            #    !cn0 & count & !pcs1
            #    !cn1 & count & !pcs1;
```

• The Chip Interface

The encryption chip is loaded and unloaded serially, four bits at a time in this design. The equations for the interface logic are in Figure 4. Also in this figure is a simple state diagram for the two bit counter required for this design. This state machine is buried, and its decoded outputs are used to control the serial transfers.

• Starting the Peripheral Chip

To begin execution in the peripheral chip, a bi-directional signal named "start" is asserted. This is an active low signal. The controller must assert this signal low for four clock cycles. Then the exponentiation chip will hold this line low until it has completed its operations. An external pull up resistor is required. The internal flip-flop, whose output is named "stint", contains the state of the peripheral. This is used to signal the microprocessor that the subsystem is busy when the processor reads the ATV750's status.

• Multiplexing Flip-Flop Inputs and I/O Pins

One I/O pin / flip-flop combination can be used to store the state of the encryption chip and to output this to the peripheral. This is accomplished by multiplexing the sum term output between the flip-flop's D input and the output buffer. The sum term and the OE product term are active to begin the encryption chip's exponentiation cycle. After the state machine counter finishes counting, the output is put into the high impedance state. If the external chip has begun its operation correctly, it will then hold the pin low. Now the state of the I/O pin is used as the D input to the flip-flop, but not output because the OE term is off. The multiplexed macrocell is in Figure 7. The following simple equations are all that is required to implement this logic:

enable start=!count;

stint:=!count

#!start & count;

start.c=clk2;

Conclusion

The application of a third generation EPLD in an I/O bus based system demonstrates the usefulness of the following features:

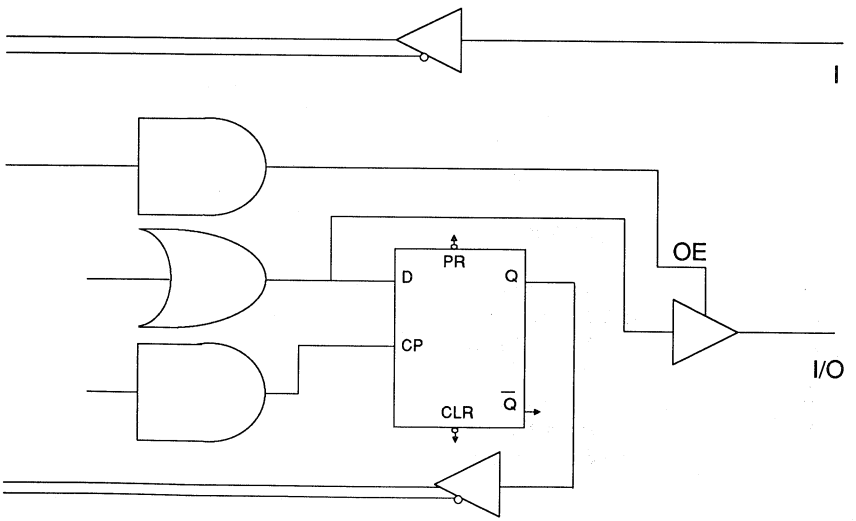
Buried Registers

Independent Feedback Paths

Asynchronous Register Clocks.

This design consists of roughly 600 gates, which fit into a ATV750 gate complexity EPLD with an 80 percent utilization factor. Due to the usefulness of the new features and their implementation in the macrocell of the ATV750, this design, which would have required 3 second generation devices, could easily fit into one ATV750.

Mulitplexed "D" Input

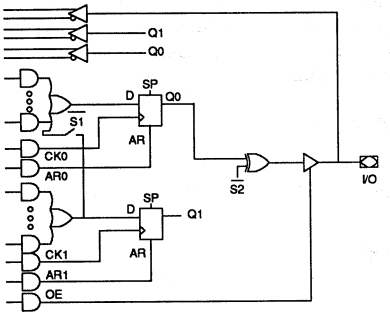


Using the Buried Nodes and Feedbacks

Introduction

Conventional EPLD I/O pin logic forces you to choose either a dedicated output pin or a dedicated input pin. This renders the output register unusable. Multiple feedback paths and individual product term controlled output enables (OEs) make the ATV750 I/O pins truly bi-directional. An ATV750 I/O pin can be configured as a dedicated input, a dedicated output, or an input and output bus interface pin. No registers are sacrificed in the process. All registers can be buried.

Registered Output



Buried Registers

To use the buried register outputs, they must have a unique name. The compilers need to know which register to associate with each signal name. Each compiler uses a different method for assigning node numbers to signal names. Table 1 shows how to assign these names for each compiler. Table 2 lists node names for each compiler. Note: Q1 need not be defined if Q0 is sharing Q1's product terms.

ABEL, Atmel-ABEL, CUPL, and Tango-PLD: If the output is combinatorial or if Q0 shares the product terms of Q1 in a registered output, the Q1 node does not need a name. Name Q1 nodes with the proper node numbers and refer to Feedback Options on how to access Q0s and Q1s.

LOGiC: LOGiC requires you to name the Q0 nodes if you are using the pin as an input and still using Q0, or if you are using OE to make the pin an input and an output.

PistoHl: No node numbers are necessary.
Q0 nodes are named by declaring
: nodename0 Q0! pinname;
Q1 nodes are named by declaring
: nodename1 Q1! pinname;

Table 1. ATV750 Node Declaration

Product	Example	Node	Declaration	Comments
ABEL	anyname	node	26;	
Atmel-ABEL	anyname	node	26;	
CUPL	pinnode	25 =	anyname;	
LOGiC	anyname	=	1;	Following key word *NODE
PistoHl	anyname	Q0!	pinname;	Use Q1! for Q1 declaration
TangoPLD	anyname			In PUTPART place "anyname" as the 25th signal

UV Erasable Programmable Logic Device

Application Note

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Table 2. ATV750 Node Numbers

ATV750 Pin Numbers	ABEL Q1	Atmel-ABEL Q1	CUPL Q1	LOGiC Q0	LOGiC Q1	TangoPLD Q1
14	26	26	25	2	1	25
15	27	27	26	4	3	26
16	28	28	27	6	5	27
17	29	29	28	8	7	28
18	30	30	29	10	9	29
19	31	31	30	12	11	30
20	32	32	31	14	13	31
21	33	33	32	16	15	32
22	34	34	33	18	17	33
23	35	35	34	20	19	34

ATV750 Feedbacks

Each third party product uses a slightly different syntax for accessing the feedback paths (refer to Table 3). Whenever the Q0 register is used and the OE term is disabled or conditionally disabled, care must be taken to ensure the correct feedback path is referred to in your equations. Version 1.11 of Tango-PLD does not support the Q0 feedback. This syntax may change with each new software revision. Please check with the specific software manufacturer or Atmel EPLD Applications if you are experiencing unexpected results.

Feedback Options: Registered Output

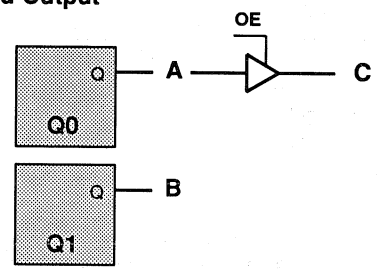


Table 3. ATV750 Feedback Paths

	A	B	C
ABEL	pinname.Q	nodename	pinname
Atmel-ABEL	pinname.Q	nodename	pinname
CUPL	pinname	nodename	pinname.IO
LOGiC	nodename0	nodename1	pinname
PistoHI	nodename0	nodename1	pinname
TangoPLD	no support	nodename	pinname

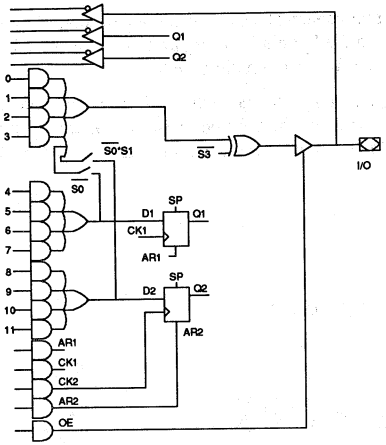
ATV2500 Node Numbering

With an additional OR, the ATV2500 logic cell becomes even more versatile than the ATV750 logic cell. Under certain situations, an additional set of buried registers must be defined. The same syntax used for ATV750 (Table 3) can be used to name the ATV2500 buried registers. The node numbers are listed in Table 4.

ABEL, Atmel-ABEL, CUPL, and TangoPLD: Q1 need not be named when the output logic cell is configured as 8- or 12-term combinatorial output. Q2 need not be named when output logic cell is configured as 12-product term combinatorial or registered output. Name Q1 and Q2 nodes with the proper node numbers and refer to Feedback Options for selecting the correct feedback paths.

PistoHI: No node numbers are necessary.
Q1 nodes are named by declaring
: nodename1 Q1! pinname;
Q2 nodes are named by declaring
: nodename2 Q2! pinname;

Combinatorial Output



Registered Output

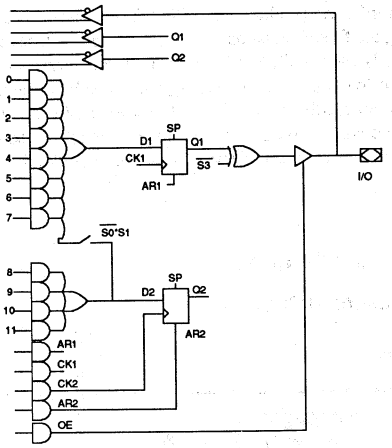


Table 4. ATV2500 Node Numbers

ATV2500 Pin Numbers	ABEL		Atmel-ABEL		CUPL		TangoPLD	
	Q1	Q2	Q1	Q2	Q1	Q2	Q1	Q2
4(1)	217	41	217	41	65	41	41	65
5(1)	218	42	218	42	66	42	42	66
6(2,3)	219	43	219	43	67	43	43	67
7(3)	220	44	220	44	68	44	44	68
8	221	45	221	45	69	45	45	69
9	222	46	222	46	70	46	46	70
11	223	47	223	47	71	47	47	71
12	224	48	224	48	72	48	48	72
13	225	49	225	49	73	49	49	73
14	226	50	226	50	74	50	50	74
15	227	51	227	51	75	51	51	75
16	228	52	228	52	76	52	52	76
24	229	53	229	53	77	53	53	77
25	230	54	230	54	78	54	54	78
26	231	55	231	55	79	55	55	79
27	232	56	232	56	80	56	56	80
28	233	57	233	57	81	57	57	81
29	234	58	234	58	82	58	58	82
31	235	59	235	59	83	59	59	83
32	236	60	236	60	84	60	60	84
33	237	61	237	61	85	61	61	85
34	238	62	238	62	86	62	62	86
35	239	63	239	63	87	63	63	87
36	240	64	240	64	88	64	64	88

Notes: 1. Due to the memory limitations of PC/MS DOS, ABEL PC versions 3.0 to 3.2 and Atmel-ABEL 1.01 do not support the macrocells associated with pin 4 and 5. These pins can only be used as inputs.
2. These same versions of ABEL and Atmel-ABEL (see above) do not support the AR terms of Q2 associated with pin 6.
3. These same versions of ABEL and Atmel-ABEL (see above) do not support the Synchronous Preset of pin 6 and 7.

ATV2500 Feedbacks

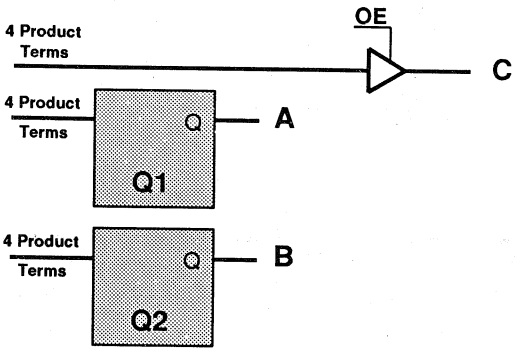
Each third party product uses a slightly different syntax for accessing the feedback paths (refer to Table 5). Whenever the Q1 register is used while the OE term is disabled or conditionally disabled (e.g. during read cycles), care must be taken to ensure the correct feedback path is used. For example, a counter can lose its count if you use the pin feedbacks rather than the Q1 register feedbacks and decide to disable the OE for the read cycle.

The current version of Tango_PLD cannot support the Q1 feedback when the I/O pin is configured as an input (OE disabled) or when OE is conditionally disabled.

This syntax may change with each new software revision. Please check with the specific software manufacturer or Atmel EPLD Applications if you experience unexpected results.

Feedback Options:

Combinatorial Output



Registered Output

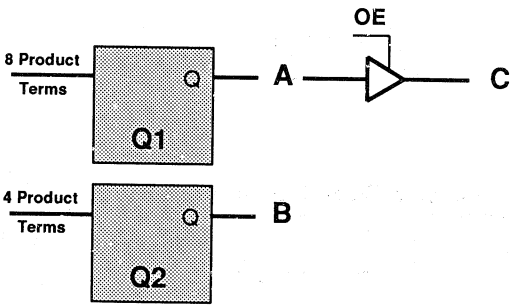


Table 5. ATV2500 Feedback Paths

		A	B	C
ABEL	Registered	pinname.Q	nodename2	pinname
	Combinatorial	nodename1	nodename2	pinname,
CUPL	Registered	pinname	nodename2	pinname.IO
	Combinatorial	nodename1	nodename2	pinname
Tango-PLD	Registered	no support	nodename2	pinname
	Combinatorial	nodename1	nodename2	pinname

Testing Non-Windowed CMOS PLDs

Atmel's testing of non-windowed CMOS PLDs is comprehensive and thorough. It is sufficient to guarantee programmability and performance. The wafer-probe test checks one-hundred percent of all memory elements for programmability. Final test of packaged units checks programming a second time. Performance testing on the "Quality Test Array" (QTA) guarantees AC test parameters. This data shows a high degree of correlation with standard array performance data.

Introduction

Atmel's corporate goal is to meet or exceed our customers' requirements one-hundred percent of the time. This means we must prove to ourselves that each product shipped will perform as specified or better.

PLDs must meet two different device requirements: they must program as a memory device, and they must function as a logic device. This requires testing all devices in two very different ways.

The programmable elements in Atmel's CMOS PLDs are UV EPROM memory cells. The AND array programs like an EPROM. UV light cannot penetrate non-windowed packages (e.g., any plastic package or solid lid ceramic package). Erasing a non-windowed EPROM element is not possible. Any testing by Atmel before shipment cannot program the main AND array or the customer cannot enter his own pattern.

Atmel's test methodology guarantees our PLDs will program and perform to the data sheet, even without programming this main AND array.

Figure 1. Non-Windowed PLD Test Flow

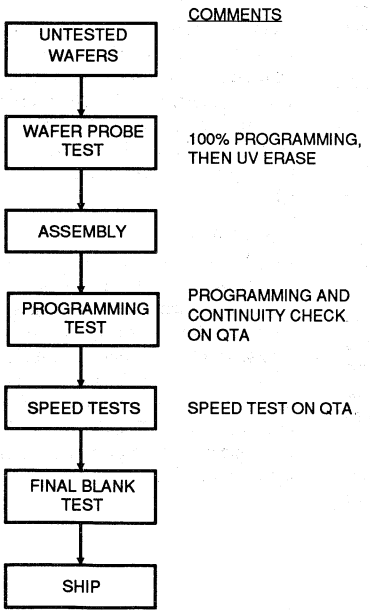
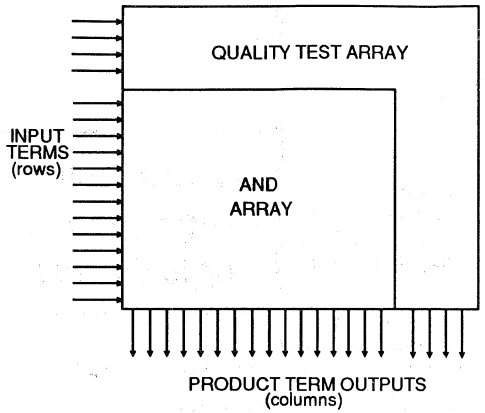


Figure 2. PLD Topography



Programming

After wafer fabrication, the first test is wafer-probe (figure 1). All PLD dice manufactured by Atmel use a similar wafer test program. This test programs one-hundred percent of the memory bits used to implement the AND array in our PLDs. This programming algorithm is more aggressive than that implemented by programming manufacturers. After verifying all bits, the wafer is then UV erased before proceeding further.

Package assembly is next. If the packaging used does not have a UV translucent window, the customer is the only one who can program the device. Atmel must guarantee performance and programming by testing other EPROM cells in the device.

These other EPROM cells are next to the main AND array. A discussion of the PLD AND array topography clarifies how we test the extra EPROM cells (figure 2).

Product term inputs enter the AND array from one end, and form the "rows" of the matrix. Product term outputs leave from the bottom— product terms form the "columns" of the matrix. On the far right of figure 2 are the Quality Test Array product terms (columns). At the top of the array are the QTA input terms (rows).

Even though wafer-probe tests all units' programming, packaged units also have their QTA terms tested. Since these terms are physically at the ends of the inputs and outputs, this test checks the integrity of these lines. The test detects any shorts or opens on the inputs or outputs. Programming these locations also provides a thorough test of the programming circuitry.

The wafer-probe test programs one-hundred percent of all locations, and the package test checks the programming circuitry for continuity and programmability.

Performance Testing

The logic test parameters divide into two groups: DC and AC test values. All of the DC test parameter tests are independent of the logic programmed into the device. This means that DC testing is the same for every PLD sold by Atmel, independent of the package used.

Every different logic implementation results in different AC performance. Atmel measures AC performance using a "worst case" pattern. This pattern is slightly different in nature for each PLD. This pattern uses every resource available in the device. Outputs can be made to switch in the same direction at the same time. The test program applies worst case combinations of input term and product term patterns to the device. Atmel collects AC data with this pattern on each UV erasable device shipped.

Non-erasable devices cannot use their main array for this test. Atmel programs a special speed test pattern into the QTA. Tests on this array measure all of the same AC characteristics as those done on erasable units. Correlations between the main array and the QTA follow.

Correlation

Three parameters measured on 26 units show a high degree of correlation between windowed PLD testing and non-windowed PLD testing. Measurements of T_{CO}, T_S, and T_{PD} show little difference between performance testing on the standard array versus performance testing on the QTA.

T_{CO} (clock to output) is independent of the memory array. The signal path is directly from the clock input buffer to all 10 flip-flops in the AT22V10, and then straight to the output buffer. The data shows a very tight distribution, and the difference in the two measurement techniques is within the accuracy of the setup (see table 1).

T_S (setup time) and T_{PD} (propagation delay) are dependent on the EPROM array. The data shows an excellent correlation, with the non-windowed test actually measuring slower than the windowed test. Atmel engineers carefully designed the quality test array to use the worst case paths for all conditions. This combination is not available to the user, but guarantees that the QTA speed path will be slower than the user's speed path (see table 2).

Summary

Atmel thoroughly tests all CMOS PLDs independent of the package used. Programming tests check one-hundred percent of the memory elements on all units shipped. Performance testing on the Quality Test Array measures all AC test parameters with "worse than" worse case conditions. Data taken with both the non-windowed and the windowed performance tests demonstrates that the non-windowed test is accurate and has extra guardband. Customers can feel confident that Atmel's PLDs meet their performance criteria independent of the package chosen.

Table 1. T_{CO} Performance Testing Comparison

Parameter Test	T_{CO} Window	T_{CO} Non-Window	Delta
Average	8.91 ns	8.68 ns	+0.23 ns
Std. Dev.	0.18 ns	0.15 ns	0.06 ns

Table 2. T_S and T_{PD} Performance Testing Comparison

Parameter Test	T_S Window	T_S Non-Window	Delta	T_{PD} Window	T_{PD} Non-Window	Delta
Average	6.80 ns	6.97 ns	-0.17 ns	13.92 ns	14.17 ns	-0.25 ns
Std. Dev.	0.09 ns	0.11 ns	0.09 ns	0.25 ns	0.25 ns	0.18 ns

Conversion of Atmel's EPLDs to ATL Series Gate Arrays

Application Specific Integrated Circuit

Application Note

Introduction

Atmel designs and manufactures complex CMOS programmable logic devices (PLDs) and high performance CMOS gate arrays. In a natural progression, Atmel now offers a seamless, direct conversion from PLD designs to our ATL Series Gate Arrays. Atmel's process converts a single PLD into a gate array that is pin-for-pin compatible. This drop-in replacement matches the exact timing of the PLD. Atmel's conversion is to a true gate array, and can integrate multiple PLDs into a single chip, something a "hard-wired" PLD cannot do. With Atmel you can prototype your ASIC in programmable logic and transfer it to a gate array for volume production, and avoid redoing the design.

Atmel's EPLD conversion process requires little or no engineering effort from the customer. This application note explains the conversion of JEDEC file based PLDs, reviews the results of a conversion and discusses when a conversion makes sense.

Figure 1. Supply Current versus Input Frequency

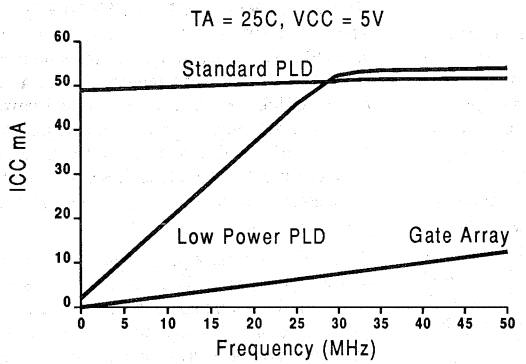


Table 1. PLD to Gate Array Conversion Methodologies

	Conversion Methodology	Gate Utilization	Timing Match	Comments
1.	Logic Synthesis	Best	Low	Best used when performance improvement is required or when several PLDs are combined.
2.	Deterministic	Moderate	Moderate	Eliminates internal timing concerns.
3.	Timing Matching	Lowest	High	Eliminates both internal and system timing concerns.

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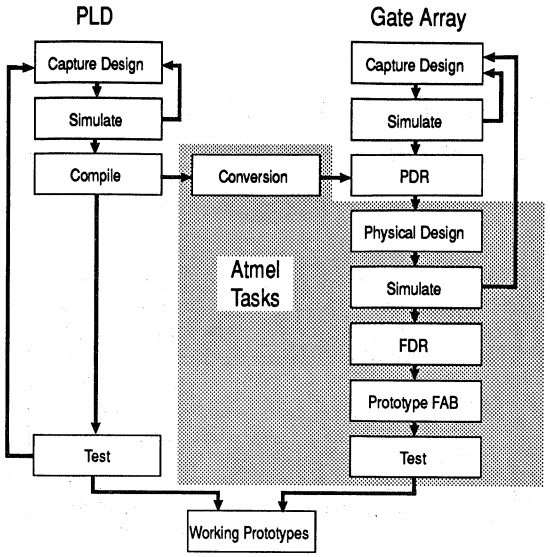
Figure 2. Design Process



Why Convert?

PLD sales have grown tremendously over the past several years because they save time and money. PLDs use inexpensive design tools on inexpensive platforms. An EPLD design takes only hours and modification is easy. As a result, a designer can implement an ASIC design and evaluate its performance in the same week. Instant feedback gives design engineers a quick way to fix system errors without additional cost. PLDs provide an ideal solution for low to moderate volume designs or for fast prototyping. Gate arrays offer superior performance, higher gate density and lower cost per gate in volume production. Gate array design tools dropped in cost in recent years, and quality third party tools have emerged. These tools still cost more than PLD tools, however. Prototypes are available in a few weeks, still longer than the several hours turnaround of a PLD.

There are four instances when converting from a PLD to a gate array offers the user a direct benefit:

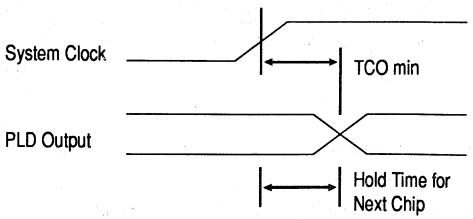
1. High Volume: If the annual volume is over 10,000 units (commercial), converting to a gate array can save money.
2. Performance: Gate Arrays have lower current requirements and offer faster speed than a PLD (see Figure 1).
3. Integration: Atmel's conversion to true gate arrays integrates several PLDs into a single chip. This requires less board space and provides a cost saving.
4. Prototyping: Using PLDs for prototyping and gate arrays for production gives the user the best of both worlds—fast design cycle times and low cost volume production.

Conversion Process Summary

Atmel's conversion process minimizes the engineering effort required from the customer. Figure 2 outlines the conversion process flow. The first requirement is a JEDEC file from ABEL, CUPL, or other JEDEC based development system. Also required are a specification and functional test vectors. The JEDEC file describes the interconnections between the PLD's logic gates. Atmel requires a block diagram representing the interconnects between PLDs to integrate two or more PLDs into a single chip.

Once we receive the required inputs, we convert the JEDEC file into an equivalent netlist in our ATL series library. After conversion, a simulation using the original test vectors verifies the gate array design. The optimization process is next. Optimization can match or improve the timing performance of the gate array with respect to the original PLD design.

Figure 3. System Timing Concerns (Positive Hold Times)



Atmel holds a Preliminary Design Review (PDR) with the customer before physical design of the chip begins. If the preliminary results satisfy the customer, he signs off the results of the converted design. From this point on the process is identical to that of a traditionally designed gate array. The next step is physical placement and routing followed by verification of the electrical design rules. Atmel uses Cadence's Verilog-XL as our golden simulator. Atmel guarantees performance equal to that predicted by Verilog-XL.

Atmel's software extracts back annotation data from the layout. A post-route timing simulation uses this data for final verification. Meeting the timing specification may require minor layout modifications. At the Final Design Review (FDR) the customer reviews and approves the post-route simulation data. After approval, mask generation and wafer fabrication occurs. Prototype deliveries can occur in as little as two to three weeks. Production deliveries can start in six weeks after customer approval of prototypes.

Conversion

Customer requirements and applications dictate which conversion technique to use:

Deterministic

PLDs have a uniform, deterministic architecture. Every signal traverses the same length path and avoids race conditions. If the converted design is a drop-in replacement, the design must meet the specifications of the original design. This includes minimum and maximum signal arrival times as well as set-up and hold times. Why is this important? An example (Figure 3) is when PLDs drive a chip with a positive hold time. A reduction in the minimum clock to output timing causes a violation of the hold time. The gate array runs faster than the PLD, but the system fails.

Atmel's software converts the PLD JEDEC file into an equivalent circuit in our 1.0-µ cell library. Using a deterministic approach, the software implements the gate array logic using blocks similar in structure to the PLD's. The software converts the JEDEC file directly into product term and sum term logic blocks. Potential timing problems disappear using this technique. The converted test vectors verify that the gate array design is functionally equivalent to the original design.

If the original PLD design is completely synchronous, timing optimization finds the minimum propagation delay for each signal path. The optimizer makes the maximum signal arrival time for each path in the gate array equal to that path in the PLD. Adding additional gates to the product and sum terms matches the propagation delays of the gate array with those of the original PLD.

Synthesis

PLD compilers offer behavioral level simulation. Logic synthesis maps the behavioral level design into a functionally equivalent circuit in our gate array library. The process of synthesis is relatively easy and offers maximum gate utilization and performance. This technique is best when converting several PLDs into a single gate array or when the customer requires a performance improvement.

Figure 4. T_S (ns) versus VCC (V)

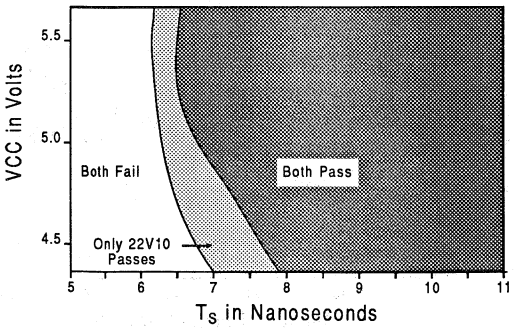


Figure 5. T_{CO} (ns) versus VCC (V)

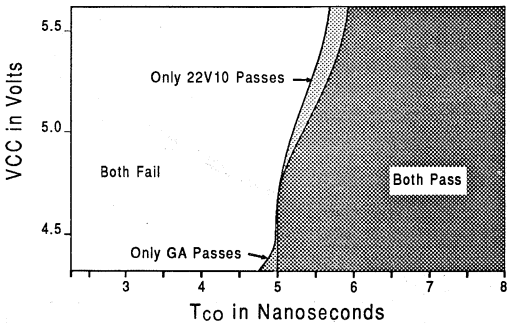


Figure 6. T_{PD} (ns) versus VCC (V)

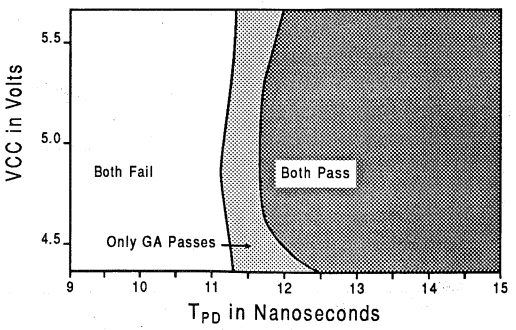


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Figure 7. Normalized T_{CO} versus Temperature

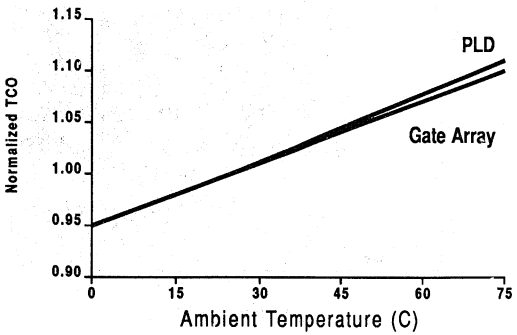


Figure 8. Normalized T_S versus Temperature

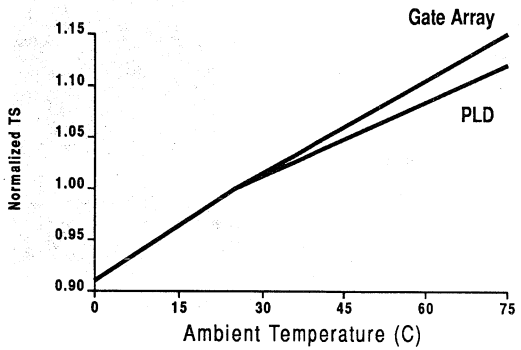
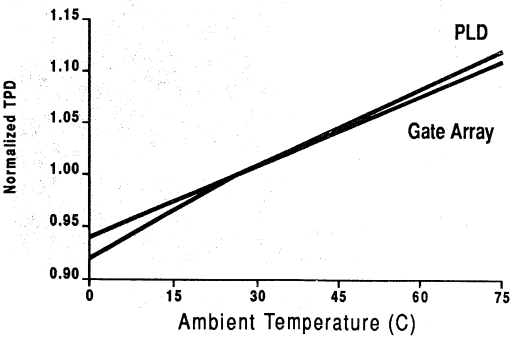


Figure 9. Normalized T_{PD} versus Temperature



Atmel uses Synopsys as our synthesis tool. Synopsys analyzes the behavioral description of the PLD and synthesizes a gate level description in the Atmel cell library. The resulting netlist is functionally equivalent to the original PLD. Synopsys also optimizes the design for speed, power usage and gate count.

Synthesis reduces the PLDs to the smallest possible gate array implementation. Since the design structure is not the same or deterministic, the timing will be different than the original design.

Conversion Results

The following figures show timing data for PLDs converted into gate arrays. Figure 4 shows a "schmoo" of T_S (set-up time) versus VCC. The schmoo compares an AT22V10-15DC with an ATL4. The ATL4 contains the same logic converted with timing matching. The lightly shaded region shows where the 22V10 is slightly faster. On the whole, the performance is similar, with the 22V10 less than 1 ns faster at any voltage.

Figure 5 shows T_{CO} versus VCC. The results are the same. T_{CO} is an important parameter, as mentioned before. Figure 6 shows T_{PD} versus VCC.

Figure 7 shows the T_{CO} results versus temperature. The clock to output timings are within 2% of each other over the commercial temperature range. Figures 8 and 9 show the temperature dependence for T_S and T_{PD}.

How to Figure Utilization

Utilization results from completed conversions give us the following formulas. For an ATL4, and *deterministic conversion*, the percentage utilization is:

$$\%\ utilization = (0.15\,x + 0.08\,y + 1.5\,z)\ \%$$

where x is number of pterms, y is number of pins, and z is number of registers.

For an ATL4, and *timing matching conversion*, the percentage utilization is:

$$\%\ utilization = (0.35\,x + 0.08\,y + 1.5\,z)\ \%$$

PLD compilers provide data on product term usage. With this, and the number of pins and registers, we can predict gate utilization for specific designs.

For gate comparison purposes, 1% of an ATL4 corresponds to approximately 31 gates. The formulas for gates used are:

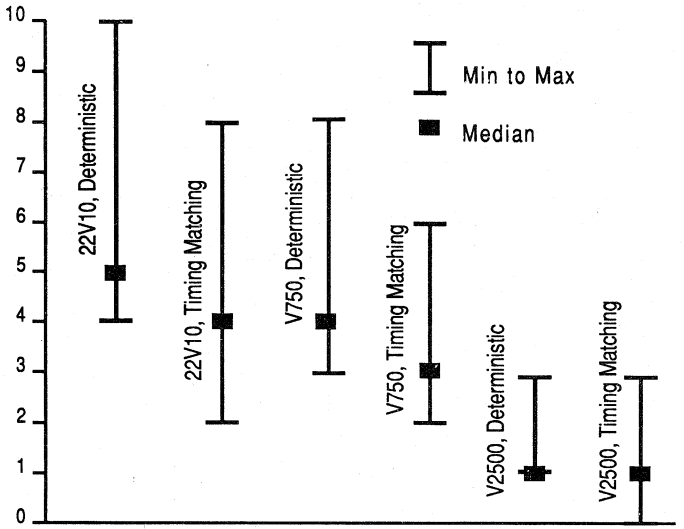
For *deterministic conversion*:

$$number\ of\ gates\ used = 4.7x + 2.5y + 46.7z$$

For *timing matching conversion*:

$$number\ of\ gates\ used = 10.9x + 2.5y + 46.7z$$

Figure 10. Number of Specific PLD Designs which will fit in an ATL4 (Min, Median, Max)



Figuring How Many will Fit

Using these formulas, an accurate estimate for specific designs is possible. Figure 10 shows a range for the number of specific PLD designs which will fit into an ATL4. Numerous customer designs analyzed by Atmel provided the data. Designs based on multiple PLDs often have a wide range of PLD utilization per device. The number shown as the "median" is a good estimate when considering converting multiple PLDs into a gate array. Individual PLD designs will lie between the shown minimum and maximum. The maximum number is usually a function of the number of I/O pins required.

Summary

Atmel offers three types of conversion from PLDs to gate arrays. Timing matching and deterministic conversions reduce the potential timing problems possible with conversion. Measured results show an excellent correlation between the PLD and gate array timings. Formulas exist to help determine how many PLDs can fit in a gate array. All that one needs is a JEDEC file with good test vectors, and the conversion process can begin.

Alternate Sourcing Of Existing ASIC Designs

Introduction

Atmel's flexible design system supports customers with varied design interface requirements. The system accepts designs from existing netlists, from schematics, and from netlists synthesized from HDL or VHDL descriptions. This application note describes the netlist translation path which allows customers to automatically map existing ASIC designs into Atmel's gate array family for a pin-for-pin compatible, drop-in replacement.

Atmel can translate designs from most major ASIC suppliers. The designs are mapped into Atmel's ATL series gate array family which is described in Table 1. This family provides a range of usable gate counts up to 80,000 gates and pin counts up to 360 pins.

These gate arrays are fabricated in Atmel's advanced CMOS technology, the features of which are summarized in Table 2. The design can be optimized for speed or power consumption, modified to add logic or memory functions or replicated for a pin-for-pin, drop-in replacement.

Table 1. ATL Series Gate Arrays

Device Number	Maximum Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate(1) Speed
ATL4	4,100	2,600	68	60	434 ps
ATL10	10,000	6,500	124	116	434 ps
ATL20/20C	22,000	12,000	144/160	136/138	434 ps
ATL40	40,000	22,000	180	168	434 ps
ATL60	57,000	30,000	224	208	434 ps
ATL130	131,000	67,000	256	236	434 ps
ATL160	157,000	80,000	360	320	434 ps

Note: 1. Nominal 2 Input Nand Gate With a Fan Out of 2

Table 2. AT22000 CMOS Wafer Process

Feature	AT22000
Drawn Gate Length	1.0 µ
Effective Gate Length	0.8 µ
Metal Levels	2
First Metal Pitch	3.0 µ
Second Metal Pitch	3.4 µ
Silicide Process	Yes
Supply Voltage	+5.0 V, +3.3 V

Atmel Design Translation

The Atmel ASIC Design Translation Flow is presented in Figure 1. This translation flow creates a design which replicates the original design in form, fit, function and performance and verifies that design through simulation and testing of engineering samples. In order to execute the design translation, the data in Table 3 are required from the customer.

Table 3. Customer Design Inputs

Description of the cell library used in the original design
Netlist representing the original design
Test vectors, print on change in ASCII or TSSI™ format
Critical path description
Description of asychronous paths and previous timing problems (if any)
Back annotation delay data for the original design
Device specifications
Sample devices

The first step in the design flow is translation of the original design into the Atmel library. This is accomplished using the netlist provided by the customer and Synopsys™ to recreate the original design. The design is then mapped into Atmel's cell library. Static path timing analysis is performed for both the recreated original design and the mapped design and a comparison is done to identify any significant timing differences. Particular attention is paid to the critical paths identified in the customer supplied data package.

The second step in the design flow is a comprehensive logic and timing simulation using the Verilog-XL™ simulator. This analysis is done by comparing the simulation data to the device requirements, as defined by customer supplied test vectors and timing specifications. If a sample of the original design is available, characterization data from the sample will also be compared to translated design simulation results and specifications. During this phase, test vectors are automatically translated to provide vectors for simulation and Automatic Test Program Generation. A Preliminary Design Review (PDR) is held with the customer at the completion of this phase.

The final design phase is physical layout of the device on the selected Atmel gate array and computer verification of the design. Automatic place-and-route software is used to lay out the design using the Atmel netlist created during translation. Back annotated interconnect data is extracted and supplied to Verilog-XL™ for a final post-route timing simulation. Any layout revisions to meet timing requirements are completed and the design is computer checked to insure that the layout meets all design requirements. A Final Design Review (FDR) is held with the customer at the completion of this phase.

With the customer's concurrence, the design is released for engineering sample fabrication and characterization. Samples are delivered to the customer along with the design files and elecrical test data for evaluation, system verification and qualification.

Optional Services

In addition to direct translation, Atmel can provide the following services:

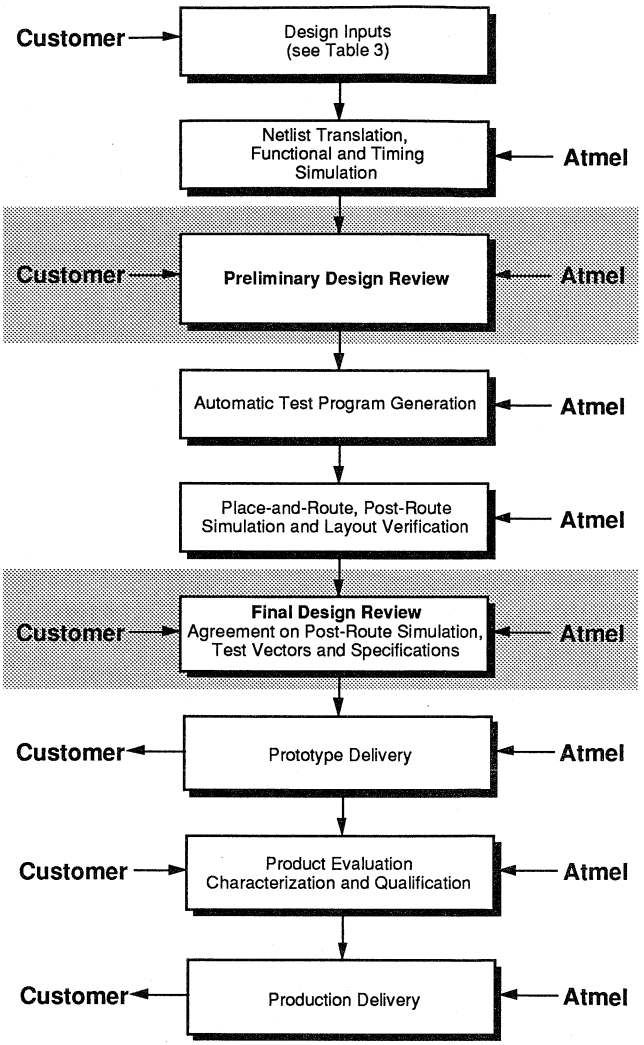
Design Optimization: After initial mapping into the Atmel cell library, the translated design can be optimized for performance (speed), or cost (minimum gate count). This optimization is accomplished using logic synthesis during the translation phase. In addition, logic changes can be made or additional logic and/or memory can be added.

Customer Simulation: In addition to the standard design files, Atmel can provide schematics and timing libraries in a variety of formats to allow the customer to perform in-house simulation and fault grading.

Fault Grading: Atmel can fault grade the translated design to measure fault coverage in the design.

Testability: The Atmel cell library has been configured to automatically allow conformance to the IEEE 1149.1 Test Architecture Standard (JTAG). Other boundary and serial scan techniques are also available.

Figure 1. Design Translation Flow



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Interfacing the AT76C10/E to a Microcontroller

CMOS Programmable Amplifier Delay Equalizer

Application Note

Introduction

The AT76C10/E is a programmable gain amplifier integrated with a programmable telephone line group delay equalizer on a single chip. Its serial interface enables it to be packaged in an economical and space-saving 16-pin DIP. The AT76C10/E is especially suited for modems and data communications equipment where it can compensate for line gain variations and group delay distortions. In the E^2PROM version of the chip, the AT76C10E, a particular gain or delay configuration can be stored in the device's nonvolatile memory and recalled later by the user.

The programmable gain and group delay responses are controlled and configured by a serial 7-bit configuration code. The purpose of this application note is to illustrate how this serial configuration can be accomplished in a microcomputer environment, more specifically, utilizing a microcontroller (the Intel 8031AH) to interface to the AT76C10/E. Such an interface enables the gain and delay responses to be changed or updated in real-time (for the AT76C10) as well as saved into the E^2PROM (for the AT76C10E).

As shown in Figure 1, the Intel 8031AH, an 8-bit latch, a transmission line receiver, and external memory form a complete and versatile system to generate control and data bits for the AT76C10/E. An RS-232C cable can connect this system to the serial port of a microcomputer (e.g. IBM PC) or TTY terminal. The serial port transmits data to the microcontroller, which, under software control, outputs them as serial bits to the AT76C10/E for controlling the gain and delay outputs as desired by the user. As will be explained below, an evaluation board implementing the system just described has been developed by Atmel Corporation following the guidelines in this application note.

The Hardware

The 8031AH has four 8-bit I/O ports: P0, P1, P2, and P3. Ports P0 and P2, however, are used for external memory addressing when external memory is present (as is the case here) and are thus unavailable as general-purpose I/O ports. This leaves all of the 8 bits of port P1 and five bits of port P3 available for I/O. P1.0, P1.1, and P1.2, are used to produce respectively, via software instructions, the signals $\overline{CS}$, $\overline{WE}$, and DIN necessary to program the AT76C10/E.

The 8-bit latch acts as the low-order address latch/data buffer for the signals between the P0 I/O port of the microcontroller and the external memory. The line receiver enables the microcontroller to receive data signals from the microcomputer or TTY terminal via the RS-232C link.

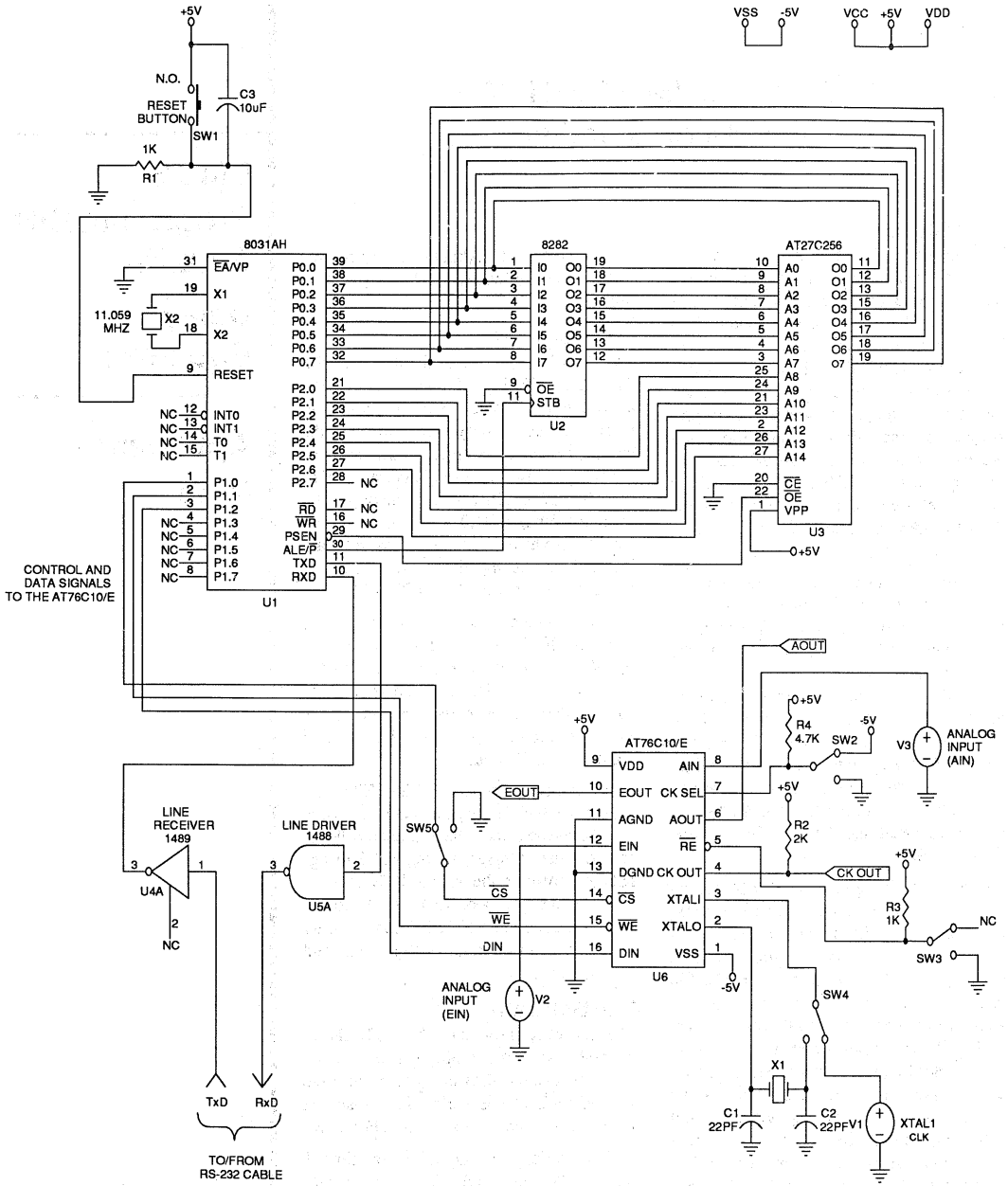
External memory consists of the AT27C256 EPROM, which houses the system software. This firmware directs the microcontroller to send out the necessary timing and data signals to configure the AT76C10/E. If additions or changes need to be made to the firmware code the AT27C256 can be easily erased via ultra-violet (UV) light and reprogrammed.

The Software

The software programs the 8031AH to generate the correct timing waveforms and to strobe desired data bit patterns into the AT76C10/E. This is achieved as illustrated by the programming flowchart in Figure 2.

First the serial port data register and timer 1 need to be initialized with proper values

Figure 1. Microcontroller Interface to the AT76C10/E



The Software (Continued)

depending on desired transmission parameters and baud rate. A 9600-baud data transmission rate has been used in this application. As soon as the accumulator receives a character from the keyboard the data is sent out bit by bit (LSB first) as data bits through the carry flag to the serial data input pin of the AT76C10/E. Appropriate delays and specific bit-manipulating instructions then control and synchronize the transitions of $\overline{CS}$ and $\overline{WE}$ with the data bits so that the writing waveforms conform to timing specifications defined in the device data sheet. Seven rising edges of $\overline{WE}$ strobe in a complete data word in a single write cycle.

The complete programming code is given in Figure 3. It directly implements the flowchart in Figure 2.

Using The AT76C10/E Evaluation Board

As previously mentioned, an evaluation board integrating the hardware and software subsystems covered in this application note is available from Atmel Corporation. This board includes a 5.25" disk (IBM-PC format) with gain/delay programming menus and is designed to enable the user to quickly and easily evaluate the functionality and performance of the AT76C10/E through a standard serial interface to an IBM PC or compatible computer. Through the board one can cycle through all the individual gain/delay steps in each of the two amplifiers and the group delay equalizer.

Figure 2. 8031 Programming Algorithm

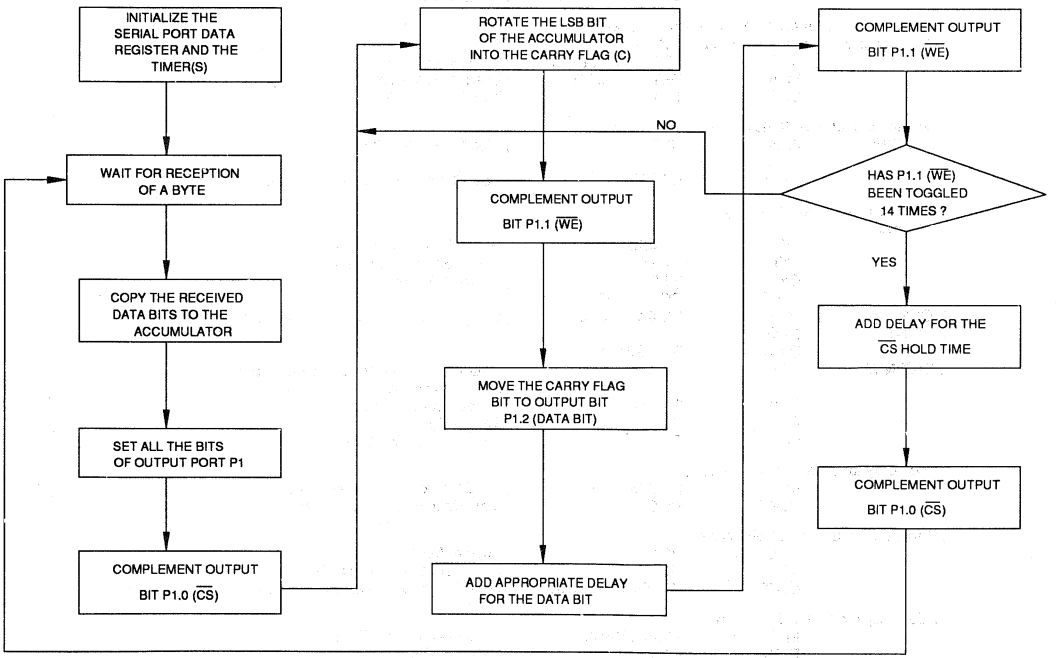


Figure 3. Program Code for AT76C10/E

```
;*****************************************************************
;*                                                               *
;*                  8031 program for the AT76C10/E               *
;*                        Evaluation Board                       *
;*                                                               *
;*                                                               *
;*                  Written by: Ta Wei (David) Lee               *
;*                    (C) 1988  ATMEL Corporation                *
;*                                                               *
;*****************************************************************
;
; 8031 control program for programming the AT76C10/E

; Constant Definitions:
ST          EQU     0FFH
RST         EQU     00H
DONE        EQU     14              ; 14 edges (falling and rising) for WEB
UARTMODE    EQU     01010000B       ; Set UART for: start, 8 data bits, stop
TMODLOAD    EQU     00100001B       ; Initialization word for the TMOD register
PCON        EQU     87H             ; Power Control Register
RELOAD      EQU     -3              ; Reload rate for 9600 baud
DATADLY     EQU     3H              ; Delay for a valid data bit
CSBHDLY     EQU     4H              ; Delay for CSB hold time
CSBIDLE     EQU     2               ; Delay before starting another CSB cycle
WEBIDLE     EQU     1               ; Delay before starting another WEB cycle

; Start of the program:
START:      ORG     00H
            LJMP    BEGIN

; Initialize the serial port data register for 8-bit UART mode:
BEGIN:      ORG     100H            ; Start of the code
            MOV     P3,#ST          ; Set the entire P3 I/O register
            MOV     PCON,#RST       ; No double baud rate wanted !
            MOV     SCON,#UARTMODE  ; Initialize the register

; Initialize timer 1 for an auto-reload rate of 32x9600 Hz.
; (T0 is used as a cascaded 16-bit counter.)
            MOV     TMOD,#TMODLOAD  ; Initialize the TMOD register
            MOV     TH1,#RELOAD     ; Load the reload rate
            SETB    TR1             ; Turn Timer 1 ON

; Receive a character (byte) from the serial port:
RECEIVE:    JNB     RI,$            ; Wait for a character
            CLR     RI
            MOV     A,SBUF          ; Copy the byte to the accumulator

; Start the programming sequence:
; First cycle:
            MOV     R1,#RST         ; Reset the WEB counter
            MOV     P1,#ST          ; Set all bits of output port 1
            CPL     P1.0            ; Toggle CSB low
            AJMP    CONTINUE
MORE:       MOV     R2,#WEBIDLE     ; Delay to generate the proper WEB high time
AGAIN1:     NOP
            DJNZ    R2,AGAIN1
CONTINUE:   RRC     A               ; Rotate the LSB bit of the accumulator
                                    ; into the carry flag
            MOV     P1.2,C          ; Output one data bit
            CPL     P1.1            ; Toggle WEB
            INC     R1              ; Increment the WEB counter

; Add delay for a data bit to stabilize:
            MOV     R0,#DATADLY     ; Load the delay into the counter
            DJNZ    R0,$            ; If not done yet, wait some more...

; Continue the data bit strobe cycle:
            CPL     P1.1            ; Toggle WEB
            INC     R1              ; Increment the WEB counter
            CJNE    R1,#DONE,MORE   ; Have 7 data bits been strobed in ?

; Add delay for the CSB hold time:
            MOV     R0,#CSBHDLY     ; Load the delay for TCH
            DJNZ    R0,$            ; Delay finished ?

; End of one programming cycle:
            CPL     P1.0            ; Toggle CSB high
            MOV     R2,#CSBIDLE     ; Waiting time for another cycle start...
AGAIN2:     NOP
            DJNZ    R2,AGAIN2
            AJMP    RECEIVE         ; Wait for another byte reception
            END     START           ; End of the program
```

A/D Conversion Using the AT76C120

How the AT76C120 Works

The AT76C120 simultaneously samples and holds both analog inputs, ADIN1 (Channel-1) and ADIN2 (Channel-2), once every CONV period. The AT76C120 then performs an A/D conversion of both samples and returns the two resulting 16-bit or 18-bit 2's complement codes at the serial data output pin DOUT during the following CONV clock period.

Selecting Which Channel's Data Comes Out First

Channel-1 output data will be returned first, during CONV "low" (and Channel-2 data will be returned second, during CONV "high") when a logic "1" is present at the input SEL1. Conversely, a logic "0" at the input SEL1 will cause Channel-2 data to be returned first, during CONV "low" (and CHANNEL-1 data to be returned second, during CONV "high").

Required Clocking for the AT76C120

The AT76C120 requires two clocks, SCLK and CONV, for proper operation:

- SCLK is the system clock and can have a maximum frequency of 6.144 MHz. It takes 64 SCLK cycles for the AT76C120 to perform one A/D conversion, and 64 more SCLK cycles for the digital data to be output (while a new sample is being converted).
- CONV is the convert clock, and its period corresponds to one A/D conversion. It should equal 64 SCLK cycles. Normally, CONV is derived from SCLK using a negative-edge triggered divide-by-64 counter, and both SCLK and CONV run continuously. In this mode, the AT76C120 will be sampling continuously at frequencies up to 96 kHz. Since CONV initiates conversions, however, it is possible to use CONV as a trigger for one-shot sampling.

Using the AT76C120 A/D Converter in One-Shot Mode

The AT76C120 can be used in a single-shot mode for acquiring data. To get one sample from each of the two channels, you need one conversion cycle to sample and convert the ADIN1 and ADIN2 inputs, and another conversion cycle to clock out both Channel 1 and Channel 2 digital codes. A total of two CONV periods and 128 SCLK cycles are required.

To use the AT76C120 in single-channel single-shot mode, you need one conversion cycle to sample and convert the ADIN1 or ADIN2 inputs, and another half cycle to clock out the Channel 1 or Channel 2 digital code. Only 1.5 CONV periods, and 96 SCLK periods are required.

One-shot sampling can be implemented by holding CONV low until a sample is desired. Note that while waiting to sample, SCLK can be either running or stopped. When a sample is desired, both SCLK and CONV are brought high, initiating a sample-and-hold of the analog inputs. SCLK should be clocked 32 times, at which point CONV is brought low. SCLK should then be clocked 32 more times, completing the first conversion cycle. CONV should then be brought high, and SCLK should be clocked 32 times, shifting out the first channel's digital code. For single-channel sampling, this would be the end and CONV should once again be brought low until a new sample is desired, and the process is repeated. For dual-channel sampling, CONV should be brought low, and SCLK should be clocked 32 more times, shifting out the second channel's digital code, and completing the second conversion cycle. CONV should be held low until a new sample is desired, at which time the process repeats.

CMOS Dual-Channel 16/18-Bit A/D Converters

Application Note

Analog Interface

Due to the high sampling rate of the AT76C120, little if any anti-alias filtering is required for most industrial applications. For high performance Digital Audio applications, external Anti-Alias Lowpass or Bandpass Filters, shown as AAFs in the Sample Connection Diagram, should be used to eliminate signals outside the desired passband. Low noise op amps with low output impedance such as the OP27 should also be used to supply the analog inputs.

Digital Interface

The AT76C120 uses a single multiplexed serial data output pin, DOUT. CH-1 and CH-2 data bits are synchronized with SCLK, and are available during either the "high" or the "low" period of CONV. CONV, if equal to SCLK divided by 64, makes a transition from "high" to "low" or vice versa after the LSB is shifted out of DOUT. This allows the serial data to be latched easily into most popular D/A converters or digital signal processors by using CONV rising or falling edges. For applications with an 8-bit, 16-bit, or 32-bit host microprocessor, 16- or 18-bit wide parallel data may be desired, and serial-to-parallel conversion will be needed. In such cases, SCLK can be used to shift in the serial data from DOUT, and CONV can be used as a latch to output the parallel data.

More on Converting the Output Data from Serial to Parallel

It may be desirable to convert the AT76C120's serial data to parallel data. This may be achieved using 18 shift registers and 18 output latches, or several serial-to-parallel converters. Additionally, there may be a need to provide control signals to interface the parallel data with a microcontroller.

An easy way to integrate the entire serial-to-parallel conversion, complete with control signals for interface, is to use an Atmel ATV2500 Erasable Programmable Logic Device. This device has the necessary I/O pins, logic terms, and registers to easily and conveniently interface the AT76C120 with most microcontrollers and DSP devices.

The ATV2500 is capable of latching in all 16/18 data bits that have been output serially from the AT76C120. All 16/18 bits can be presented in parallel on ATV2500's output pins. Additionally, the ATV2500 can transfer this same data in 8-bit bytes, complete with handshaking, to a host device.

Power Supply Decoupling and Grounding

To obtain the highest performance possible with the AT76C120, critical signal paths, power supply lines, and ground planes on the circuit board should be laid out carefully to minimize noise coupling or aliasing into sensitive analog paths. As illustrated in the diagram showing a Sample Connection for Typical Applications (figure 1), a separate AVCC line decoupled to AGND with a tantalum capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C120. Similarly, a separate analog ground return, AGND, which is connected to the most quiet point in the system ground plane, should be used.

For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath pins 1 to 6 and pins 19 to 24.

High frequency noise on the power and ground lines can be aliased into the passband by the sampling action of the AT76C120. If a switching power supply has to be used, both AVCC and AGND need to be isolated from the system supplies with inductors of appropriate values.

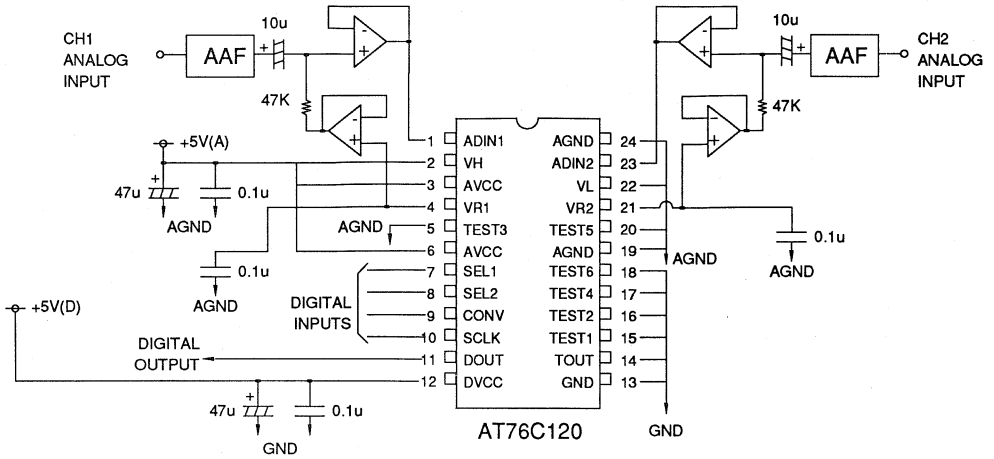
Evaluating the AT76C120 with the Atmel AT76C120 Demonstration Board

The AT76C120 Dual-Channel 16/18-Bit A/D Converter may be evaluated using the Atmel AT76C120 Evaluation Board (see figure 2). This board can perform analog input signal conditioning, timing waveform generation, and serial-to-parallel data conversion. Evaluation requires a low-ripple, low-noise power supply, a low-distortion signal source, a clock source, and a digital signal processor.

The AT76C120 Evaluation Board requires a +15-volt and -15-volt analog power supply, and a +5-volt digital power supply. Voltage reference circuitry has already been included on the board. The user may build filters and buffers for the analog inputs in the analog patch area provided. The required clocking for the system may be generated using the SCLK BNC, or by inserting a clock oscillator in the socket provided. An Atmel ATV750 EPLD programmed as a divide-by-64 counter generates the convert clock CONV. An Atmel ATV2500 Erasable Programmable Logic Device (EPLD) programmed as a serial-to-parallel converter places the 18-bit digital output codes from the AT76C120 at the pins of a 25 x 2 header. Because the ATV2500 is programmable, the digital interface may be modified by the user to meet specific interfacing needs, including the ability to program in control and handshake signals to facilitate data transfer to a host processor.

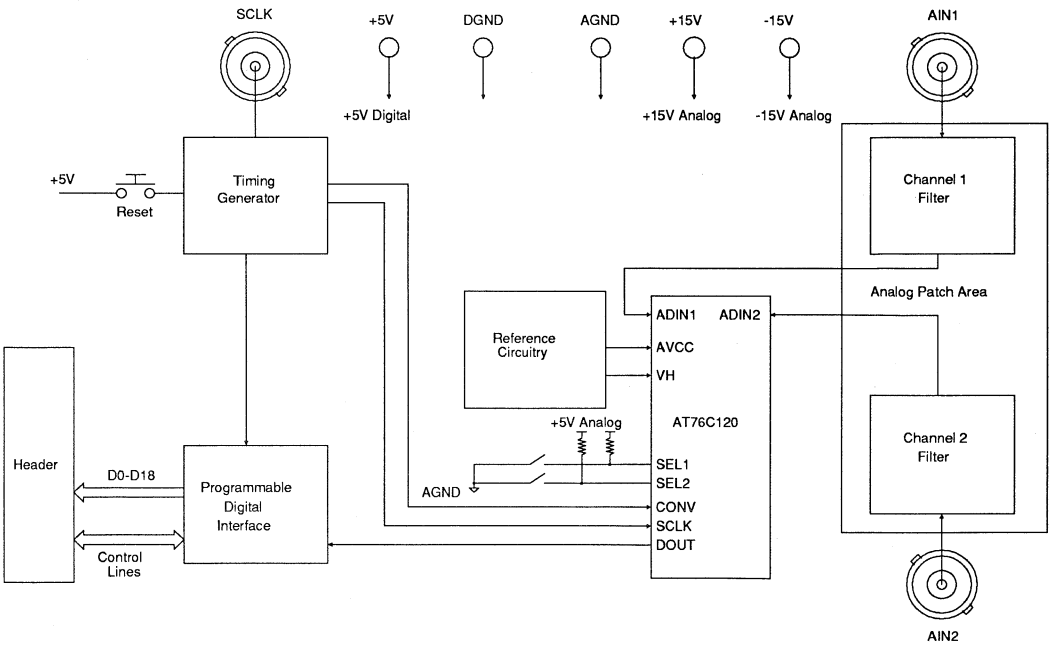
Dynamic evaluation of the AT76C120 is one application for the AT76C120 Evaluation Board. After building the appropriate filters in the analog patch areas, a spectrally pure sinusoid may be applied to the analog inputs of the AT76C120. Consecutive data samples may be collected as they appear at the header, and FFT may be performed to produce spectral information on the converter, such as signal-to-noise and signal-to-distortion ratios.

Figure 1: Sample Connection for Typical Application



Notes: 1. AVCC, AGND, +5V (A)- analog supply
2. DVCC, GND, +5V (D)- digital supply
3. Use high quality 0.1 µF ceramic chip capacitors

Figure 2: AT76C120 Evaluation Board



12

AT76C176A Color Palette DAC

110 MHz Monolithic CMOS Hi-Res Video Color Palette

Application Note

The Atmel family of 6-bit video color palette (color look-up table) devices include the AT76C176A (28-pin), the AT76C176A1 (32-pin), and the AT76C176A2 (44-pin). They are designed for the IBM VGA 8514/A, XGA graphics standards and beyond. The VGA standard is already well supported by the software industry, but there are significant applications developing beyond standard VGA requiring higher resolutions. The Atmel devices can meet this emerging need. This application note will explore features of this family's members which can be fully utilized by graphics hardware designers and systems designers for implementing high-performance graphics solutions. It will also examine some design-related issues concerning such implementations.

SPEED: The AT76C176A/A1/A2 are available in these different speeds: 50 MHz, 66 MHz, 80 MHz, and 110 MHz. The speed refers to the maximum pixel clock frequency at which the device can be driven. Basically, the higher this frequency the greater the number of pixels that can be displayed on a CRT (cathode-ray tube) screen for bit-mapped graphics.

The equation used to calculate the color palette pixel clock rate required for a particular range of display resolution is as follows:

PCLK = 1.35 (HORIZONTAL RESOLUTION × VERTICAL RESOLUTION × VERTICAL SCAN RATE)

The horizontal resolution means the horizontal number of pixels and the vertical resolution means the vertical number of pixels. The vertical scan rate term refers to the vertical video scanning frequency of CRT monitors, which can vary between 43 Hz and 72 Hz but is typically 60 Hz, while the 35% factor refers to the portion of each frame time taken up by the horizontal and vertical retrace. For interlaced displays the vertical scanning rate becomes 43 Hz instead of 60 Hz. This means the screen image would be refreshed 43 times a second.

For example, if a non-interlaced resolution of 1024 x 768 refreshed at 60 Hz is desired, the required pixel clock rate would be:

$$PCLK = 1.35\ (1024 \times 768 \times 60)$$
$$= 63.7\ MHz$$

To appreciate the magnitude of these frequencies, one must look at the graphical applications which these devices are capable of displaying. Standard VGA specifies resolution modes such as 320 x 200 pixels with 256 possible simultaneous colors and 640 x 480 pixels with 16 colors, whereas presently available Super-VGA (and VESA or Video Electronics Standards Association) specifications call for a standard resolution of 800 x 600 in 16 or 256 simultaneous colors. These colors are normally available from a total palette of 262,144 colors.

50 MHz: At this speed the color look-up table device can drive RGB monitors up to a maximum of 1024 x 768 pixels, 256 colors, in interlaced mode. At the time of this writing this is the typical maximum resolution displayable by some of the best selling Super-VGA and multisync-type monitors. At this device speed virtually all the requirements called for by the VGA and Super-VGA specifications can be met.

66 MHz: At this frequency the color palette can drive display monitors up to 1024 x 768 pixels, 256 colors, in non-interlaced mode. A non-interlaced monitor costs more than an interlaced monitor capable of the same resolution, but it can be more pleasing to the eye, since the screen "flicker" associated with interlaced monitors is eliminated. The "flashing" phenomenon present in interlaced monitors is due to the fact that only alternate scan lines are updated during every frame (vertical refresh), rather than every single scan line.

80 MHz: At this speed the top displayable resolution reaches 1024 x 960 pixels, 256 colors, in non-interlaced mode with a 60-Hz refresh rate, virtually approaching worksta-

tion-quality graphics. This speed is also suitable for driving 1024 x 768 non-interlaced monitors with a higher refresh rate of 72 Hz. At 72 Hz, screen flicker will not be detected even under fluorescent lighting conditions, which typically induce flicker perceptions. Mainstream personal computer software can be written to take advantage of these high resolutions with a resulting hardware / software cost-performance ratio several times less expensive than similar workstation solutions.

110 MHz: Finally, at this speed an eye-pleasing top resolution of 1280 x 1024 pixels (non-interlaced mode) can be achieved, with the device still capable of simultaneously displaying 256 different colors on-screen. This type of resolution, which even exceeds some workstation-level monitors, would be ideal for applications such as CAD drawings, computer modeling, scanned images, video animation, and imaging, with resulting photo-realistic images and shaded renderings. As a quick comparison, at 1280 x 1024 there are 1,310,720 pixels of information on-screen compared to 307,200 pixels at the normal 640 x 480 VGA resolution, which is a factor of four greater! With the rapidly emerging software markets of windows-based graphical user environments and multimedia applications for personal computers, the Atmel color palette devices providing such a high resolution would bring unprecedented workstation-grade graphics performance to personal computer users at an affordable cost.

POWER SAVINGS: In the PLCC and LCC versions of the AT76C176A family there is a power-down mode, an especially useful feature in laptop and notebook computers. When activated by software, this mode turns off the video DACs and the internal clock circuitry of the device, causing total device current consumption to be dramatically reduced from its normal operating value. The power-down mode will afford a battery-operated system a much longer per-charge life, since current consumption can drop to as low as 100 µA, compared to 150 mA or more in active mode.

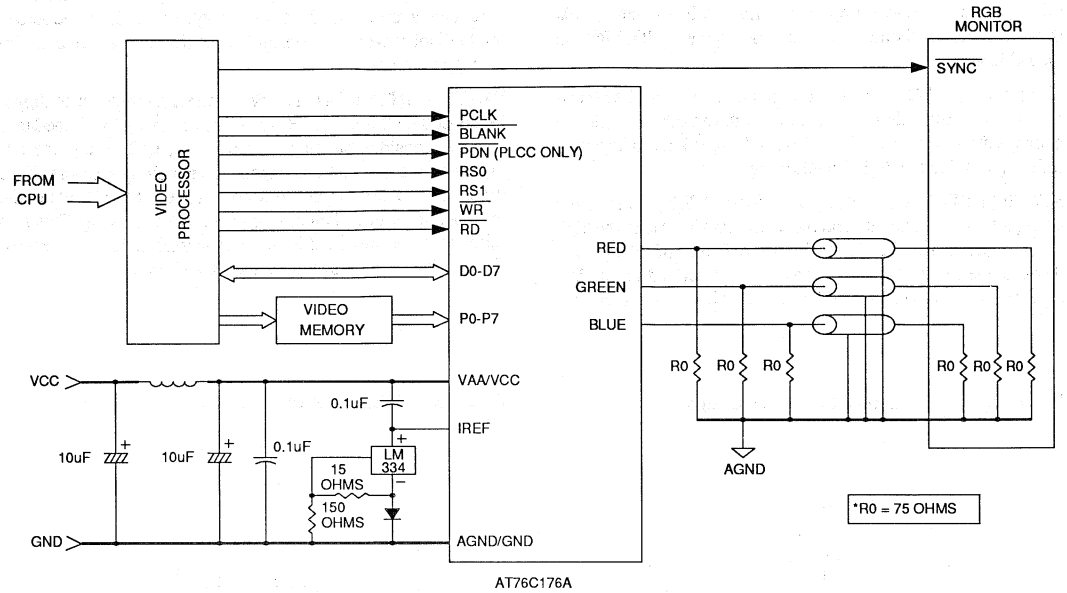
MILITARY APPLICATIONS: All the members of the AT76C176A family are processed up to full military specifications. This leads to consistent high reliability and quality. It also means that many previously expensive, proprietary military graphics subsystem designs can be easily upgraded to a cost-effective graphics solution supported by a wide array of standard off-the-shelf software written for the VGA standard. For example, military situational and awareness displays can be directly driven by Atmel color palette devices. The use of colors can dramatically add more meaningful information to the operators and users of visual equipment in the areas of avionics, logistics, radar and sonar systems, satellite communication, tactical warfare, and many others. Even if only a single primary color is used (e.g. GREEN) different shading levels could relay different objects very effectively.

RANGE OF COLORS: As discussed in the SPEED section, the Atmel color palette devices can simultaneously display a maximum of 256 distinct colors on-screen *throughout* their speed range. This means 8 bits are allowed to define the color of each pixel. These 256 colors are available at any time from a total group of 262,144 colors. The specific set of 256 colors shown at any given instant can be easily changed through software. For most personal computer-based applications software, the availability of 8 bits per pixel and 262,144 colors to choose from is more than adequate.

PACKAGING: The AT76C176A1 and the AT76C176A2 are the 32-pin and 44-pin PLCC versions of the AT76C176A, respectively. These packages are specially suited for the latest surface-mounted PCB manufacturing techniques and can significantly decrease the amount of real-estate space required to implement an efficient graphics solution. Furthermore, these PLCC packages, with very short pins, can minimize the inductance inherently present in integrated circuit device pins, leading to sharper reproduction of colors with less distortion in analog displays. Other packaging such as LCC are also available.

The next section highlights design issues relevant to system and graphics subsystem designers. Also shown is a sample connection for the Atmel color palette in a typical design.

Figure 1. Sample Connection for Typical Application



System Implementation Considerations

POWER SUPPLY DECOUPLING AND GROUNDING: To obtain the cleanest possible analog outputs from the AT76C176A, digital noise coupling into the analog signal paths needs to be minimized. The video data paths, power supply lines and ground planes on the circuit board should be laid out carefully to reduce noise coupling. As illustrated in Figure 1 showing a Sample Connection for Typical Application, a separate VAA line decoupled to AGND with an electrolytic capacitor in parallel with a smaller ceramic chip capacitor should be used for the analog circuits on the AT76C176A. Similarly, a separate analog ground return, AGND, which is connected to the lowest impedance point in the system ground plane, should be used.

LAYOUT: For best results, four layer PC boards with separate ground and power supply planes are recommended. The AGND plane should be laid out as an island or tub underneath the AT76C176A. All video frequency signal traces should be kept as short as possible to minimize radiation and all decoupling capacitors should be placed as close to the AT76C176A as the layout rules permit.

Noise and transients on the power and ground lines can be coupled or aliased into the video circuits by the switching action of the AT76C176A. For applications at 66 MHz and above, it may be necessary to isolate both VAA and AGND from the system supplies with inductors of appropriate values.

CURRENT REFERENCE: The IREF pin in the Atmel devices determines the maximum full scale output of the video DACs and is designed to source current with reference to the positive supply rail. The required current to produce a 0.7-volt DAC full-scale output level into a doubly-terminated 75-ohm load, as specified in the data sheet, is -8.88 mA. In order to generate this current reference two approaches are suggested here: a current- source design and a voltage-reference design.

As shown in Figure 2, the first approach is based on the LM334Z adjustable current source device. In this design the LM334Z is operated in its zero temperature coefficient mode, resistor RSET determines the reference current drawn from the color palette, and resistor R1 and the silicon diode provide compensation against temperature variations. Decoupling capacitors C1 and C2 are recommended for avoiding changes in the current reference due to possible VCC or VAA variations within the operating frequency bandwidth. RSET should be a precision resistor, preferably with a 1% tolerance.

Figure 3 illustrates the voltage-reference approach. The use of a TL431C precision voltage regulator or an equivalent device is recommended. In this design the TL431C acts as a shunt regulator to provide a constant current sink. RSET again determines the amount of current drawn from the Atmel part and should be a precision resistor, while R1 limits the current flowing into the cathode terminal of the TL431C.

VIDEO INTERFACE: The Red, Green and Blue video outputs are designed to drive doubly terminated 75 ohm lines. To minimize ringing due to impedance mismatch, 75 ohm +/- 1% thin film resistors should be placed close to the AT76C176A on the PC board.

To comply with FCC RF emission regulations, ferrite beads can be inserted at the video outputs to limit the amount of high frequency emission. The AT76C176A is designed to produce very little high frequency digital feedthrough.

SYSTEM TIMING: The pixel clock, PCLK, controls the timing of the color palette and the video DACs. Due to the high pixel frequency capabilities of the Atmel family of color palette devices, the pixel clock requirements as described in the data sheet should be carefully met. Setup and hold time requirements with respect to PCLK and duty cycle limits for PCLK should be strictly adhered to. For example, if the setup or hold times of the pixel inputs are violated, certain groups of pixels on the screen might display wrong colors and cause the appearance of an incomplete picture.

DIGITAL INTERFACE: When the high impedance digital inputs of the CMOS AT76C176A are driven by low impedance sources, considerable ringing can occur, which may degrade high video rate operation. Impedance matching resistors of the order of 50 ohms can be inserted in series at the inputs to the Pixel Address and Blanking inputs to reduce ringing. This also minimizes the amount of high frequency emission due to excessively high slew rates at the video data inputs.

Figure 2. Current-Source Reference Design

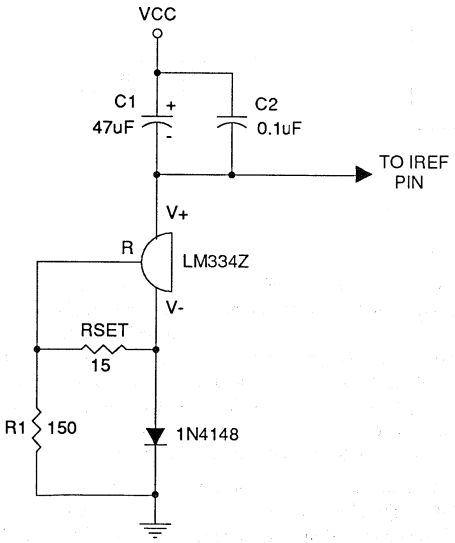
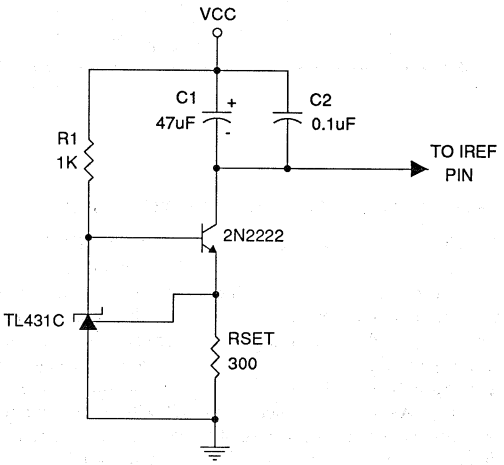


Figure 3. Voltage-Reference Design



Contents

Section 13

Quality and Reliability

Continuous Improvement System

Introduction

When one of the recipients of the 1989 Malcolm Baldridge National Quality Award accepted his award, he stated: "We realize that we are in a race without a finish line." The goal is "to improve constantly and forever the system of production and service, to improve quality and productivity, and thus constantly decrease costs."

The journey of continuous improvement involves the use of various techniques such as statistical process control (SPC), statistical design of experiments (DOE), quality functional deployment (QFD), just in time (JIT), and many others.

The mind-set to use these techniques and to support the requirements of a continuous improvement system is just as important as the tools themselves. This is the key responsibility of the executives and managers and employees of Atmel Corporation.

Our use of these techniques *throughout* the Corporation and not just in manufacturing is proof of Atmel's commitment to continuous improvement. For example, it is just as important to properly enter a customer's order as it is to manufacture it. Errors in either process result in a dissatisfied customer.

Statistical Process Control (SPC)

SPC can be divided into either statistical or non-statistical techniques. Several statistical techniques involve the mathematical portrayal of data in graphical form to display whether a process is *in control* or *out of control* (see Figure 1). Although this sounds complicated, the procedures are very easy for operators to follow.

Other statistical techniques involve determining whether a process is capable of statistically meeting the specification limits or not. Usually called the capability indices of the process, these *figures of merit* for processes are becoming widely accepted.

The non-statistical techniques are steps in problem solving. These begin with methods to collect and portray data to achieve an understanding of the process. Checklists, trend charts, and histograms are good examples of these techniques (see Figure 2).

Figure 1. Examples of process control charts

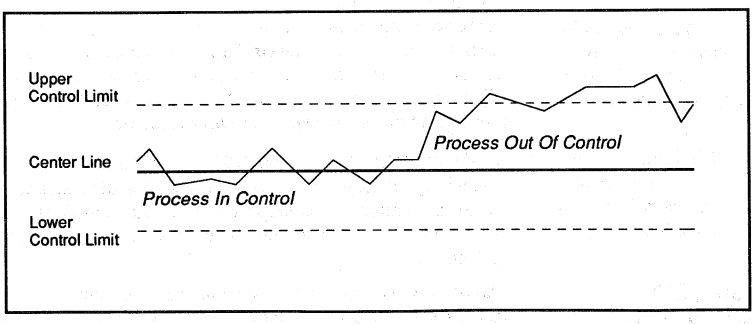
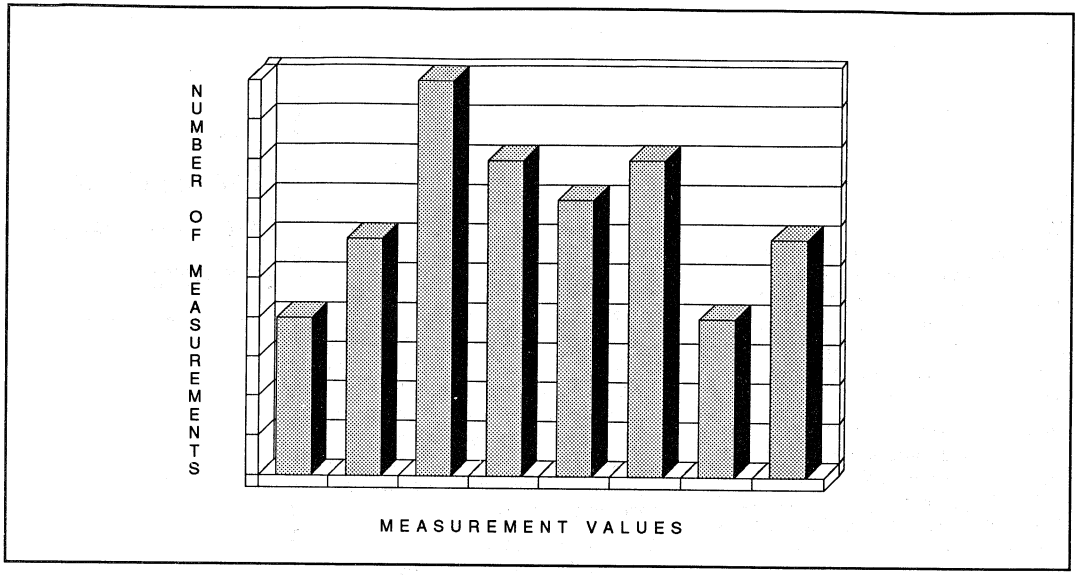


Figure 2. Example of a process histogram



The non-statistical problem solving techniques include the Pareto chart. The Pareto chart reduces the number of problems down to the *significant few* that contribute the majority of the problems.

Once those significant few are identified, the use of the Cause and Effect diagram identifies the probable causes of the problem and becomes the outline for solving it.

Statistical Design Of Experiments (DOE)

The DOE technique has been used for many years by the agricultural and chemical industries. Only recently has it made its presence felt in the *high-tech* industries.

It is perfectly suited to this industry because it has the capability to handle large numbers of variables simultaneously and to determine statistically significant variables, interactions between variables, and the amount of variation they can cause in a process or product.

When DOE is coupled with computer-aided design and process models, it can predict these relationships and outcomes without running actual experiments. This in turn reduces the time and cost of designing new products and processes or improving existing ones.

Quality Functional Deployment (QFD)

The best controlled and capable process is only as good as the product that is designed to go through it. If the design does not meet the customer's needs to begin with, there is nothing the process can do to improve it. And that is where QFD steps in.

QFD is a procedure which involves the customer in the definition and design of a product. The customer is a key member of the company team which includes marketing, design & development, manufacturing and quality departments.

The key to this technique is looking at the inter-relationships between critical variables controlled by each member of the QFD team early in the design process. Identifying and taking action on these variables enhances the design and insures that "glitches" are eliminated.

Just-In-Time (JIT)

Continuous improvement can achieve reduced production cycle times and and inventory levels. However, without a *system* to plan and oversee these reductions, the existing system may not adjust to the improvements. A JIT system insures that excess production time and inventory levels are reduced.

Consortium for Continuous Improvement

Atmel is a participating member of a consortium of major semiconductor companies. Its purpose is to create guidelines and workshops for implementing a continuous improvement system.

The consortium will publish a continuous improvement document as well as accompanying workshop materials.

Malcolm Baldridge National Quality Award

One of the best guides for company commitments towards continuous improvement lies within the criteria for the Baldridge Award. The Baldridge criteria are not a set of tools or methodologies for improvement, but rather an assessment of a company's continuous improvement system.

The major criteria evaluated by the Baldridge committee are:

- Customer Satisfaction
- Corporate Leadership
- Strategic Quality Planning
- Quality Assurance of Products and Services
- Quality Results
- Human Resource Utilization
- Information Analysis

Atmel's management team is integrating the Baldridge criteria into its continuous improvement system and the Company has announced that it will apply for the Baldridge Award.

Conclusion

Atmel is committed to the process of continuous improvement. This is most clearly displayed by its corporate-wide implementation of continuous improvement, its dedication to win the Baldridge Award, and its participation in the continuous improvement consortium.

An Executive Decision

Atmel's corporate goal is to meet or exceed our customers' requirements 100% of the time.

Atmel guarantees and tests product quality at all levels and all critical paths in the manufacturing process. Quality assurance and control are the responsibility of the executive staff reporting directly to the chief executive officer. The concern with quality begins with the initial product inception, and never ends. Atmel quality is critical for the entire life of any system that our products become a part of.

Design For Quality And Reliability

The Atmel design staff emphasizes quality and reliability throughout the design cycle. Design rules are established by experiment to insure manufacturability and reliable performance over time. All devices are designed with proprietary anti-latchup structures to eliminate the necessity of using epitaxial starting materials with their inherent higher defect densities. Special electrostatic discharge circuits are incorporated to protect package pins during handling and insertion.

Each product family has specific quality and reliability issues that require special design consideration. Nonvolatile memories that depend on charge storage must allow for the testing of charge retention to insure long term data retention. E^2PROM devices are electrically alterable, and additional circuits are incorporated to maintain data integrity during times of external signal instability (such as system power-up or failure). High performance CMOS analog designs depend on stable threshold voltage and transistor gains and must be designed to minimize manufacturing variations. Since operation frequency is a critical parameter in an EPLD device, Atmel incorporated two levels of metal interconnect into its process to allow the use of conservative transistor technology.

Eliminating inadvertent writes might be considered a system design issue, but Atmel designed write protect features into its E^2PROM family. Active on board circuits sense VCC and prevent writes for 5 ms after VCC has increased above 3.8 volts. Three line write control (CHIP ENABLE, WRITE ENABLE, AND OUTPUT ENABLE must all be held in their active states to initiate a write) and noise pulse filters (pulses less than 15 ns in duration are ignored) on the control lines are incorporated to prevent false write commands. A software key (user activated) can require that a specific sequence of addresses and data be issued to the chip before a write is activated.

The "Bathtub" Failure Curve

It is well known that integrated circuits exhibit a classical "bathtub" failure curve (Figure 13.1). Early relatively high failure rates (Phase 1) are due to process anomalies and are found during Atmel's outgoing production test. Devices which are shipped to customers then exhibit a long period of stable very low failure rates (Phase 2) which are random in time and occurrence. Finally, other failure modes will become predominant (such as metal electromigration, voltage threshold shifts, or moisture related corrosion) and the failure rate will again increase as the chip "wears out" (Phase 3).

Atmel production test flows have been developed to insure that Phase 1 failures are found before shipment. Special test structures are incorporated on chip which correlate to these failures. Specific temperature, voltage, and time dependant tests are performed to guarantee the quality of the outgoing products.

Atmel guarantees non-volatile data retention for greater than 10 years. A high temperature bake has been shown to be a good stress test for data retention[1], and 100% of Atmel's products are tested in this way. In addition, periodic 1000 hour monitor tests routinely show retention life times in excess of 50 years.

Since E^2PROM memory circuits have high transistor densities, Phase 2 failures are often dominated by write cycle induced oxide integrity faults. Atmel has incorporated internal error correction into its E^2PROM product line to minimize this type of failure. Each byte (8 bits) of data is internally stored as a 12-bit word generated using a modified Hamming code, and any single bit failure is automatically corrected during the read cycle. Failure rates for chips incorporating internal error correction are improved dramatically. For example, at the point where the cumulative failure rate for a 64K bit uncorrected E^2PROM has reached 0.1 (10% of the chips have exhibited failures), an AT28C64 corrected circuit would exhibit a failure rate of only 2 parts per million.

Phase 3 failure modes are dependant on the system application of the specific circuit. Long term reliability studies and failure analyses are used to identify potential failure modes and control them through processing, layout rules, packaging, and design. To illustrate, all E^2PROM's exhibit a finite number of write cycles (defined as endurance) due to electrons slowly becoming trapped in the tunneling oxide. The number of write cycles that occur before this failure mode predominates is dependant on such things as the cleanliness of the process and the thickness and integrity of the oxide film. The Atmel process is based on a "thin" (less than 100 Angstroms) tunnel oxide to minimize the effects of trapping and thus increase the number of cycles.

Manufacturing For Quality and Reliability

All Atmel products are manufactured to the standards of Military Standard 883C, Class B through wafer fabrication and assembly as shown in Figure 13.2. The products then follow different test flows that correspond to the different classes of products that Atmel offers.

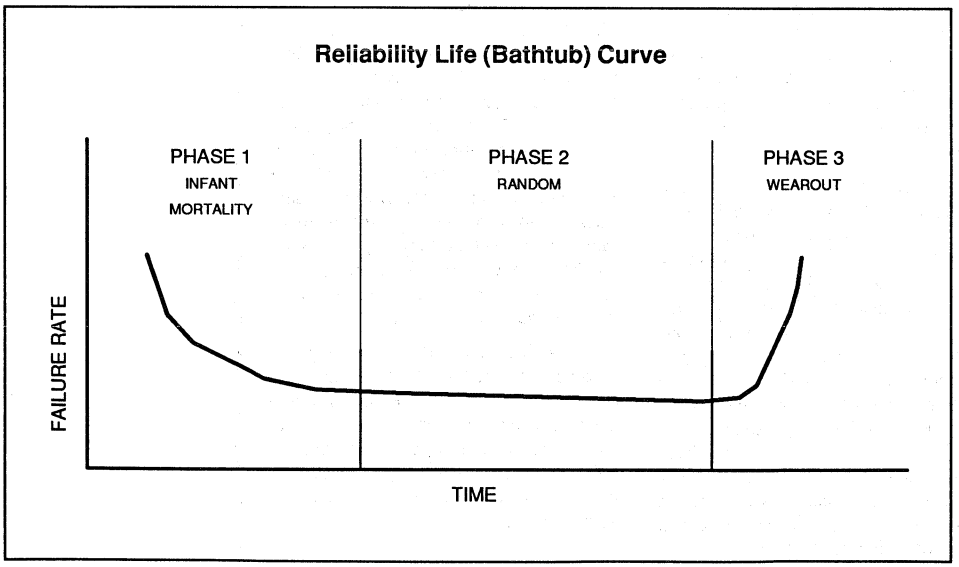
(1) Commercial Grade. This product follows Test Flow (1), Figure 13.3 and is guaranteed over the temperature range of 0°C to +70°C.

(2) Industrial Grade. This product follows Test Flow (2), Figure 13.4 and is guaranteed over the temperature range of -40°C to +85°C.

(3) Quality Enhancement Flow. This product follows Test Flow (3), Figure 13.5 which specifies burn-in of industrial product in a standard flow.

(4) Military Grade. Three classes of military products are offered by Atmel (MIL-STD-883C, Class B standard product, Standard Military Drawing (SMD) product, and Source Control Drawing (SCD) product). The Military Section discusses test procedures for these products in detail.

Figure 13.1



Note: 1. R. E. Shiner, J. M. Caywood, B. L. Euzent, "Data Retention in EPROMs", Proceedings International Reliability Physics Symposium 18, (1980), P. 238.

The Payoff

The focus of Atmel's quality and reliability efforts is the customer and his system. The common goals of highest field reliability and lowest system life cycle cost are achieved through close working relationships using programs such as "ship to stock", "just in time", and "failure trend analysis". Under these programs incoming Atmel circuits go straight to the customers' workfloors— they do not go through an incoming inspection cycle. This, of course, lowers manufacturing costs and is a testimony of the trust that has been established. In addition, long term field failures are analyzed so that corrective action plans can be implemented. Atmel has developed programs such as these with many major customers.

Figure 13.2

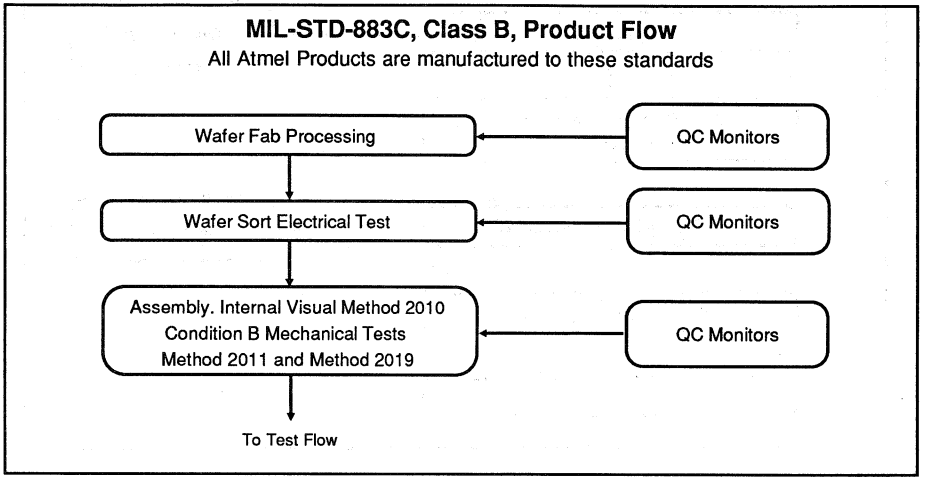


Figure 13.3

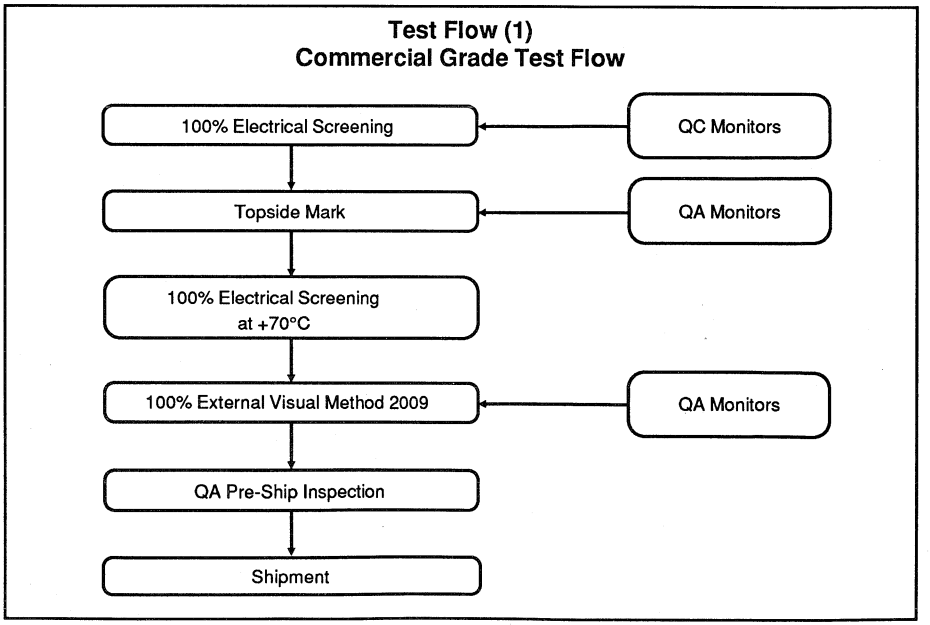


Figure 13.4

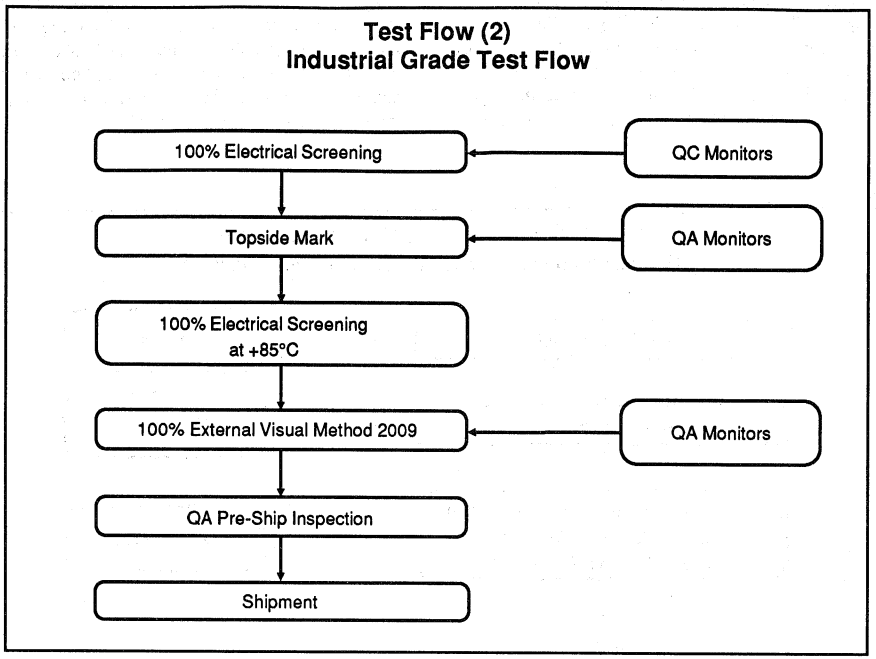
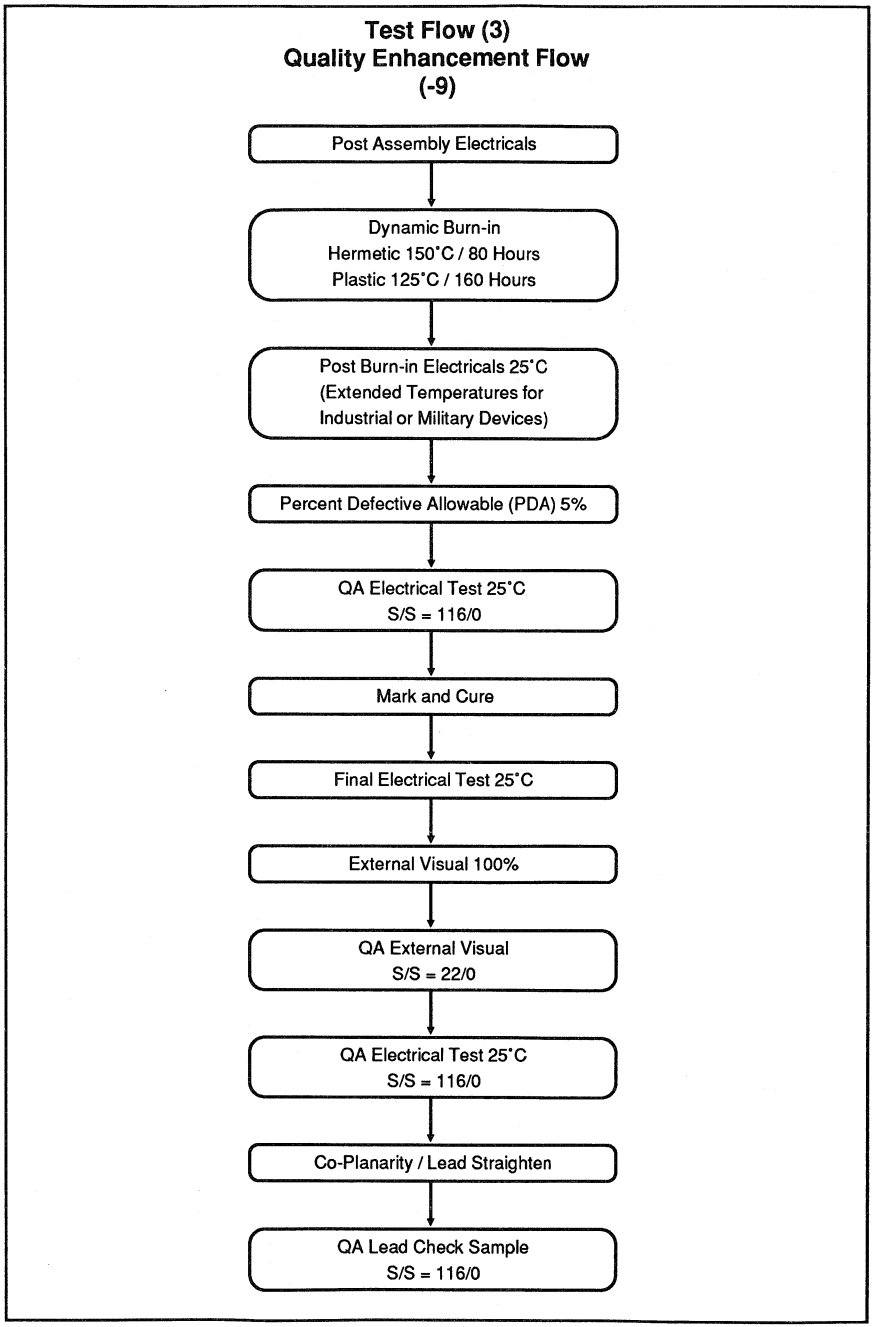

Test Flow (2)
Industrial Grade Test Flow
100% Electrical Screening
QC Monitors
Topside Mark
QA Monitors
100% Electrical Screening
at +85°C
100% External Visual Method 2009
QA Monitors
QA Pre-Ship Inspection
Shipment

Figure 13.5


Test Flow (3)
Quality Enhancement Flow
(-9)
Post Assembly Electricals
Dynamic Burn-in
Hermetic 150°C / 80 Hours
Plastic 125°C / 160 Hours
Post Burn-in Electricals 25°C
(Extended Temperatures for
Industrial or Military Devices)
Percent Defective Allowable (PDA) 5%
QA Electrical Test 25°C
S/S = 116/0
Mark and Cure
Final Electrical Test 25°C
External Visual 100%
QA External Visual
S/S = 22/0
QA Electrical Test 25°C
S/S = 116/0
Co-Planarity / Lead Straighten
QA Lead Check Sample
S/S = 116/0

ATMEL

Contents

Section 14

Military

Program Overview

All Atmel products are manufactured to the standards of Military Standard 883C, Class B through wafer fabrication and assembly, as shown in Figure 14.1. Military products then follow the test flow shown in Figure 14.2.

Quality Conformance Inspection Data

As shown in Table 14.1, Atmel performs Groups A, B, C, and D tests in compliance with Military Standard 883C, Class B. Groups A and B are performed on each inspection lot for MIL-STD-883C, Class B products. Groups C and D are periodic inspections as defined in MIL-M-38510. Preconditioning data, Group A, Group B, Group C, and Group D generic data are available for customer procurement.

Military Product Classes

Atmel offers three classes of military products:

(1) MIL-STD-883C, Class B products are fully compliant to MIL-STD-883C Paragraph 1.2.1, with no exceptions. A Certificate of Compliance (C of C) is enclosed with each shipment of MIL-STD-883C, Class B product.

(2) Standard Military Drawing (SMD) products are fully compliant to MIL-STD-883C Paragraph 1.2.1 with optional additional tests as specified in the applicable Standard Military Drawing as approved by DESC. Table 14.2 lists currently approved Atmel SMD parts, organized by Atmel part type. Table 14.3 lists currently approved Atmel SMD parts, organized by SMD number.

(3) Source Control Drawing (SCD) products are fully compliant to MIL-STD-883C Paragraph 1.2.1 with optional additional tests as specified by the specific customer specification. Atmel must review and accept a customer Source Control Drawing prior to order acceptance to assure compliance.

Figure 14.1

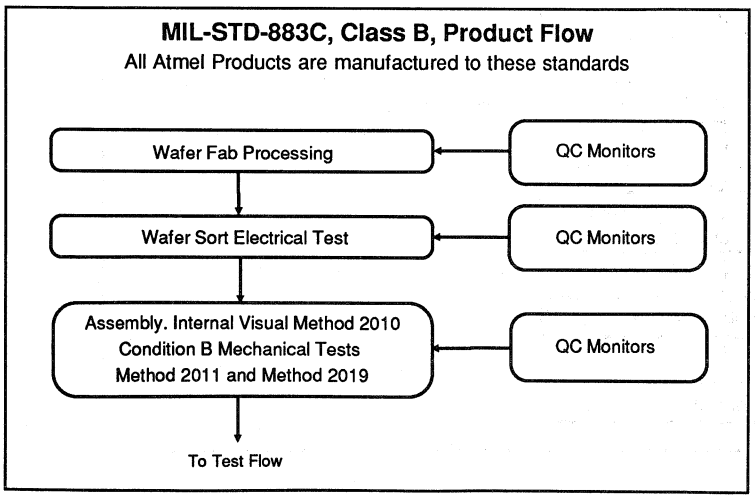


Figure 14.2

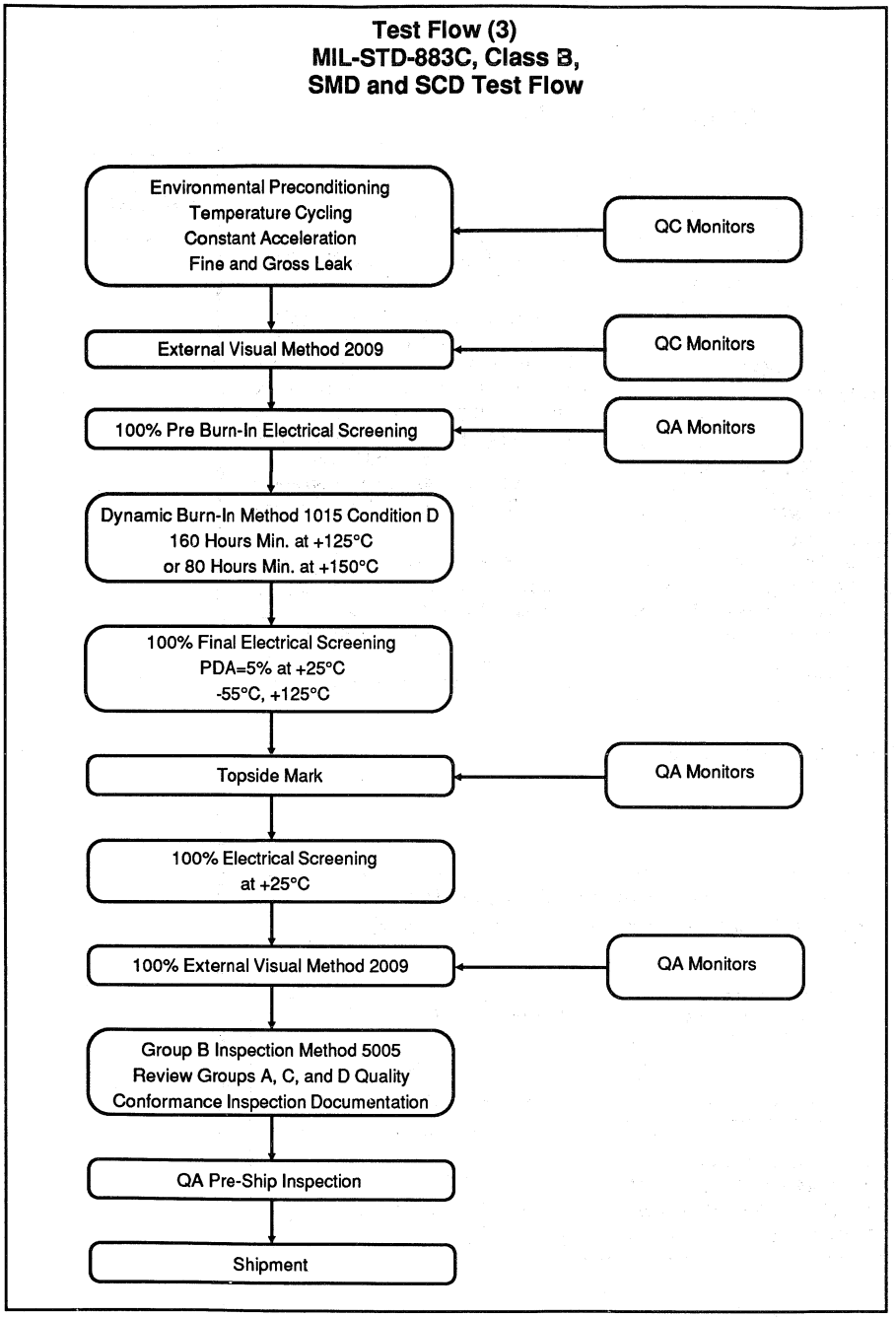

Test Flow (3)
MIL-STD-883C, Class B,
SMD and SCD Test Flow
Environmental Preconditioning
Temperature Cycling
Constant Acceleration
Fine and Gross Leak
QC Monitors
External Visual Method 2009
QC Monitors
100% Pre Burn-In Electrical Screening
QA Monitors
Dynamic Burn-In Method 1015 Condition D
160 Hours Min. at +125°C
or 80 Hours Min. at +150°C
100% Final Electrical Screening
PDA=5% at +25°C
-55°C, +125°C
Topside Mark
QA Monitors
100% Electrical Screening
at +25°C
100% External Visual Method 2009
QA Monitors
Group B Inspection Method 5005
Review Groups A, C, and D Quality
Conformance Inspection Documentation
QA Pre-Ship Inspection
Shipment

Table 14.1 Military Standard 883C, Class B Tests

Group A: Electrical Tests

Performed On Each Lot

Screen	MIL-STD-883C Method 5005 Table 1 Subgroups	LPTD
Static Tests at +25°C	1	2
Static Tests at +125°C	2	2
Static Tests at -55°C	3	2
Dynamic Tests at +25°C	4	2
Function Tests at +25°C	7	2
Function Tests at +125°C	8A	2
Function Tests at -55°C	8B	2
Switching Tests at +25°C	9	2
Switching Tests at +125°C	10	2
Switching Tests at -55°C	11	2

Group B: Assembly Integrity Tests

Performed On Each Lot

Screen	MIL-STD-883C Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 2			
Resistance to Solvents	2015	Top and Bottom Marks	4(0)
SUBGROUP 3			
Solderability	2003	+245°C +/-5°C	10
SUBGROUP 5			
Bond Strength	2011	Condition D	15

Group C: Die Related Tests

Performed Per MIL-STD-883C Paragraph 1.2.1

Screen	MIL-STD-883C Test Method	Conditions	LTPD
SUBGROUP 1			
Steady State Life Test	1005	Condition D	5
End Point Electricals	5005	As specified in the applicable device specification	

Table 14.1 Military Standard 883C, Class B Tests *(continued)*

Group D: Package Related Tests

Performed Per MIL-STD-883C Paragraph 1.2.1
By Package Type, Assembly Location, and Exterior Lead Finish

Screen	MIL-STD-883C Test Method	Conditions	Quantity (Accept No. or LTPD)
SUBGROUP 1			
Physical Dimensions	2016	MIL-M-38510, Appendix C	15
SUBGROUP 2			5
Lead Integrity	2004	Condition B2 (Condition D for LCC)	
Seal: Fine	1014	Conditon A or B	
Seal:Gross	1014	Condition C	
SUBGROUP 3			15
Thermal Shock	1011	Condition B, 15 Cycles	
Temperature Cycling	1010	Condition C, 100 Cycles	
Moisture Resistance	1004	10 Cycles	
End Point Electricals	5005	As specified in the applicable device specification (within 42 hrs)	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1004 and 1010	
SUBGROUP 4			15
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E, 30 KG., Y1	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination	1010		
End Point Electricals	5005	As specified in the applicable device specification	
SUBGROUP 5			15
Salt Atmosphere	1009	Condition A	
Seal: Fine	1014	Condition A or B	
Seal: Gross	1014	Condition C	
Visual Examination		Per Visual of Method 1009	
SUBGROUP 6			3 (0) or 5 (1)
Internal Water Vapor Content	1018	5,000 PPM Maximum Water Content at 100°C	
SUBGROUP 7			15
Adhesion of Lead	2025	Glass Frit Seal Only	
Finish		(LTPD for Number of Leads)	
SUBGROUP 8			5 (0)
Lid Torque	2024	Glass Frit Seal Only	

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT22V10

Generic Number	Standard Military Drawing Number				Description	
C22V10	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-87539	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-87539	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-87539	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-87539	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87539 **01 KX**	AT22V10-25YM/883
	5962-87539 **01 LX**	AT22V10-25DM/883
	5962-87539 **01 3X**	AT22V10-25LM/883
	5962-87539 **02 KX**	AT22V10-30YM/883
	5962-87539 **02 LX**	AT22V10-30DM/883
	5962-87539 **02 3X**	AT22V10-30LM/883
	5962-87539 **03 KX**	AT22V10-40YM/883
	5962-87539 **03 LX**	AT22V10-40DM/883
	5962-87539 **03 3X**	AT22V10-40LM/883
	5962-87539 **04 KX**	AT22V10-20YM/883
	5962-87539 **04 LX**	AT22V10-20DM/883
	5962-87539 **04 3X**	AT22V10-20LM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT22V10L

Generic Number	Standard Military Drawing Number				Description	
C22V10L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88724	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88724	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88724	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88724	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88724 **01 KX**	AT22V10L-25YM/883
	5962-88724 **01 LX**	AT22V10L-25DM/883
	5962-88724 **01 3X**	AT22V10L-25LM/883
	5962-88724 **02 KX**	AT22V10L-30YM/883
	5962-88724 **02 LX**	AT22V10L-30DM/883
	5962-88724 **02 3X**	AT22V10L-30LM/883
	5962-88724 **03 KX**	AT22V10L-40YM/883
	5962-88724 **03 LX**	AT22V10L-40DM/883
	5962-88724 **03 3X**	AT22V10L-40LM/883
	5962-88724 **04 KX**	AT22V10L-20YM/883
	5962-88724 **04 LX**	AT22V10L-20DM/883
	5962-88724 **04 3X**	AT22V10L-20LM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT22V10 OTP

Generic Number	Standard Military Drawing Number				Description	
C22V10 OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88670	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88670	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-88670	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88670	04	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88670 **01 KX**	AT22V10-25FM/883
	5962-88670 **01 LX**	AT22V10-25GM/883
	5962-88670 **01 3X**	AT22V10-25NM/883
	5962-88670 **02 KX**	AT22V10-30FM/883
	5962-88670 **02 LX**	AT22V10-30GM/883
	5962-88670 **02 3X**	AT22V10-30NM/883
	5962-88670 **03 KX**	AT22V10-40FM/883
	5962-88670 **03 LX**	AT22V10-40GM/883
	5962-88670 **03 3X**	AT22V10-40NM/883
	5962-88670 **04 KX**	AT22V10-20FM/883
	5962-88670 **04 LX**	AT22V10-20GM/883
	5962-88670 **04 3X**	AT22V10-20NM/883

Case Outline	
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT22V10L OTP

Generic Number	Standard Military Drawing Number				Description	
C22V10L OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-89755	01	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-89755	02	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
	5962-89755	03	K, L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-89755 **01 KX**	AT22V10L-25FM/883
	5962-89755 **01 LX**	AT22V10L-25GM/883
	5962-89755 **01 3X**	AT22V10L-25NM/883
	5962-89755 **02 KX**	AT22V10L-30FM/883
	5962-89755 **02 LX**	AT22V10L-30GM/883
	5962-89755 **02 3X**	AT22V10L-30NM/883
	5962-89755 **03 KX**	AT22V10L-40FM/883
	5962-89755 **03 LX**	AT22V10L-40GM/883
	5962-89755 **03 3X**	AT22V10L-40NM/883

Case Outline	
K	24C, 24 Lead, Non-Windowed, Ceramic Flat Package (Cerpack)
L	24D3, 24 Lead 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

ATV750

Generic Number	Standard Military Drawing Number				Description	
V750	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88726	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	40
	5962-88726	02	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	35

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88726 **01 LX**	ATV750-40DM/883
	5962-88726 **01 3X**	ATV750-40LM/883
	5962-88726 **02 LX**	ATV750-35DM/883
	5962-88726 **02 3X**	ATV750-35LM/883

Case Outline	
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27C256R

Generic Number	Standard Military Drawing Number				Description	
27C256R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86063	01	X, Y, Z	X, A, C	32K x 8 EPROM	200
	5962-86063	02	X, Y, Z	X, A, C	32K x 8 EPROM	250
	5962-86063	03	X, Y, Z	X, A, C	32K x 8 EPROM	300
	5962-86063	04	X, Y, Z	X, A, C	32K x 8 EPROM	170
	5962-86063	05	X, Y, Z	X, A, C	32K x 8 EPROM	150

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86063 **01 XX**	AT27C256R-20DM/883
	5962-86063 **01 YX**	AT27C256R-20LM/883
	5962-86063 **01 ZX**	AT27C256R-20KM/883
	5962-86063 **02 XX**	AT27C256R-25DM/883
	5962-86063 **02 YX**	AT27C256R-25LM/883
	5962-86063 **02 ZX**	AT27C256R-25KM/883
	5962-86063 **03 XX**	AT27C256R-30DM/883
	5962-86063 **03 YX**	AT27C256R-30LM/883
	5962-86063 **03 ZX**	AT27C256R-30KM/883
	5962-86063 **04 XX**	AT27C256R-17DM/883
	5962-86063 **04 YX**	AT27C256R-17LM/883
	5962-86063 **04 ZX**	AT27C256R-17KM/883
	5962-86063 **05 XX**	AT27C256R-15DM/883
	5962-86063 **05 YX**	AT27C256R-15LM/883
	5962-86063 **05 ZX**	AT27C256R-15KM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27HC256R

Generic Number	Standard Military Drawing Number				Description	
27HC256R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86063	08	X, Y, Z	X, A, C	32K x 8 EPROM	70

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86063 **08 XX**	AT27HC256R-70DM/883
	5962-86063 **08 YX**	AT27HC256R-70LM/883
	5962-86063 **08 ZX**	AT27HC256R-70KM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

AT27HC256RL

Generic Number	Standard Military Drawing Number				Description	
27HC256RL	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86063	06	X, Y, Z	X, A, C	32K x 8 EPROM	120
	5962-86063	07	X, Y, Z	X, A, C	32K x 8 EPROM	90

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86063 **06 XX**	AT27HC256RL-12DM/883
	5962-86063 **06 YX**	AT27HC256RL-12LM/883
	5962-86063 **06 ZX**	AT27HC256RL-12KM/883
	5962-86063 **07 XX**	AT27HC256RL-90DM/883
	5962-86063 **07 YX**	AT27HC256RL-90LM/883
	5962-86063 **07 ZX**	AT27HC256RL-90KM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27C512R

Generic Number	Standard Military Drawing Number				Description	
27C512R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87648	01	X, Y, Z	X, A, C	64K x 8 EPROM	150
	5962-87648	02	X, Y, Z	X, A, C	64K x 8 EPROM	200
	5962-87648	03	X, Y, Z	X, A, C	64K x 8 EPROM	250
	5962-87648	04	X, Y, Z	X, A, C	64K x 8 EPROM	120

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87648 **01 XX**	AT27C512R-15DM/883
	5962-87648 **01 YX**	AT27C512R-15LM/883
	5962-87648 **01 ZX**	AT27C512R-15KM/883
	5962-87648 **02 XX**	AT27C512R-20DM/883
	5962-87648 **02 YX**	AT27C512R-20LM/883
	5962-87648 **02 ZX**	AT27C512R-20KM/883
	5962-87648 **03 XX**	AT27C512R-25DM/883
	5962-87648 **03 YX**	AT27C512R-25LM/883
	5962-87648 **03 ZX**	AT27C512R-25KM/883
	5962-87648 **04 XX**	AT27C512R-12DM/883
	5962-87648 **04 YX**	AT27C512R-12LM/883
	5962-87648 **04 ZX**	AT27C512R-12KM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27C010

Generic Number	Standard Military Drawing Number				Description	
27C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-89614	01	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	300
	5962-89614	02	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	250
	5962-89614	03	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	200
	5962-89614	04	X, Y	X, A, C	128K x 8, 1-Mbit EPROM	170

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-89614 **01M XX**	AT27C010-30DM/883
	5962-89614 **01M YX**	AT27C010-30LM/883
	5962-89614 **02M XX**	AT27C010-25DM/883
	5962-89614 **02M YX**	AT27C010-25LM/883
	5962-89614 **03M XX**	AT27C010-20DM/883
	5962-89614 **03M YX**	AT27C010-20LM/883
	5962-89614 **04M XX**	AT27C010-17DM/883
	5962-89614 **04M YX**	AT27C010-17LM/883

Case Outline	
X	28DW6, 28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32LW, 32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32KW, 32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27C1024

Generic Number	Standard Military Drawing Number				Description	
27C1024	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-86805	01	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	300
	5962-86805	02	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	250
	5962-86805	03	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	200
	5962-86805	04	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	170

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86805 **01 QX**	AT27C1024-30DM/883
	5962-86805 **01 XX**	AT27C1024-30LM/883
	5962-86805 **02 QX**	AT27C1024-25DM/883
	5962-86805 **02 XX**	AT27C1024-25LM/883
	5962-86805 **03 QX**	AT27C1024-20DM/883
	5962-86805 **03 XX**	AT27C1024-20LM/883
	5962-86805 **04 QX**	AT27C1024-17DM/883
	5962-86805 **04 XX**	AT27C1024-17LM/883

Case Outline	
Q	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
X	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27HC1024

Generic Number	Standard Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
27HC1024	5962-86805	07	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	90
	5962-86805	08	Q, X	X, A, C	64K x 16, 1-Mbit EPROM	70

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-86805 **07 QX**	AT27HC1024-90DM/883
	5962-86805 **07 XX**	AT27HC1024-90LM/883
	5962-86805 **08 QX**	AT27HC1024-70DM/883
	5962-86805 **08 XX**	AT27HC1024-70LM/883

Case Outline	
Q	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
X	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27HC641R

Generic Number	Standard Military Drawing Number				Description	
27HC641R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87515	01	J, K, 3	X, A, C	8K x 8 [UV] PROM	45
	5962-87515	02	J, K, 3	X, A, C	8K x 8 [UV] PROM	55
	5962-87515	03	J, K, 3	X, A, C	8K x 8 [UV] PROM	70
	5962-87515	04	J, K, 3	X, A, C	8K x 8 [UV] PROM	90

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87515 **01 JX**	AT27HC641R-45DM/883
	5962-87515 **01 KX**	AT27HC641R-45CM/883
	5962-87515 **01 3X**	AT27HC641R-45LM/883
	5962-87515 **02 JX**	AT27HC641R-55DM/883
	5962-87515 **02 KX**	AT27HC641R-55CM/883
	5962-87515 **02 3X**	AT27HC641R-55LM/883
	5962-87515 **03 JX**	AT27HC641R-70DM/883
	5962-87515 **03 KX**	AT27HC641R-70CM/883
	5962-87515 **03 3X**	AT27HC641R-70LM/883
	5962-87515 **04 JX**	AT27HC641R-90DM/883
	5962-87515 **04 KX**	AT27HC641R-90CM/883
	5962-87515 **04 3X**	AT27HC641R-90LM/883

Case Outline	
J	24DW6, 24 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
K	24CW, 24 Lead, Windowed, Ceramic Flat Package (Cerpack)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT27HC642R

Generic Number	Standard Military Drawing Number				Description	
27HC642R	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	Access Time (ns)
	5962-87515	01	L	X, A, C	8K x 8 [UV] PROM	45
	5962-87515	02	L	X, A, C	8K x 8 [UV] PROM	55
	5962-87515	03	L	X, A, C	8K x 8 [UV] PROM	70
	5962-87515	04	L	X, A, C	8K x 8 [UV] PROM	90

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87515 **01** **LX**	AT27HC642R-45DM/883
	5962-87515 **02** **LX**	AT27HC642R-55DM/883
	5962-87515 **03** **LX**	AT27HC642R-70DM/883
	5962-87515 **04** **LX**	AT27HC642R-90DM/883

Case Outline	
L	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64

Generic Number	Standard Military Drawing Number				Description				
28C64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	13	U, X, Y, Z	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	350	1	10K
	5962-87514	14	U, X, Y	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	300	1	10K
	5962-87514	15	U, X, Y, Z	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	250	1	10K
	5962-87514	16	U, X, Y	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
	5962-87514	17	U, X, Y	X, A, C	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **13 UX**	AT28C64-35KM/883
	5962-87514 **13 XX**	AT28C64-35DM/883
	5962-87514 **13 YX**	AT28C64-35LM/883
	5962-87514 **13 ZX**	AT28C64-35FM/883
	5962-87514 **14 UX**	AT28C64-30KM/883
	5962-87514 **14 XX**	AT28C64-30DM/883
	5962-87514 **14 YX**	AT28C64-30LM/883
	5962-87514 **15 UX**	AT28C64-25KM/883
	5962-87514 **15 XX**	AT28C64-25DM/883
	5962-87514 **15 YX**	AT28C64-25LM/883
	5962-87514 **15 ZX**	AT28C64-25FM/883
	5962-87514 **16 UX**	AT28C64-20KM/883
	5962-87514 **16 XX**	AT28C64-20DM/883
	5962-87514 **16 YX**	AT28C64-20LM/883
	5962-87514 **17 UX**	AT28C64-15KM/883
	5962-87514 **17 XX**	AT28C64-15DM/883
	5962-87514 **17 YX**	AT28C64-15LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28C64X

Generic Number	Standard Military Drawing Number				Description				
28C64X	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	18	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	350	1	10K
	5962-87514	19	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	300	1	10K
	5962-87514	20	U, X, Y, Z	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	250	1	10K
	5962-87514	21	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	200	1	10K
	5962-87514	22	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **18 UX**	AT28C64X-35KM/883
	5962-87514 **18 XX**	AT28C64X-35DM/883
	5962-87514 **18 YX**	AT28C64X-35LM/883
	5962-87514 **19 UX**	AT28C64X-30KM/883
	5962-87514 **19 XX**	AT28C64X-30DM/883
	5962-87514 **19 YX**	AT28C64X-30LM/883
	5962-87514 **20 UX**	AT28C64X-25KM/883
	5962-87514 **20 XX**	AT28C64X-25DM/883
	5962-87514 **20 YX**	AT28C64X-25LM/883
	5962-87514 **20 ZX**	AT28C64X-25FM/883
	5962-87514 **21 UX**	AT28C64X-20KM/883
	5962-87514 **21 XX**	AT28C64X-20DM/883
	5962-87514 **21 YX**	AT28C64X-20LM/883
	5962-87514 **22 UX**	AT28C64X-15KM/883
	5962-87514 **22 XX**	AT28C64X-15DM/883
	5962-87514 **22 YX**	AT28C64X-15LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28PC64

Generic Number	Standard Military Drawing Number				Description				
28PC64	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	06	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
	5962-87514	07	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
	5962-87514	08	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
	5962-87514	09	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **06 UX**	AT28PC64-35KM/883
	5962-87514 **06 XX**	AT28PC64-35DM/883
	5962-87514 **06 YX**	AT28PC64-35LM/883
	5962-87514 **07 UX**	AT28PC64-30KM/883
	5962-87514 **07 XX**	AT28PC64-30DM/883
	5962-87514 **07 YX**	AT28PC64-30LM/883
	5962-87514 **08 UX**	AT28PC64-25KM/883
	5962-87514 **08 XX**	AT28PC64-25DM/883
	5962-87514 **08 YX**	AT28PC64-25LM/883
	5962-87514 **09 UX**	AT28PC64-20KM/883
	5962-87514 **09 XX**	AT28PC64-20DM/883
	5962-87514 **09 YX**	AT28PC64-20LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC64L

Generic Number	Standard Military Drawing Number				Description				
28HC64L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-87514	10	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
	5962-87514	11	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
	5962-87514	12	U, X, Y	X, A, C	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87514 **10 UX**	AT28HC64L-12KM/883
	5962-87514 **10 XX**	AT28HC64L-12DM/883
	5962-87514 **10 YX**	AT28HC64L-12LM/883
	5962-87514 **11 UX**	AT28HC64L-90KM/883
	5962-87514 **11 XX**	AT28HC64L-90DM/883
	5962-87514 **11 YX**	AT28HC64L-90LM/883
	5962-87514 **12 UX**	AT28HC64L-70KM/883
	5962-87514 **12 XX**	AT28HC64L-70DM/883
	5962-87514 **12 YX**	AT28HC64L-70LM/883

Case Outline	
U	32K, 32 Lead, Non-Windowed, Ceramic J-Leaded Quad Flat Package (Cerquad)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256

Generic Number	Standard Military Drawing Number				Description				
28C256	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88525	01	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
	5962-88525	02	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
	5962-88525	03	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
	5962-88525	04	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
	5962-88525	06	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **01 UX**	AT28C256-35UM/883
	5962-88525 **01 XX**	AT28C256-35DM/883
	5962-88525 **01 YX**	AT28C256-35LM/883
	5962-88525 **01 ZX**	AT28C256-35FM/883
	5962-88525 **02 UX**	AT28C256-30UM/883
	5962-88525 **02 XX**	AT28C256-30DM/883
	5962-88525 **02 YX**	AT28C256-30LM/883
	5962-88525 **02 ZX**	AT28C256-30FM/883
	5962-88525 **03 UX**	AT28C256-25UM/883
	5962-88525 **03 XX**	AT28C256-25DM/883
	5962-88525 **03 YX**	AT28C256-25LM/883
	5962-88525 **03 ZX**	AT28C256-25FM/883
	5962-88525 **04 UX**	AT28C256-20UM/883
	5962-88525 **04 XX**	AT28C256-20DM/883
	5962-88525 **04 YX**	AT28C256-20LM/883
	5962-88525 **04 ZX**	AT28C256-20FM/883
	5962-88525 **06 UX**	AT28C256-15UM/883
	5962-88525 **06 XX**	AT28C256-15DM/883
	5962-88525 **06 YX**	AT28C256-15LM/883
	5962-88525 **06 ZX**	AT28C256-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256E

Generic Number	Standard Military Drawing Number				Description				
28C256E	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88525	05	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **05 UX**	AT28C256E-25UM/883
	5962-88525 **05 XX**	AT28C256E-25DM/883
	5962-88525 **05 YX**	AT28C256E-25LM/883
	5962-88525 **05 ZX**	AT28C256E-25FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28C256F

Generic Number	Standard Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
28C256F	5962-88525	07	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	150	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88525 **07 UX**	AT28C256F-15UM/883
	5962-88525 **07 XX**	AT28C256F-15DM/883
	5962-88525 **07 YX**	AT28C256F-15LM/883
	5962-88525 **07 ZX**	AT28C256F-15FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

AT28HC256

Generic Number	Standard Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
28HC256	5962-88634	03	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	90	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **03 UX**	AT28HC256-90UM/883
	5962-88634 **03 XX**	AT28HC256-90DM/883
	5962-88634 **03 YX**	AT28HC256-90LM/883
	5962-88634 **03 ZX**	AT28HC256-90FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256F

Generic Number	Standard Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
28HC256F	5962-88634	04	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **04 UX**	AT28HC256F-90UM/883
	5962-88634 **04 XX**	AT28HC256F-90DM/883
	5962-88634 **04 YX**	AT28HC256F-90LM/883
	5962-88634 **04 ZX**	AT28HC256F-90FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256L

Generic Number	Standard Military Drawing Number				Description				
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
28HC256L	5962-88634	01	U, X, Y, Z	X, A, C	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **01 UX**	AT28HC256L-12UM/883
	5962-88634 **01 XX**	AT28HC256L-12DM/883
	5962-88634 **01 YX**	AT28HC256L-12LM/883
	5962-88634 **01 ZX**	AT28HC256L-12FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28HC256LF

Generic Number	Standard Military Drawing Number				Description				
28HC256LF	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Speed(ms)	Endurance (Cycles)
	5962-88634	02	U, X, Y, Z	X, A, C	32K x 8 E^2PROM Data Polling	Byte/Page	120	3	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88634 **02 UX**	AT28HC256LF-12UM/883
	5962-88634 **02 XX**	AT28HC256LF-12DM/883
	5962-88634 **02 YX**	AT28HC256LF-12LM/883
	5962-88634 **02 ZX**	AT28HC256LF-12FM/883

Case Outline	
U	28U, 28 Pin, Ceramic Pin Grid Array (PGA)
X	28D6, 28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
Y	32L, 32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	28F, 28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.2 - Atmel SMD Part Types, Listed by Atmel Part Number

AT28C010

Generic Number	Standard Military Drawing Number				Description				
28C010	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd(ms)	Endurance (Cycles)
	5962-38267	01	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^2PROM Data Polling	Byte/ Page	250	10	10K
	5962-38267	03	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
	5962-38267	05	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
	5962-38267	07	X, Y, Z	X, A, C	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-38267 **01M XX**	AT28C010-25BM/883
	5962-38267 **01M YX**	AT28C010-25LM/883
	5962-38267 **01M ZX**	AT28C010-25FM/883
	5962-38267 **03M XX**	AT28C010-20BM/883
	5962-38267 **03M YX**	AT28C010-20LM/883
	5962-38267 **03M ZX**	AT28C010-20FM/883
	5962-38267 **05M XX**	AT28C010-15BM/883
	5962-38267 **05M YX**	AT28C010-15LM/883
	5962-38267 **05M ZX**	AT28C010-15FM/883
	5962-38267 **07M XX**	AT28C010-12BM/883
	5962-38267 **07M YX**	AT28C010-12LM/883
	5962-38267 **07M ZX**	AT28C010-12FM/883

Case Outline	
X	32B, 32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
Y	44L, 44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Z	32F, 32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)

Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-38267						
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description End Write Indicator**	**Write Mode**	**Access Time(ns)**	**Write Spd. (ms)**	**Endur. (Cycles)**
5962-38267 01M XX	AT28C010-25BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M YX	AT28C010-25LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 01M ZX	AT28C010-25FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	250	10	10K
5962-38267 03M XX	AT28C010-20BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M YX	AT28C010-20LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 03M ZX	AT28C010-20FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	200	10	10K
5962-38267 05M XX	AT28C010-15BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M YX	AT28C010-15LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 05M ZX	AT28C010-15FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	150	10	10K
5962-38267 07M XX	AT28C010-12BM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M YX	AT28C010-12LM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K
5962-38267 07M ZX	AT28C010-12FM/883	128K x 8, 1-Mbit E^2PROM $\overline{\text{Data}}$ Polling	Byte/ Page	120	10	10K

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-86063			
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**Access Time (ns)**
5962-86063 01 XX	AT27C256R-20DM/883	32K x 8 EPROM	200
5962-86063 01 YX	AT27C256R-20LM/883	32K x 8 EPROM	200
5962-86063 01 ZX	AT27C256R-20KM/883	32K x 8 EPROM	200
5962-86063 02 XX	AT27C256R-25DM/883	32K x 8 EPROM	250
5962-86063 02 YX	AT27C256R-25LM/883	32K x 8 EPROM	250
5962-86063 02 ZX	AT27C256R-25KM/883	32K x 8 EPROM	250
5962-86063 03 XX	AT27C256R-30DM/883	32K x 8 EPROM	300
5962-86063 03 YX	AT27C256R-30LM/883	32K x 8 EPROM	300
5962-86063 03 ZX	AT27C256R-30KM/883	32K x 8 EPROM	300
5962-86063 04 XX	AT27C256R-17DM/883	32K x 8 EPROM	170
5962-86063 04 YX	AT27C256R-17LM/883	32K x 8 EPROM	170
5962-86063 04 ZX	AT27C256R-17KM/883	32K x 8 EPROM	170
5962-86063 05 XX	AT27C256R-15DM/883	32K x 8 EPROM	150
5962-86063 05 YX	AT27C256R-15LM/883	32K x 8 EPROM	150
5962-86063 05 ZX	AT27C256R-15KM/883	32K x 8 EPROM	150
5962-86063 06 XX	AT27HC256RL-12DM/883	32K x 8 EPROM	120
5962-86063 06 YX	AT27HC256RL-12LM/883	32K x 8 EPROM	120
5962-86063 06 ZX	AT27HC256RL-20LM/883	32K x 8 EPROM	120
5962-86063 07 XX	AT27HC256RL-90DM/883	32K x 8 EPROM	90
5962-86063 07 YX	AT27HC256RL-90LM/883	32K x 8 EPROM	90
5962-86063 07 ZX	AT27HC256RL-90KM/883	32K x 8 EPROM	90
5962-86063 08 XX	AT27HC256R-70DM/883	32K x 8 EPROM	70
5962-86063 08 YX	AT27HC256R-70LM/883	32K x 8 EPROM	70
5962-86063 08 ZX	AT27HC256R-70KM/883	32K x 8 EPROM	70

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-86805

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-86805 01 QX	AT27C1024-30DM/883	64K x 16, 1-Mbit EPROM	300
5962-86805 01 XX	AT27C1024-30LM/883	64K x 16, 1-Mbit EPROM	300
5962-86805 02 QX	AT27C1024-25DM/883	64K x 16, 1-Mbit EPROM	250
5962-86805 02 XX	AT27C1024-25DM/883	64K x 16, 1-Mbit EPROM	250
5962-86805 03 QX	AT27C1024-20DM/883	64K x 16, 1-Mbit EPROM	200
5962-86805 03 XX	AT27C1024-20DM/883	64K x 16, 1-Mbit EPROM	200
5962-86805 04 QX	AT27C1024-17DM/883	64K x 16, 1-Mbit EPROM	170
5962-86805 04 XX	AT27C1024-17LM/883	64K x 16, 1-Mbit EPROM	170
5962-86805 07 QX	AT27HC1024-90DM/883	64K x 16, 1-Mbit EPROM	90
5962-86805 07 XX	AT27HC1024-90LM/883	64K x 16, 1-Mbit EPROM	90
5962-86805 08 QX	AT27HC1024-70DM/883	64K x 16, 1-Mbit EPROM	70
5962-86805 08 XX	AT27HC1024-70LM/883	64K x 16, 1-Mbit EPROM	70

5962-87514

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 06 UX	AT28PC64-35KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 06 XX	AT28PC64-35DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 06 YX	AT28PC64-35LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	2	10K
5962-87514 07 UX	AT28PC64-30KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 07 XX	AT28PC64-30DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 07 YX	AT28PC64-30LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	2	10K
5962-87514 08 UX	AT28PC64-25KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 08 XX	AT28PC64-25DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 08 YX	AT28PC64-25LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	2	10K
5962-87514 09 UX	AT28PC64-20KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K
5962-87514 09 XX	AT28PC64-20DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-87514 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 09 YX	AT28PC64-20LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	2	10K
5962-87514 10 UX	AT28HC64L-12KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 10 XX	AT28HC64L-12DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 10 YX	AT28HC64L-12LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	120	2	10K
5962-87514 11 UX	AT28HC64L-90KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 11 XX	AT28HC64L-90DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 11 YX	AT28HC64L-90LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	90	2	10K
5962-87514 12 UX	AT28HC64L-70KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 12 XX	AT28HC64L-70DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 12 YX	AT28HC64L-70LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	70	2	10K
5962-87514 13 UX	AT28C64-35KM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 XX	AT28C64-35DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 YX	AT28C64-35LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 13 ZX	AT28C64-35FM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	350	1	10K
5962-87514 14 UX	AT28C64-30KM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 14 XX	AT28C64-30DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 14 YX	AT28C64-30LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	300	1	10K
5962-87514 15 UX	AT28C64-25KM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 XX	AT28C64-25DM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 YX	AT28C64-25LM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K
5962-87514 15 ZX	AT28C64-25FM/883	8K x 8 E^2PROM Rdy/$\overline{\text{Busy}}$	Byte	250	1	10K

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-87514 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 16 UX	AT28C64-20KM/883	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
5962-87514 16 XX	AT28C64-20DM/883	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
5962-87514 16 YX	AT28C64-20LM/883	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	200	1	10K
5962-87514 17 UX	AT28C64-15KM/883	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K
5962-87514 17 XX	AT28C64-15DM/883	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K
5962-87514 17 YX	AT28C64-15LM/883	8K x 8 E^2PROM Rdy/$\overline{Busy}$	Byte	150	1	10K
5962-87514 18 UX	AT28C64X-35KM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	350	1	10K
5962-87514 18 XX	AT28C64X-35DM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	350	1	10K
5962-87514 18 YX	AT28C64X-35LM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	350	1	10K
5962-87514 19 UX	AT28C64X-30KM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	300	1	10K
5962-87514 19 XX	AT28C64X-30DM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	300	1	10K
5962-87514 19 YX	AT28C64X-30LM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	300	1	10K
5962-87514 20 UX	AT28C64X-25KM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	250	1	10K
5962-87514 20 XX	AT28C64X-25DM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	250	1	10K
5962-87514 20 YX	AT28C64X-25LM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	250	1	10K
5962-87514 20 ZX	AT28C64X-25FM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	250	1	10K
5962-87514 21 UX	AT28C64X-20KM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	200	1	10K
5962-87514 21 XX	AT28C64X-20DM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	200	1	10K
5962-87514 21 YX	AT28C64X-20LM/883	8K x 8 E^2PROM $\overline{Data}$ Polling	Byte	200	1	10K

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-87514 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-87514 22 UX	AT28C64X-15KM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 XX	AT28C64X-15DM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K
5962-87514 22 YX	AT28C64X-15LM/883	8K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte	150	1	10K

5962-87515

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87515 01 JX	AT27HC641R-45DM/883	8K x 8 [UV] PROM	45
5962-87515 01 KX	AT27HC641R-45CM/883	8K x 8 [UV] PROM	45
5962-87515 01 LX	AT27HC642R-45DM/883	8K x 8 [UV] PROM	45
5962-87515 01 3X	AT27HC641R-45LM/883	8K x 8 [UV] PROM	45
5962-87515 02 JX	AT27HC641R-55DM/883	8K x 8 [UV] PROM	55
5962-87515 02 KX	AT27HC641R-55CM/883	8K x 8 [UV] PROM	55
5962-87515 02 LX	AT27HC642R-55DM/883	8K x 8 [UV] PROM	55
5962-87515 02 3X	AT27HC641R-55LM/883	8K x 8 [UV] PROM	55
5962-87515 03 JX	AT27HC641R-70DM/883	8K x 8 [UV] PROM	70
5962-87515 03 KX	AT27HC641R-70CM/883	8K x 8 [UV] PROM	70
5962-87515 03 LX	AT27HC642R-70DM/883	8K x 8 [UV] PROM	70
5962-87515 03 3X	AT27HC641R-70LM/883	8K x 8 [UV] PROM	70
5962-87515 04 JX	AT27HC641R-90DM/883	8K x 8 [UV] PROM	90
5962-87515 04 KX	AT27HC641R-90CM/883	8K x 8 [UV] PROM	90
5962-87515 04 LX	AT27HC642R-90DM/883	8K x 8 [UV] PROM	90
5962-87515 04 3X	AT27HC641R-90LM/883	8K x 8 [UV] PROM	90

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-87539

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87539 01 KX	AT22V10-25YM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 LX	AT22V10-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 3X	AT22V10-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 02 KX	AT22V10-30YM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 02 LX	AT22V10-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 02 3X	AT22V10-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-87539 03 KX	AT22V10-40YM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 03 LX	AT22V10-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 03 3X	AT22V10-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-87539 04 KX	AT22V10-20YM/883	22-Input, 10-Output and-or-Logic Array	20
5962-87539 04 LX	AT22V10-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-87539 04 3X	AT22V10-20LM/883	22-Input, 10-Output and-or-Logic Array	20

5962-87648

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-87648 01 XX	AT27C512R-15DM/883	64K x 8 EPROM	150
5962-87648 01 YX	AT27C512R-15LM/883	64K x 8 EPROM	150
5962-87648 01 ZX	AT27C512R-15KM/883	64K x 8 EPROM	150
5962-87648 02 XX	AT27C512R-20DM/883	64K x 8 EPROM	200
5962-87648 02 YX	AT27C512R-20LM/883	64K x 8 EPROM	200
5962-87648 02 ZX	AT27C512R-20KM/883	64K x 8 EPROM	200
5962-87648 03 XX	AT27C512R-25DM/883	64K x 8 EPROM	250
5962-87648 03 YX	AT27C512R-25LM/883	64K x 8 EPROM	250
5962-87648 03 ZX	AT27C512R-25KM/883	64K x 8 EPROM	250
5962-87648 04 XX	AT27C512R-12DM/883	64K x 8 EPROM	120
5962-87648 04 YX	AT27C512R-12LM/883	64K x 8 EPROM	120
5962-87648 04 ZX	AT27C512R-12KM/883	64K x 8 EPROM	120

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-88525

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 01 UX	AT28C256-35UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 XX	AT28C256-35DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 01 YX	AT28C256-35LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte Page	350	10	10K
5962-88525 01 ZX	AT28C256-35FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	350	10	10K
5962-88525 02 UX	AT28C256-30UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 XX	AT28C256-30DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 YX	AT28C256-30LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 02 ZX	AT28C256-30FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	300	10	10K
5962-88525 03 UX	AT28C256-25UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 XX	AT28C256-25DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 YX	AT28C256-25LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 03 ZX	AT28C256-25FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	10K
5962-88525 04 UX	AT28C256-20UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 XX	AT28C256-20DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 YX	AT28C256-20LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 04 ZX	AT28C256-20FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	200	10	10K
5962-88525 05 UX	AT28C256E-25UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 XX	AT28C256E-25DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 YX	AT28C256E-25LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 05 ZX	AT28C256E-25FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	250	10	100K
5962-88525 06 UX	AT28C256-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-88525 (continued)

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88525 06 XX	AT28C256-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 YX	AT28C256-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 06 ZX	AT28C256-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	10	10K
5962-88525 07 UX	AT28C256F-15UM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 XX	AT28C256F-15DM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 YX	AT28C256F-15LM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K
5962-88525 07 ZX	AT28C256F-15FM/883	32K x 8 E^2PROM $\overline{\text{Data}}$ Polling	Byte/Page	150	3	10K

5962-88634

Atmel Order Number	Atmel Similar Part Number	Circuit Description End Write Indicator	Write Mode	Access Time(ns)	Write Spd. (ms)	Endur. (Cycles)
5962-88634 01 UX	AT28HC256L-12UM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 01 XX	AT28HC256L-12DM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 01 YX	AT28HC256L-12LM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 01 ZX	AT28HC256L-12FM/883	32K x 8 E^2PROM	Byte/Page	120	10	10K
5962-88634 02 UX	AT28HC256LF-12UM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 02 XX	AT28HC256LF-12DM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 02 YX	AT28HC256LF-12LM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 02 ZX	AT28HC256LF-12FM/883	32K x 8 E^2PROM	Byte/Page	120	3	10K
5962-88634 03 UX	AT28HC256-90UM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 03 XX	AT28HC256-90DM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 03 YX	AT28HC256-90LM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 03 ZX	AT28HC256-90FM/883	32K x 8 E^2PROM	Byte/Page	90	10	10K
5962-88634 04 UX	AT28HC256F-90UM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K
5962-88634 04 XX	AT28HC256F-90DM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K
5962-88634 04 YX	AT28HC256F-90LM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K
5962-88634 04 ZX	AT28HC256F-90FM/883	32K x 8 E^2PROM	Byte/Page	90	3	10K

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-88670

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88670 01 KX	AT22V10-25FM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 LX	AT22V10-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 3X	AT22V10-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 02 KX	AT22V10-30FM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 02 LX	AT22V10-30GM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 02 3X	AT22V10-30NM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88670 03 KX	AT22V10-40FM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 03 LX	AT22V10-40GM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 03 3X	AT22V10-40NM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88670 04 KX	AT22V10-20FM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 04 LX	AT22V10-20GM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88670 04 3X	AT22V10-20NM/883	22-Input, 10-Output and-or-Logic Array	20

5962-88724

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88724 01 KX	AT22V10L-25YM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 LX	AT22V10L-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 3X	AT22V10L-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 02 KX	AT22V10L-30YM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 02 LX	AT22V10L-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 02 3X	AT22V10L-30LM/883	22-Input, 10-Output and-or-Logic Array	30
5962-88724 03 KX	AT22V10L-40YM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 03 LX	AT22V10L-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 03 3X	AT22V10L-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88724 04 KX	AT22V10L-20YM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 LX	AT22V10L-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 3X	AT22V10L-20LM/883	22-Input, 10-Output and-or-Logic Array	20

Table 14.3 - Atmel SMD Part Types, Listed by SMD Number

5962-88726

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-88726 01 LX	ATV750-40DM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88726 01 3X	ATV750-40LM/883	22-Input, 10-Output and-or-Logic Array	40
5962-88726 02 LX	ATV750-35DM/883	22-Input, 10-Output and-or-Logic Array	35
5962-88726 02 3X	ATV750-35LM/883	22-Input, 10-Output and-or-Logic Array	35

5962-89614

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-89614 01M XX	AT27C010-30DM/883	128K x 8, 1-Mbit EPROM	300
5962-89614 01M YX	AT27C010-30LM/883	128K x 8, 1-Mbit EPROM	300
5962-89614 02M XX	AT27C010-25DM/883	128K x 8, 1-Mbit EPROM	250
5962-89614 02M YX	AT27C010-25LM/883	128K x 8, 1-Mbit EPROM	250
5962-89614 03M XX	AT27C010-20DM/883	128K x 8, 1-Mbit EPROM	200
5962-89614 03M YX	AT27C010-20LM/883	128K x 8, 1-Mbit EPROM	200
5962-89614 04M XX	AT27C010-17DM/883	128K x 8, 1-Mbit EPROM	170
5962-89614 04M YX	AT27C010-17LM/883	128K x 8, 1-Mbit EPROM	170

5962-89755

Atmel Order Number	Atmel Similar Part Number	Circuit Description	Access Time (ns)
5962-89755 01 KX	AT22V10L-25FM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 LX	AT22V10L-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 3X	AT22V10L-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 02 KX	AT22V10L-30FM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 02 LX	AT22V10L-30GM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 02 3X	AT22V10L-30NM/883	22-Input, 10-Output and-or-Logic Array	30
5962-89755 03 KX	AT22V10L-40FM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 03 LX	AT22V10L-40GM/883	22-Input, 10-Output and-or-Logic Array	40
5962-89755 03 3X	AT22V10L-40NM/883	22-Input, 10-Output and-or-Logic Array	40

Atmel Modified Class S Integrated Circuit Test Flow

Introduction

Atmel has expanded upon and modified standard "Class S" testing procedures to accommodate up-to-date small-geometry integrated circuit processing methods which are not covered in the standard Class S Flow. This document describes Atmel's current Modified Class S Flow.

Modified Class S Flow

Screen Requirements	Atmel Procedure Number	MIL-STD-883C (as applicable)
Wafer Lot Acceptance		MIL-STD-883C, M5007[4]
Assembly		
Wafer Mount	1980-004, 900-055	
Wafer Saw	1980-003, 900-059	
Wafer Clean	1980-005, 900-100	
Die Sort, Manual	1980-029, 900-024	
2nd Optical, Military		Method 2010, Cond A, Class S Criteria
Package Clean	1980-037, 900-004	
Die Attach	Package Related	Mark Wafer No. on Pkg
Shear Test	1980-038, 900-046	Method 2019
Inspect [1]	1980-050, 900-102	Method 2010, Cond A [5]
Wire Bond	1980-013, 900-118, 900-031	
Wire Bond Pull Test	1980-039, 900-032	Method 2011, Cond D
Non Dest. Bond Pull	1980-039, 900-032	Method 2023
3rd Optical, Military	1980-050, 900-021	Method 2010 Cond A, Class S Criteria
QA Internal Visual	240-037	Method 2010, Cond A
Preseal Clean	900-008	Nitrogen Blow Off
Preseal Bake, Vacuum	900-009	
Seal	Package Related	
Mark	1980-032, 900-042	
Production Screens		
Temperature Cycling	100%	Method 1010 Cond C
Constant Acceleration	100%	Method 2001 Cond E
Visual Inspect [6]		
Pind [1]	100%	Method 2020 Cond A
Serialization	100%	
Pre-burn-in	100%	
Test @ 25°C		

Continued on Next Page

Modified Class S Flow, *Continued*

Screen Requirements	Atmel Procedure Number	MIL-STD-883C (as applicable)
Burn-in [3]	100%	Method 1015, 240 hours
Interim Elect. @ 25°C [7]	100%	
HRTB Burn-in (Option) [7]		M1015, Cond A or C, 72 hours
Post burn-in Elect 25°C	100%	Read and Record Subgroup 1
Percent Defective 3%, 5%	100%	Method 5004 p 3.5.1
Final Electrical Test	100%	Method 5004 p 3.5.2
Fine, Gross Seal [1]	100%[9]	Method 1014
Radiographic [1]	100%	Method 2012
Quality Conformance Inspection Sample Selection	Sample	Method 5005 p 3.5

Quality Conformance Inspections, Group A Electrical Tests

Perform for Every Lot

Inspection		-883 Method	100% Test	Sample/ Accept
Subgroup 1	Static Tests @ 25°C	5005	yes	116/0
Subgroup 2	Static Tests @ 125°C	5005	yes	116/0
Subgroup 3	Static Tests @ -55°C	5005	yes	116/0
Subgroup 4	Dynamic @ 25°C	5005	yes	116/0
Subgroup 5	Dynamic @ 125°C	5005	yes	116/0
Subgroup 6	Dynamic @ -55°C	5005	yes	116/0
Subgroup 7	Functional @ 25°C	5005	yes	116/0
Subgroup 8a	+125°C Functional Tests	5005	yes	116/0
Subgroup 8b	-55°C Functional Tests	5005	yes	116/0
Subgroup 9	Switching @ 25°C	5005	yes	116/0

Notes:

1. This screening procedure shall be performed within the sequence options allowed by MIL-STD-883, Method 5004, but not necessarily in the sequence shown.
2. Parametric Read and Record requirements shall exist for this procedure only when delta parametric limits are required in the PDA procedure determination by customer specification.
3. Condition F of MIL-STD-883 Method 1015 shall not apply. Paragraph 3.4.2 of MIL-STD-883 Method 5004 shall not apply.
4. Products made by Atmel do not comply to several requirements of MIL-STD-883 Method 5007. These include wafer, metal and glassivation thickness, where thickness limits are different by design, and SEM inspection where lot and sample size requirements of method 5007 are not compatible with modern equipment capacity. An alternative Atmel Wafer Lot Acceptance method exists and shall be used in place of method 5007. It is available upon request (when non-disclosure agreements exist).
5. Atmel shall take limited exception to compliance with MIL-STD-883 method 2010 for all contracts and all product. Atmel will physically perform the inspection to the best of its ability but will not guarantee absence of die visual defects in total or to any specified LTPD limit. The extreme complexity and small feature size of Atmel integrated circuit die make it physically impossible to inspect 100% of die features for the defect excluded by Method 2010.
6. This procedure will be performed at the option of Atmel. No lot acceptance criteria shall be imposed for this procedure.
7. Interim electrical screen and HTRB burn-in shall be performed only when required by customer specification. When they are performed, Read and Record requirements shall exist only when delta parametric limits are required as part of PDA determination by customer specification.
8. PIND shall be waived for non-JAN and non-883 compliant product unless specifically required by customer specification.
9. Shall be performed after all lead forming, clipping or straightening operations and only in sequence allowed by MIL-STD-883, Method 5004.
10. Shall be performed in sequence allowed by MIL-STD-883 method 5004. If any lead forming, clipping, or straightening operations occur after this procedure, a sample seal test shall be performed on the lot (Fine and Gross with LTPD = 2, C = 0).

Quality Conformance Inspections, Group B Tests

S = Sample Size / Accept Number

MIL-STD-883	883 Method	5005 Class S
Subgroup 1		
a. Physical Dimensions (1)	2016	yes, S = 2(0)
b. Internal Water Vapor Content	1018	yes (1,4,7), S = 3(0) or 5(1)
Subgroup 2 6		
a. Resistance to Solvents, S = 4(0)	2015	yes
b. Internal Vis and Mech, S = 2(0)	2013 and 2014	yes
c. Bond Strength, LTPD = 10 (2)	2011	yes
d. Die Shear Test	2019	yes
Subgroup 3		
a. Solderability (3,6), LTPD = 10	2003	yes
Subgroup 4 S = 2(0)		
a. Lead Integrity, S = 2(0)	2004 or 2028	yes
b. Seal Test Fine and Gross	1014	yes
c. Lid Torque, S = 2(0)	2024	yes (4)
Subgroup 5		
a. Steady State Life	1005	yes
b. Electrical Parameters	*	yes (8)
Subgroup 6		
a. Temp Cycle, 100 cycles	1010, Cond C	yes
b. Constant Acceleration	2001, Cond E	yes
c. Seal Test Fine and Gross	1014	yes
d. Electrical Parameters		yes (8), R and R
e. Die Shear Strength	2019	
Subgroup 7		
a. ESD	3015	yes (5), S = 3(0) / 15(0)
b. Electrical Parameters	group A, sub 1	yes (5)

*Per Device Spec.

Notes:
1. Not required for Method 5005 devices if Group D testing is performed.
2. LTPD = Number of bond pulls selected from a minimum of four devices.
3. Required number of leads must be contained in a minimum of three devices. Must be post Burn-In devices.
4. Applies only to packages with a glass-frit seal.
5. Unless otherwise specified test shall be performed for initial Qualification and product redesign as a minimum.
6. Electrical rejects may be used.
7. Required only when package contains a dessicant.
8. End point electricals as specified in applicable detail drawing.

Quality Conformance Inspections, Group D Tests

Perform Every Six Months for Method 5004, 5005 Devices

MIL-STD-883 Inspection	883 Method	5005 Class S
Subgroup 1 (1)		
a. Physical Dim, LTPD = 15	2016	yes
Subgroup 2		
a. Lead Integrity	2004 or 2028	yes
b. Seal Test Fine and Gross	1014	yes
Subgroup 3		LTPD = 15
a. Thermal Shock	1011	yes
b. Temperature Cycle	1010	yes
c. Moisture Rest.	1004	yes
d. Seal Test Fine and Gross	1014	yes
e. Visual Examination	1004, 1010	yes
f. Electrical Parameters	*	yes (2)
Subgroup 4		LTPD = 15
a. Mechanical Shock	2002	yes
b. Vibration Var. Frequency	2007	yes
c. Constant Acceleration	2001	yes
d. Seal Test Fine and Gross	1014	yes
e. Visual Examination	1010, 1011	yes
f. Electrical Parameters	*	yes (2)
Subgroup 5 (1)		S = 15(0)
a. Salt Atmosphere	1009	yes
b. Seal Test Fine and Gross (4)	1014	yes
c. Visual Examination	1009	yes
Subgroup 6 (1)		S = 3(0) or 5(1)
Internal Water Vapor Content	1018	yes
Subgroup 7 (1)		S = 15(0)
Adhesion of Lead Finish	2025	yes
Subgroup 8 (3)		S = 5(0)
Lid Torque	2024	yes

*Per Device Spec.

Notes:
1. Electrical rejects may be used.
2. Per applicable detail drawing.
3. Applies to package with glass frit-seal only.
4. Only for packages with leads exiting through a glass seal.

Quality Conformance Inspections, Group E Tests

Group E testing will be performed per device / customer specification.

Contents

15

E^2PROM Die Products

Features

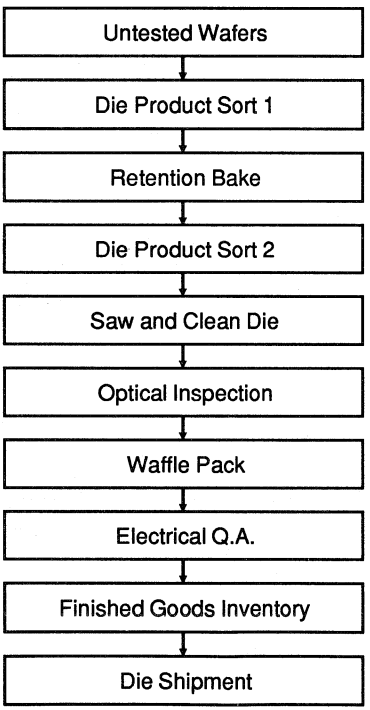
- High Performance CMOS Technology
- Low Power Dissipation - Active and Standby
- Hardware Data Protection Features
- DATA Polling for End of Write Detection
- High Reliability
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5V ± 10% Supply
- CMOS Compatible Inputs and Outputs
- 0°C to +70°C Operating Range
- Typical Die Thickness of 22 Mils

Description

To facilitate custom packaging, some Atmel E^2PROMS are available in die form. All Atmel E^2PROM die products are 100% electrically tested in wafer form and visually inspected after saw and clean. Atmel's E^2PROM die products are processed with an advanced CMOS floating gate technology. As with all Atmel products, they are designed and tested to ensure high quality and manufacturability. The devices may include such features as internal error correction for extended endurance and improved data retention characteristics.

Test Flow

Atmel's die product sort testing incorporates comprehensive functional and parametric tests into wafer level tests. The typical Atmel E^2PROM die test flow is outlined below.



Testing

Die product sort test 1 includes checks for basic D.C. parameters such as I_{CC} and input leakage as well as for A.C. switching parameters. Data pattern testing is included to guarantee the functionality of each bit and to guard against pattern sensitivity. Several oxide stress tests are included to reduce the likelihood of infant mortality failures.

The Data retention bake is included to ensure the integrity of the core cell oxides. A pattern is written to each die at the end of die sort test 1. The wafers are then subjected to a high temperature bake. After the bake, the pattern written in die sort test 1 is verified by die sort test 2.

A final quality assurance test is performed on each assembly lot. A sample of the dice ready to ship is selected and electrically examined.

Die Product Offering

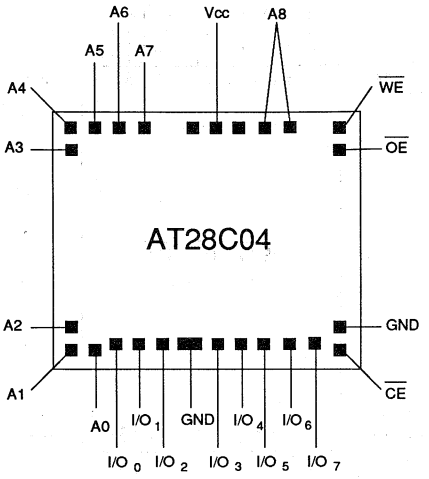
Die products are guaranteed across the commercial temperature operating range. The following E^2PROM die products are currently available from Atmel:

AT28C04	AT28HC64L
AT28C16	AT28HC256L
AT28C17	AT28HC291L
AT28C64	AT28C010
AT28PC64	AT28C1024
AT28C256	

Handling and Die Information

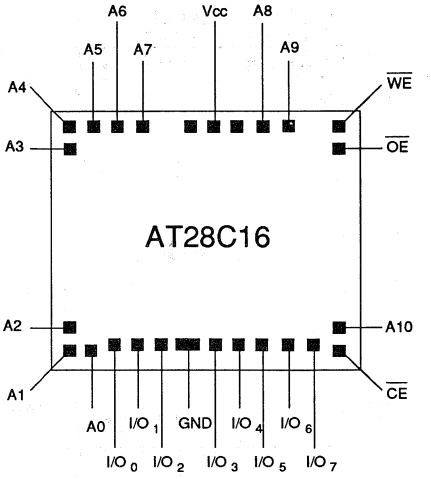
Handling instructions for E^2PROM die and other information needed for using E^2PROM die are available from Atmel.

AT28C04 DIE PINOUT



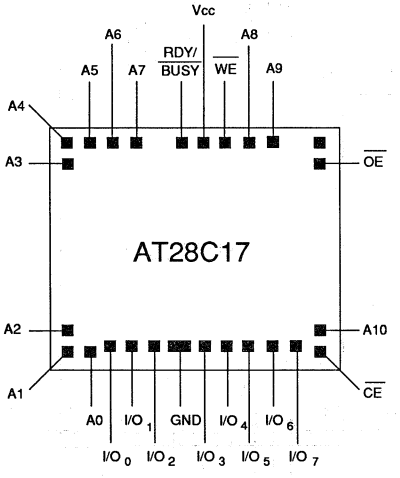
DIE SIZE: 137 X 117 mils
CONNECT SUBSTRATE TO GROUND

AT28C16 DIE PINOUT



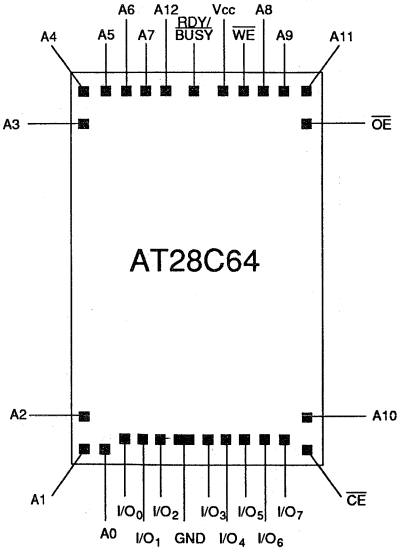
DIE SIZE: 137 X 117 mils
CONNECT SUBSTRATE TO GROUND

AT28C17 DIE PINOUT



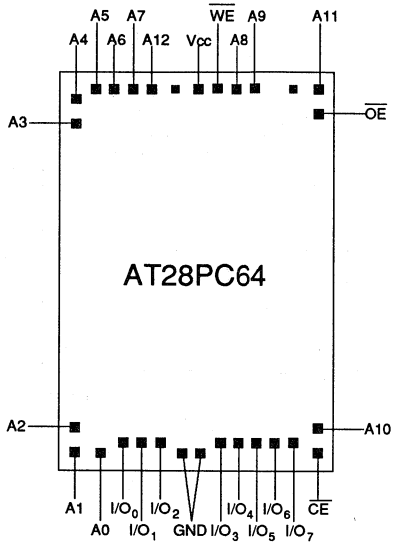
DIE SIZE: 137 X 117 mils
CONNECT SUBSTRATE TO GROUND

AT28C64 DIE PINOUT



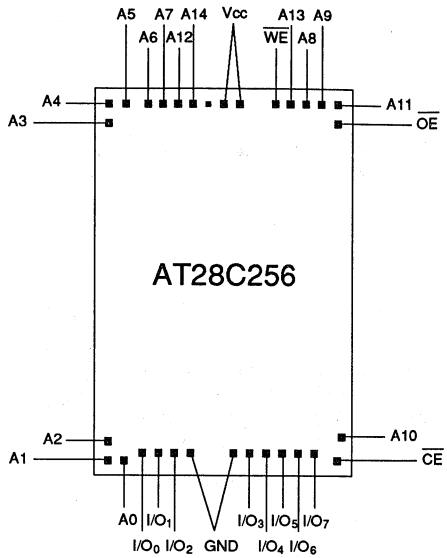
DIE SIZE: 133 X 207 mils
CONNECT SUBSTRATE TO GROUND

AT28PC64 DIE PINOUT



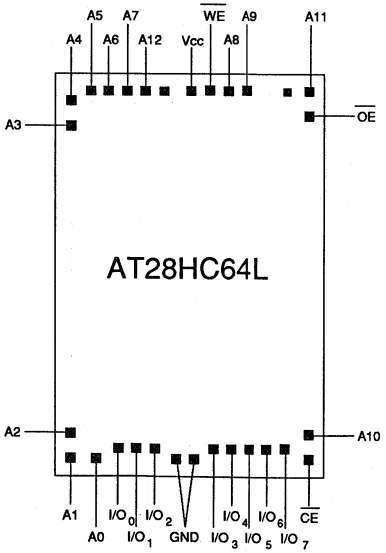
DIE SIZE: 146 X 217 mils
CONNECT SUBSTRATE TO GROUND

AT28C256 DIE PINOUT



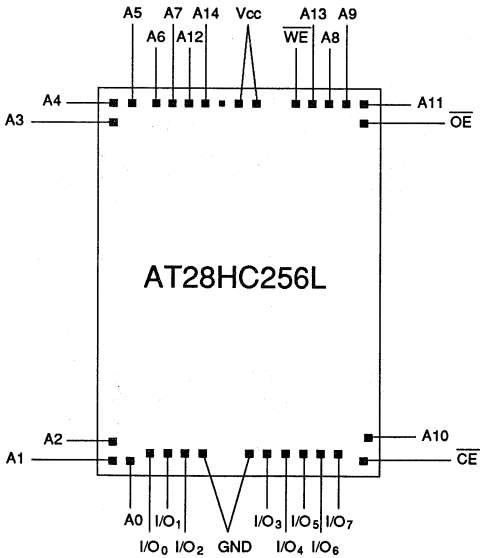
DIE SIZE: 224 X 323 mils
CONNECT SUBSTRATE TO GROUND

AT28HC64L DIE PINOUT



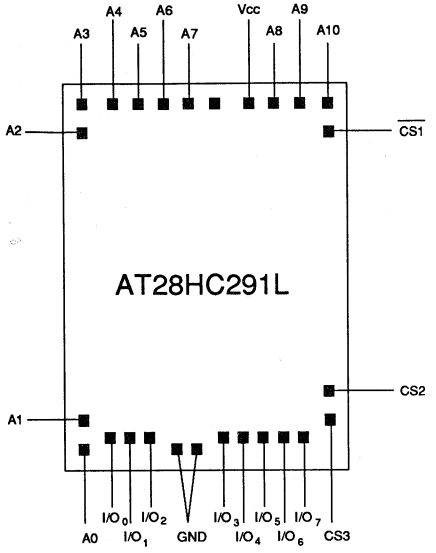
DIE SIZE: 146 X 217 mils
CONNECT SUBSTRATE TO GROUND

AT28HC256L DIE PINOUT



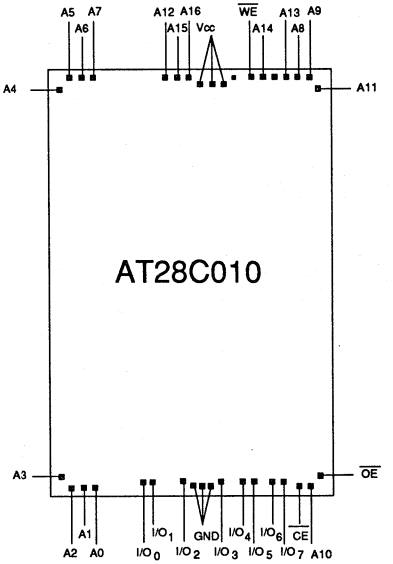
DIE SIZE: 224 X 323 mils
CONNECT SUBSTRATE TO GROUND

AT28HC291L DIE PINOUT



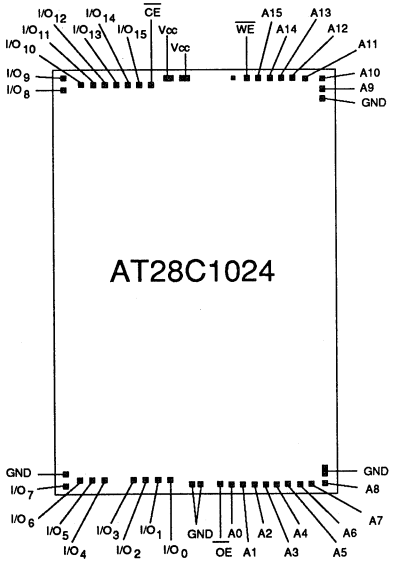
DIE SIZE: 118 X 144 mils
CONNECT SUBSTRATE TO GROUND

AT28C010 DIE PINOUT



DIE SIZE: 356 X 429 mils
CONNECT SUBSTRATE TO GROUND

AT28C1024 DIE PINOUT



DIE SIZE: 315 x 464 mils
CONNECT SUBSTRATE TO GROUND

Contents

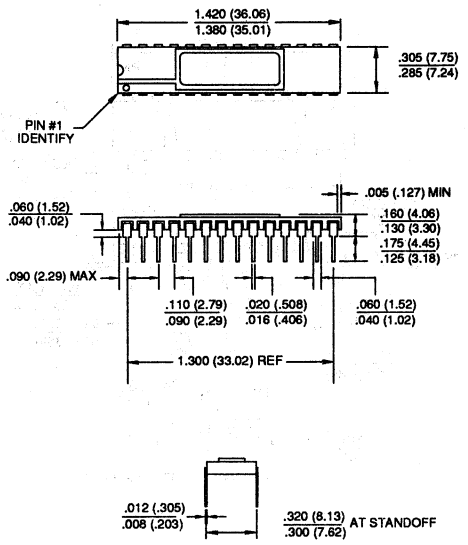
Each Atmel Data Sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.

Standard Package Outlines

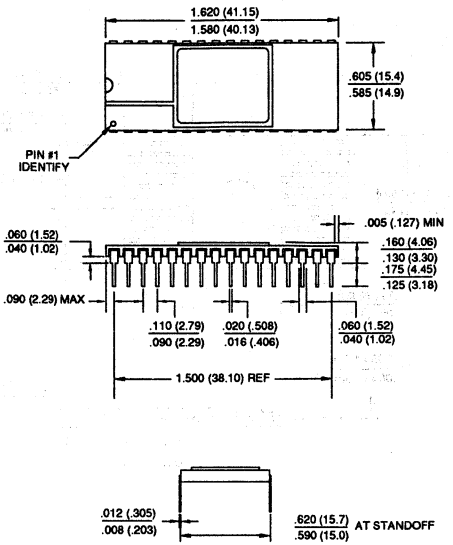
Package *Description*

Continued on next page

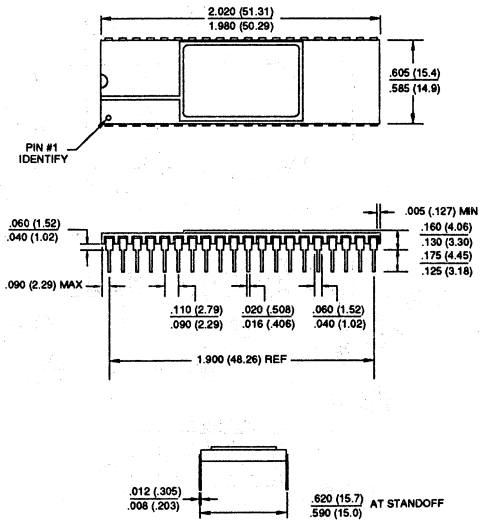
28B, 28 Lead, 0.300" Wide, Ceramic Side Braze
Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-M 38510 D-15 CONFIG 3



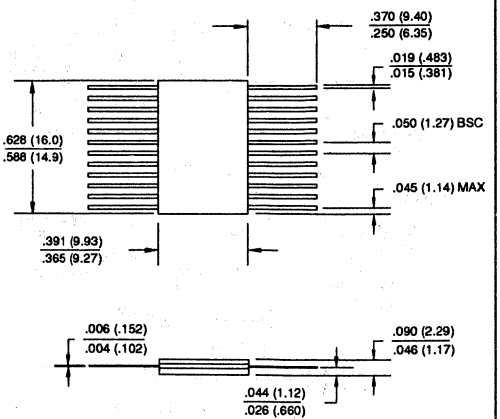
32B, 32 Lead, 0.600" Wide, Ceramic Side Braze
Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-M-38510 CONFIG 3



40B, 40 Lead, 0.600" Wide, Ceramic Side Braze
Dual Inline (Side Braze)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-5 CONFIG 3



24C, 24 Lead, Non-Windowed,
Ceramic Flat Package (Cerpack)
Dimensions in Inches and (Millimeters)
MIL-M-38510 F-6 CONFIG 1
JEDEC OUTLINE MO-019 AA



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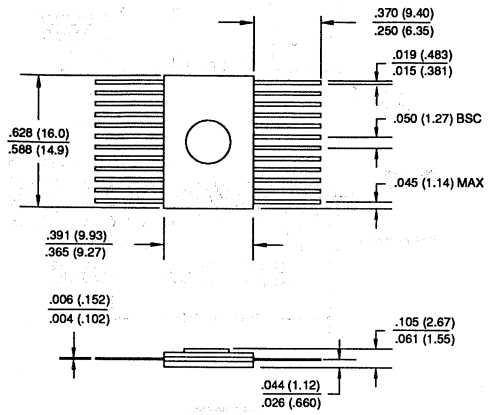
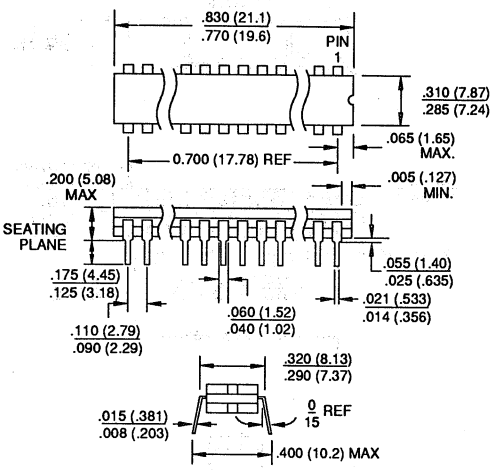
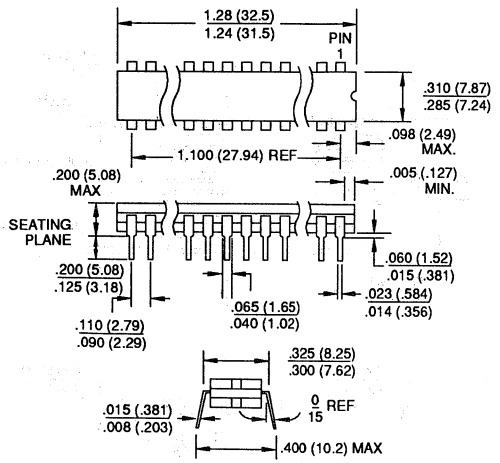
24CW, 24 Lead, Windowed,
Ceramic Flat Package (Cerpack)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-019 AA



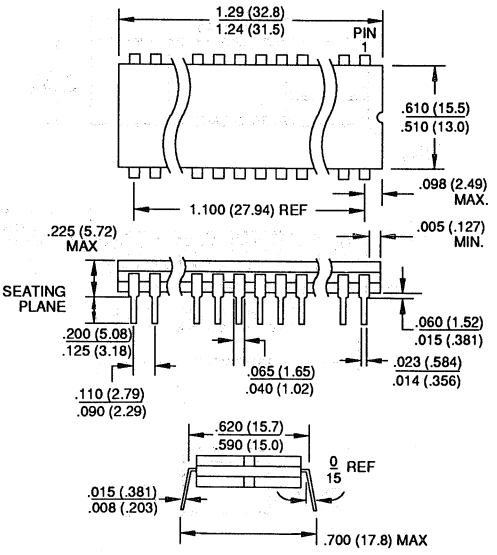
16D3, 16 Lead, 0.300" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-2 CONFIG 1



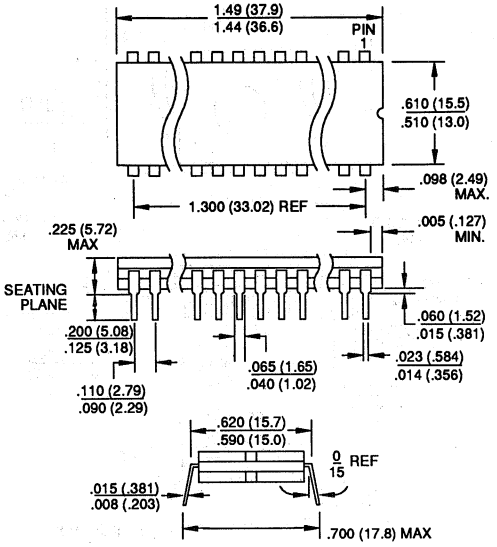
24D3, 24 Lead, 0.300" Wide, Non-Windowed
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-9 CONFIG 1



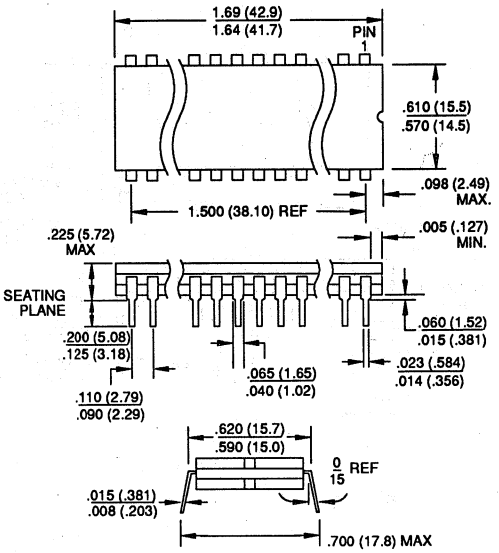
24D6, 24 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-3 CONFIG 1



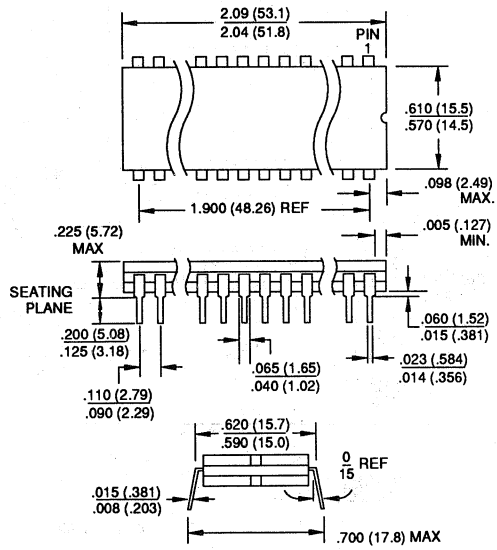
28D6, 28 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-10 CONFIG 1



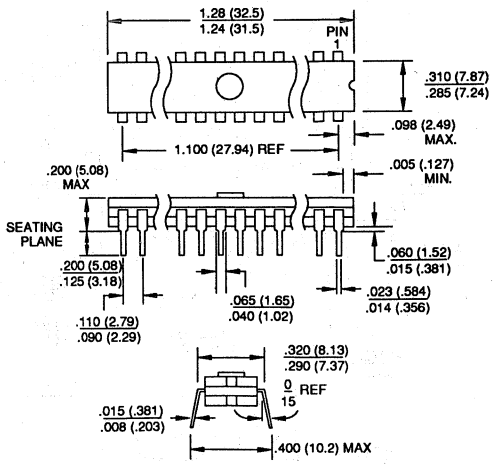
32D6, 32 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)



40D6, 40 Lead, 0.600" Wide, Non-Windowed,
Cermic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-5 CONFIG 1



24DW3, 24 Lead, 0.300" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-9 CONFIG 1



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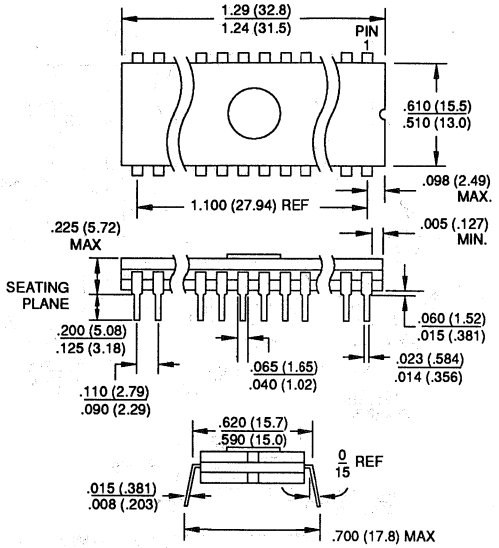
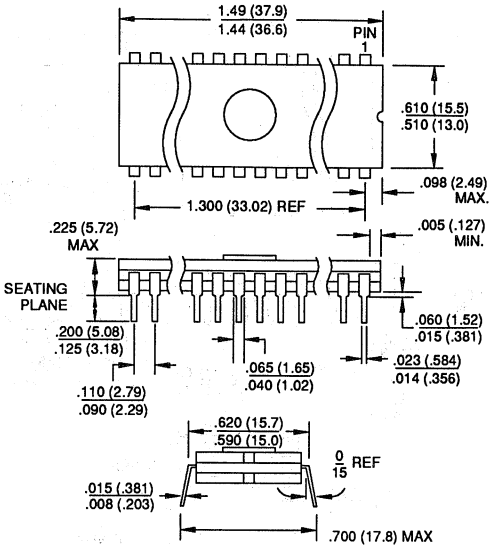
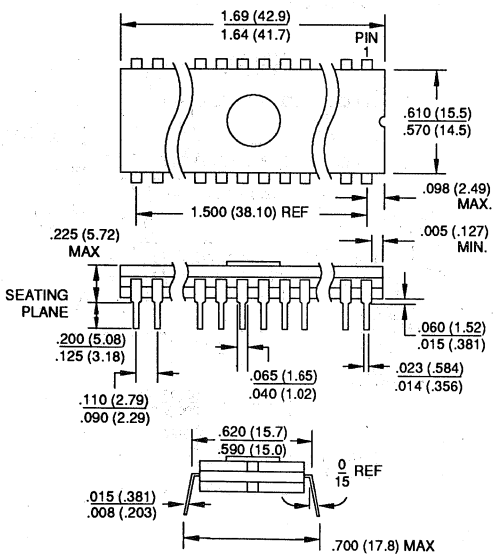
24DW6, 24 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-3 CONFIG 1



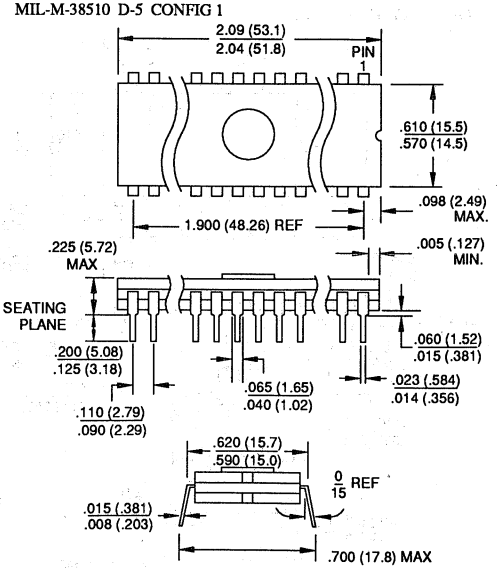
28DW6, 28 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-10 CONFIG 1



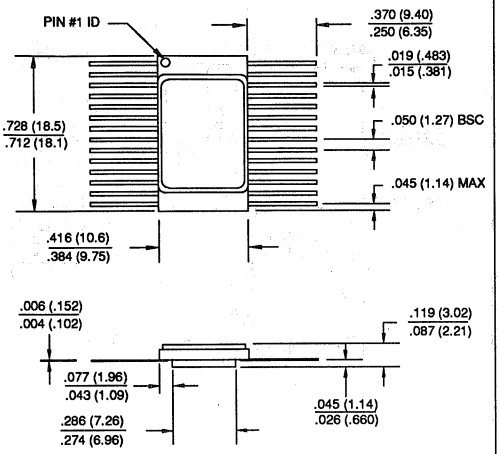
32DW6, 32 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)



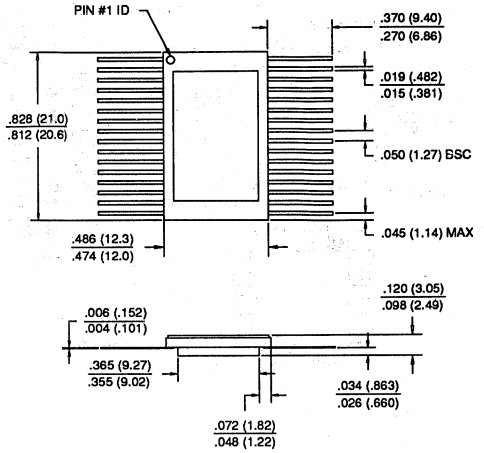
40DW6, 40 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-M-38510 D-5 CONFIG 1



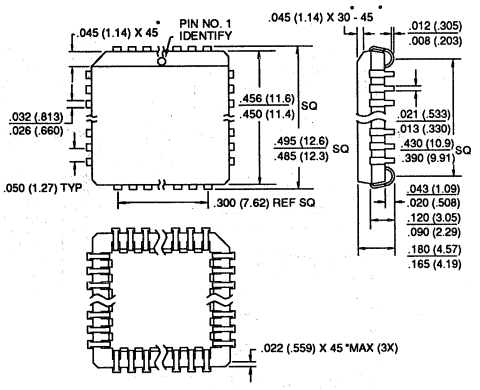
28F, 28 Lead, Non-Windowed,
Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
MIL-M-38510 F-12 CONFIG 2



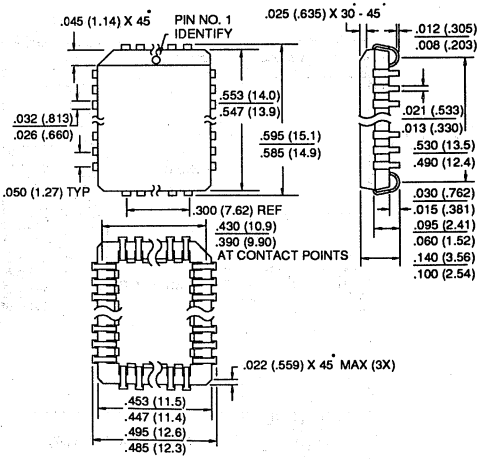
32F, 32 Lead, Non-Windowed,
Ceramic Bottom-Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-115



28J, 28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-047 AB



32J, 32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-052 AE



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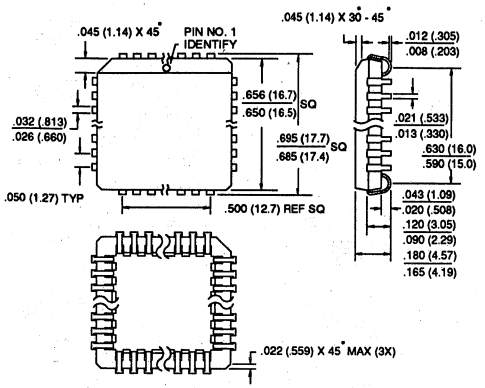
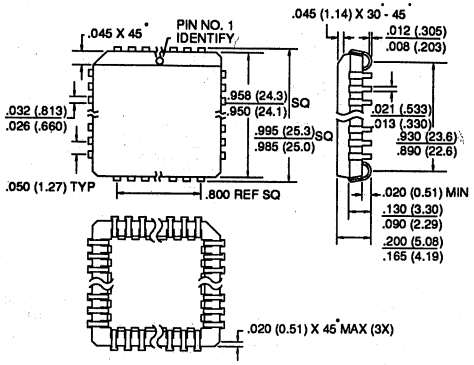
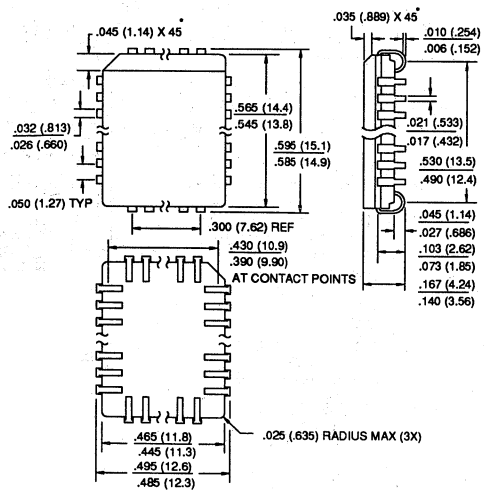
44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AC



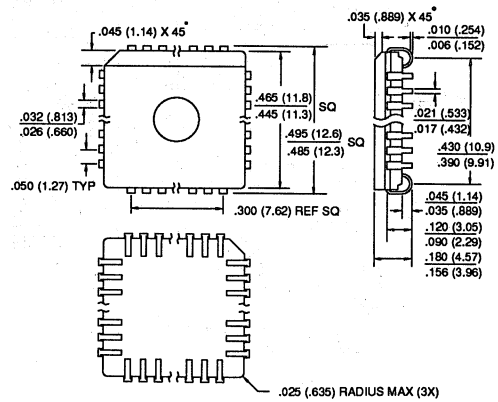
68J, 68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AE



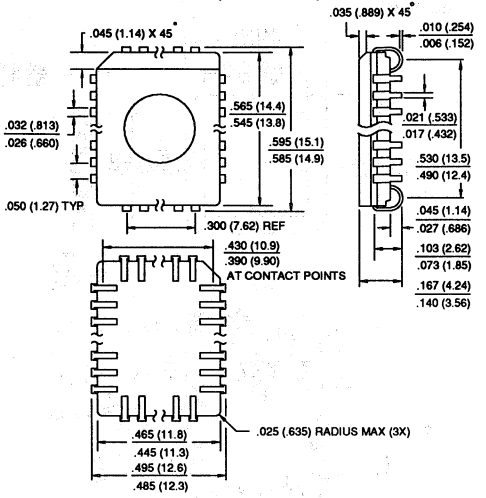
32K, 32 Lead, Non-Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)



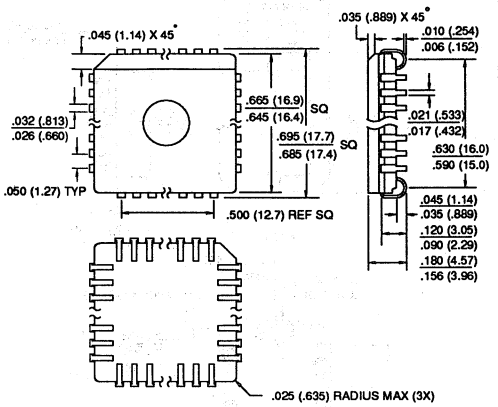
28KW, 28 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)



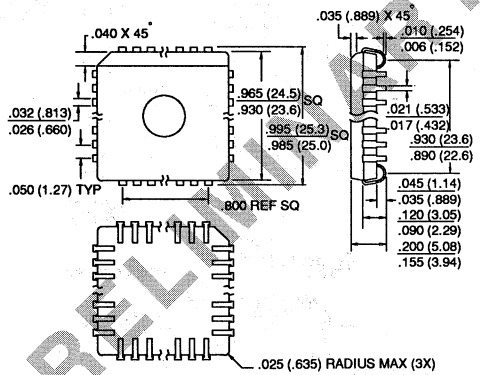
32KW, 32 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)



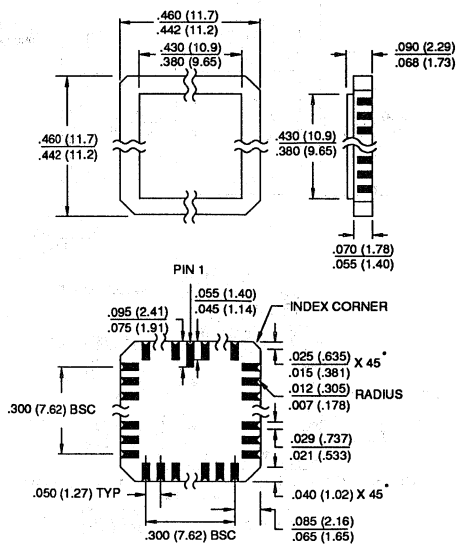
44KW, 44 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)



68KW, 68 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)

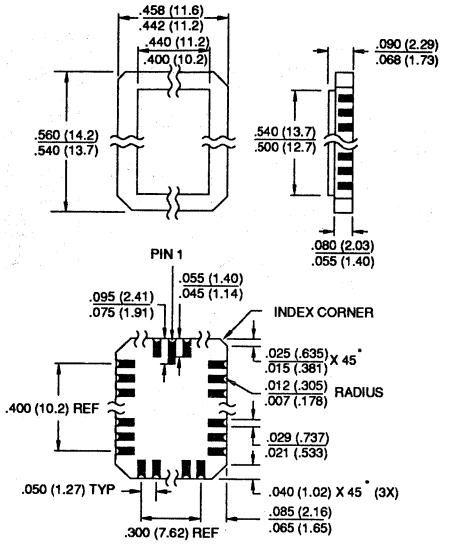


28L, 28 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-4

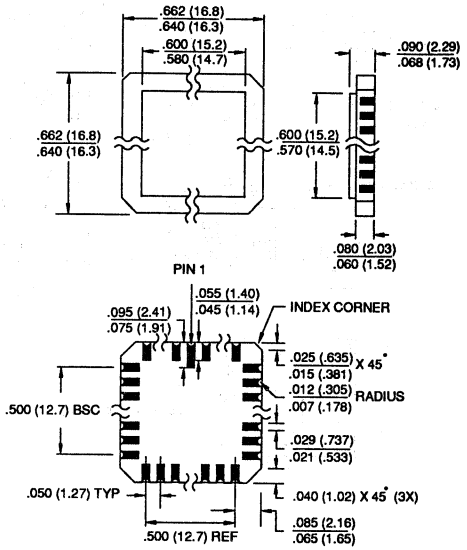


16

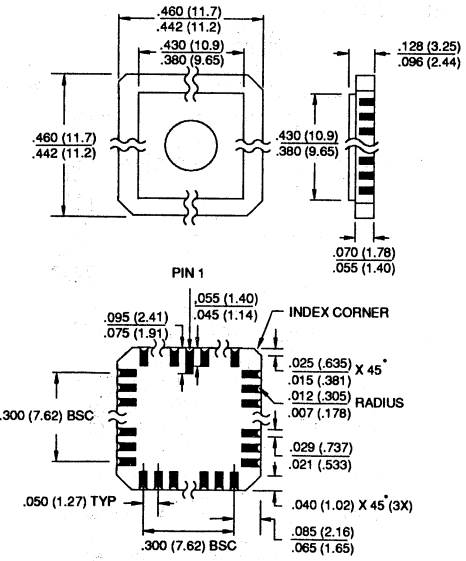
32L, 32 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-12



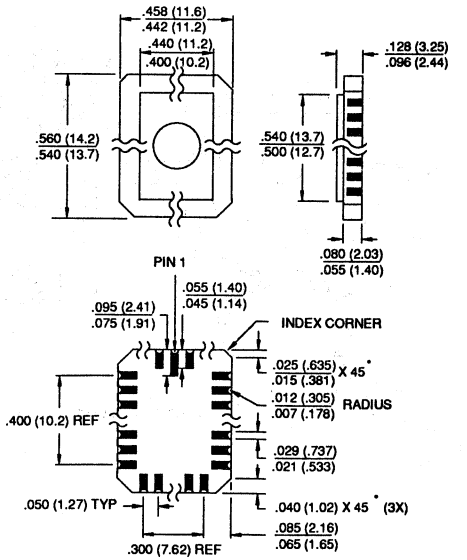
44L, 44 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)
MIL-M-38510 C-5



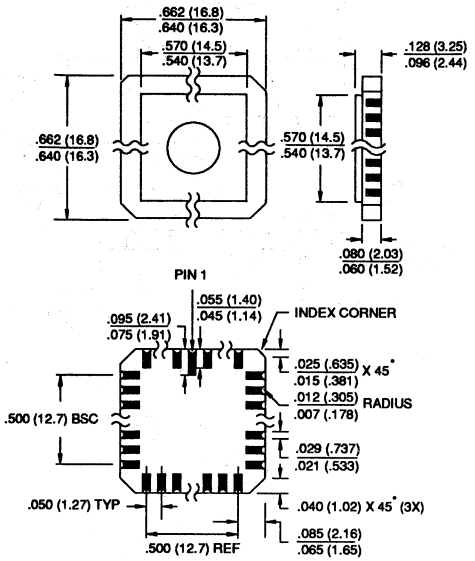
28LW, 28 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)



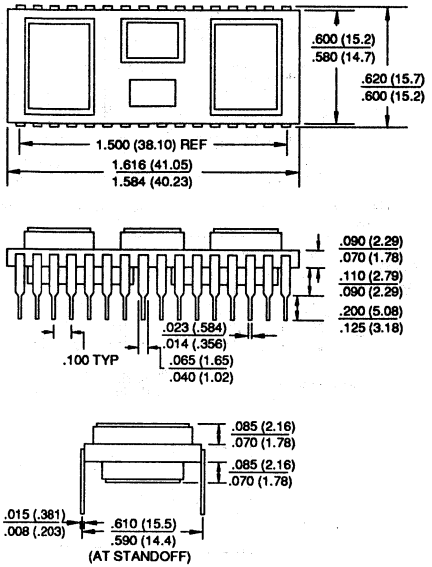
32LW, 32 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)



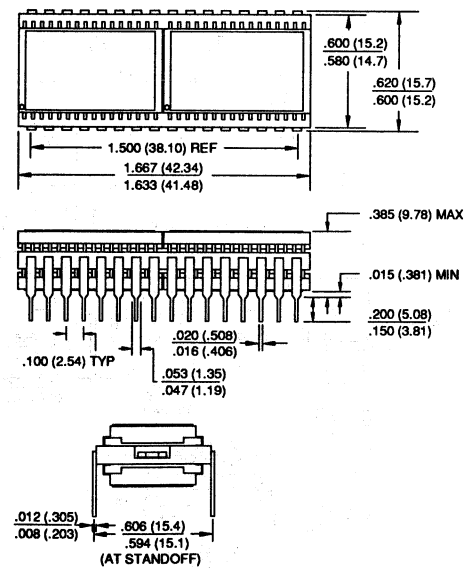
44LW, 44 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)



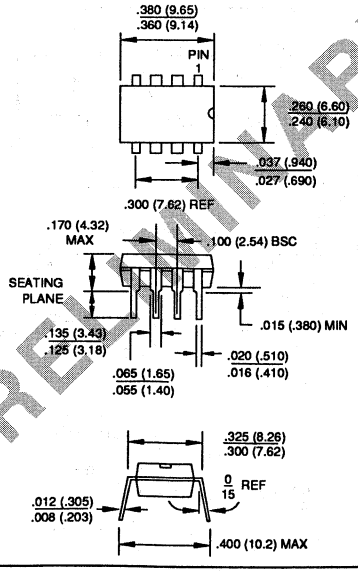
32M1, 32 Lead, Non-Windowed, Ceramic Dual Inline
32D6 Compatible LCC Module (Module)
Dimensions in Inches and (Millimeters)



32M2, 32 Lead, Non-Windowed, Ceramic Dual Inline
32D6 Compatible Flatpack Module (Module)
Dimensions in Inches and (Millimeters)

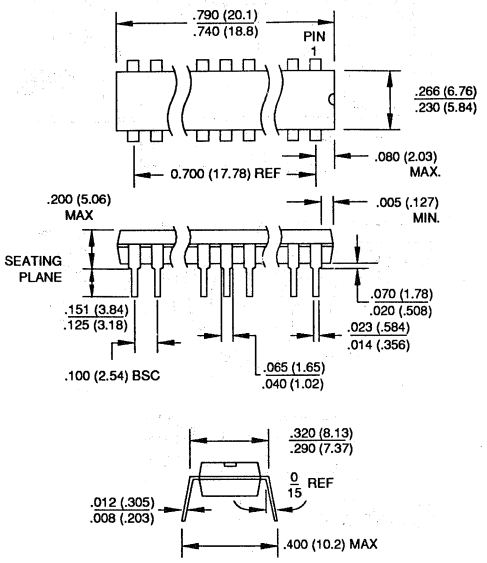


8P3, 8 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

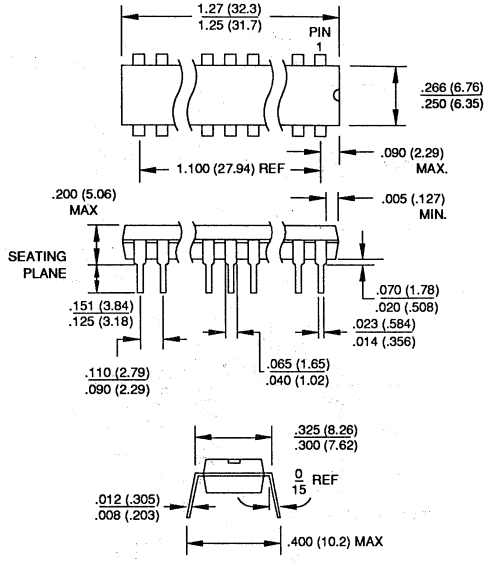


16

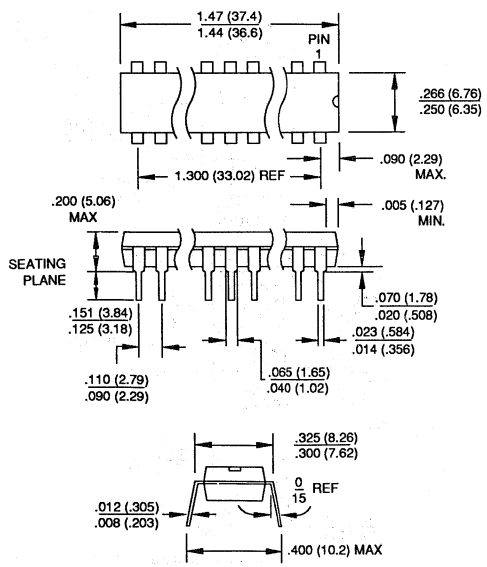
16P3, 16 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



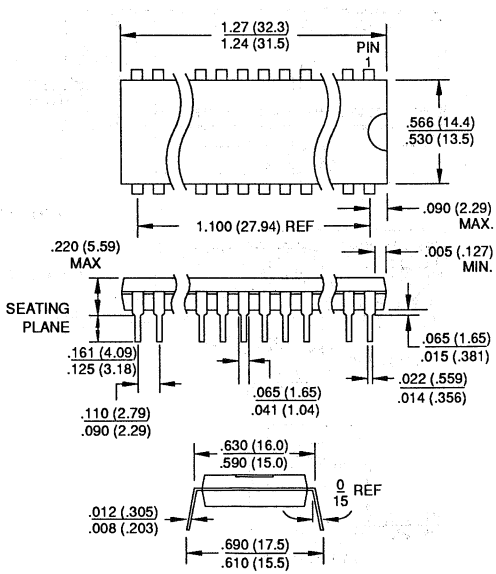
24P3, 24 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



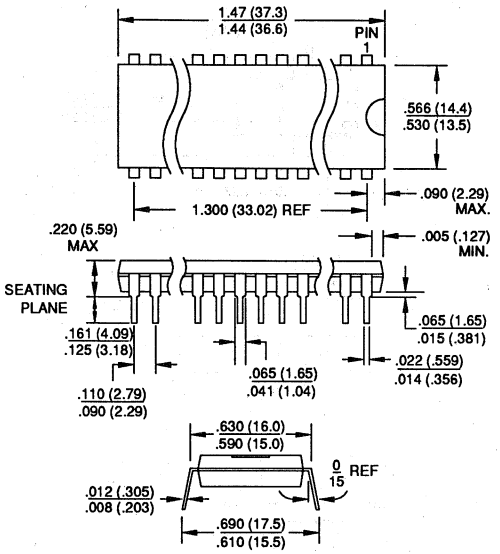
28P3, 28 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



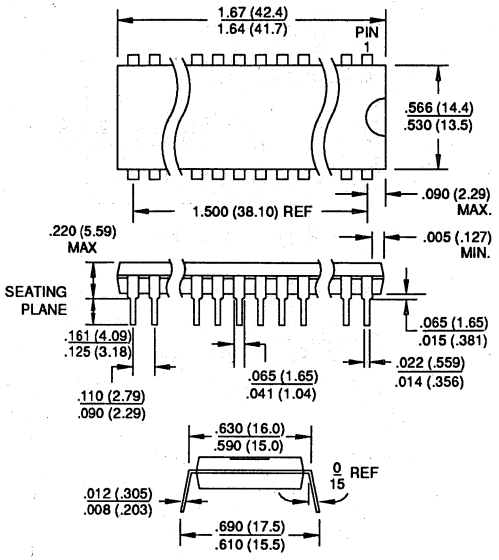
24P6, 24 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



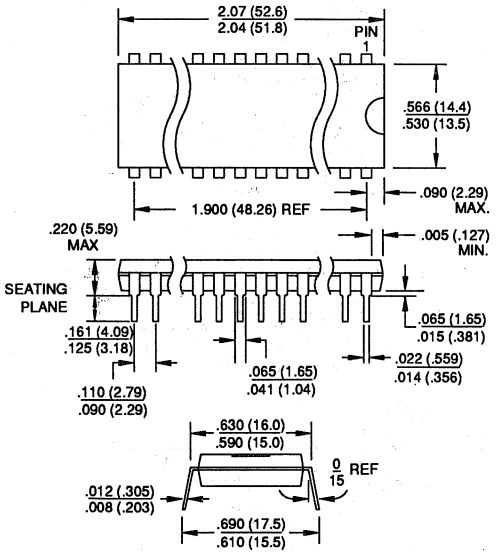
28P6, 28 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



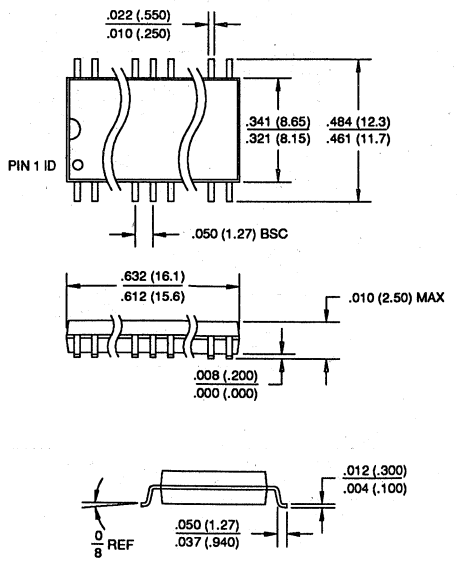
32P6, 32 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



40P6, 40 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



24R, 24 Lead, 0.330" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



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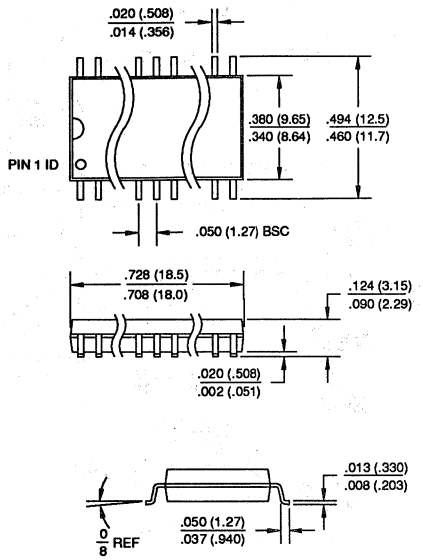
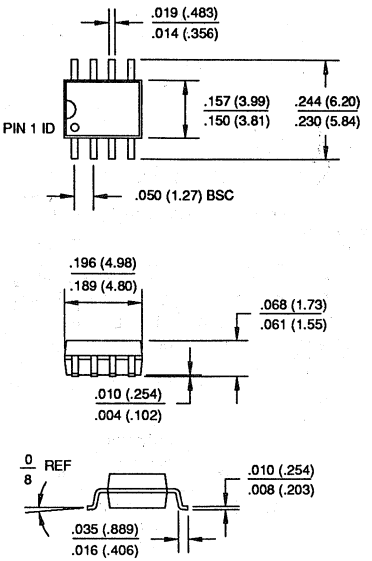
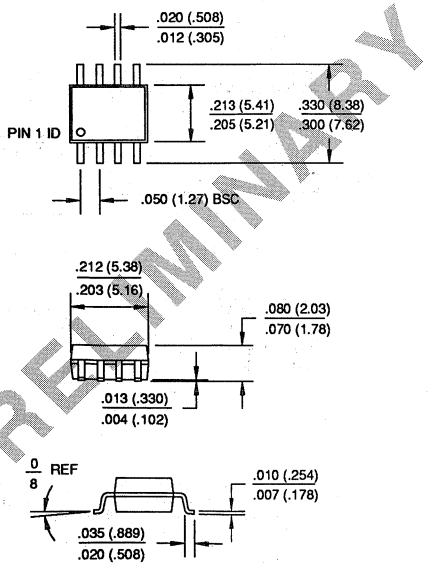
28R, 28 Lead, 0.330" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



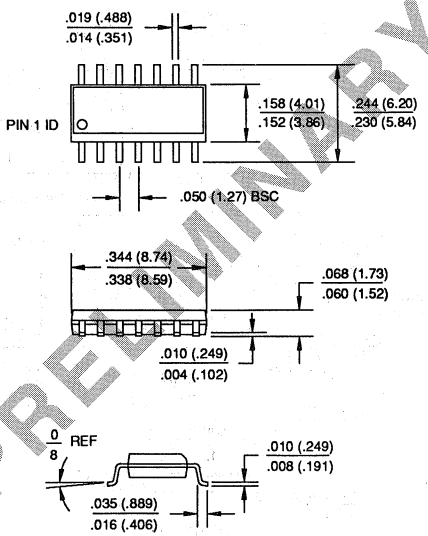
8S1, 8 Lead, 0.150" Wide,
Plastic Gull Wing Small Outline (JEDEC SOIC)
Dimensions in Inches and (Millimeters)



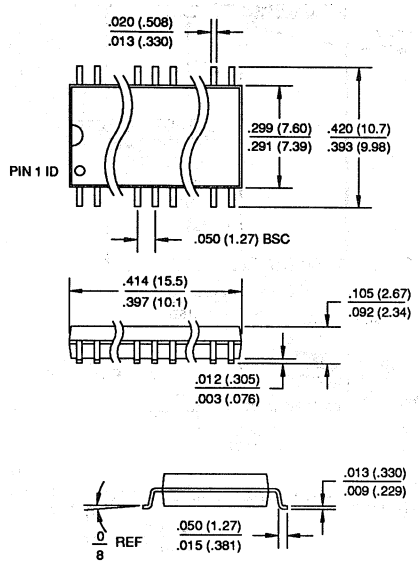
8S2, 8 Lead, 0.200" Wide,
Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)



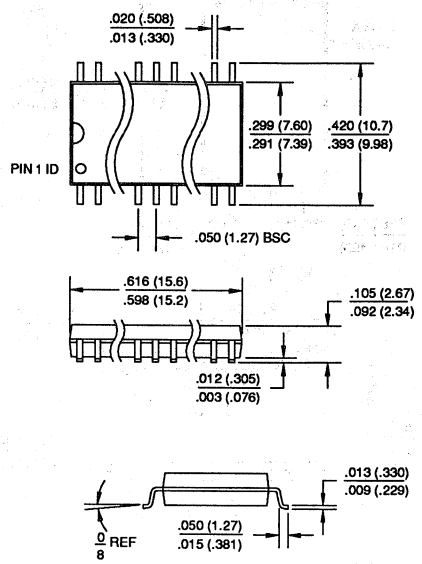
14S, 14 Lead, 0.150" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



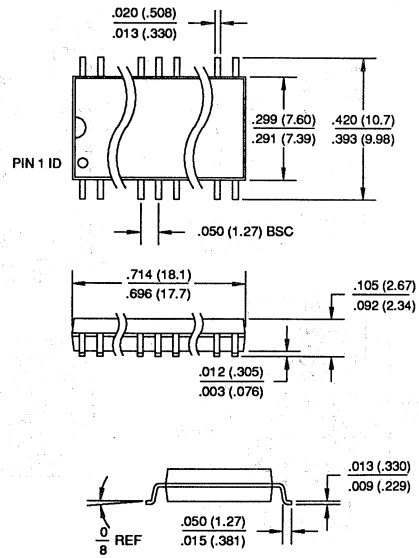
16S, 16 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



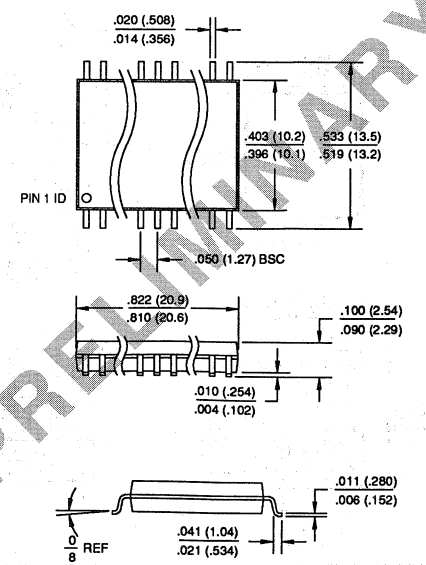
24S, 24 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



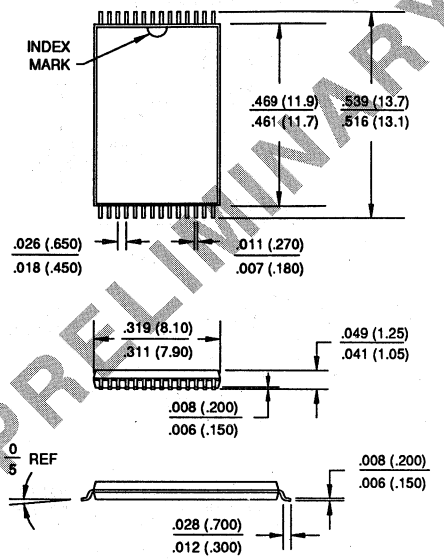
28S, 28 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



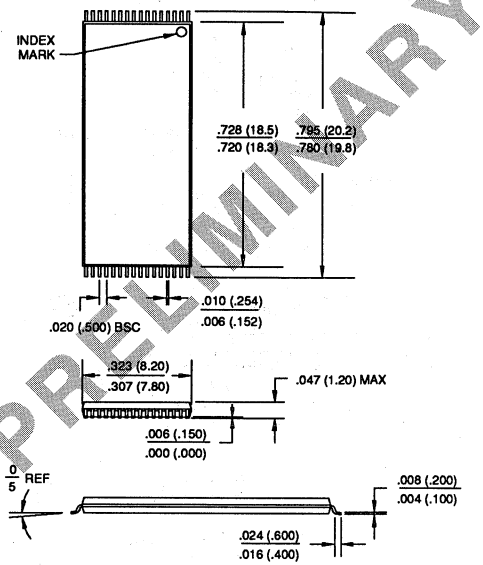
32S, 32 Lead, 0.450" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



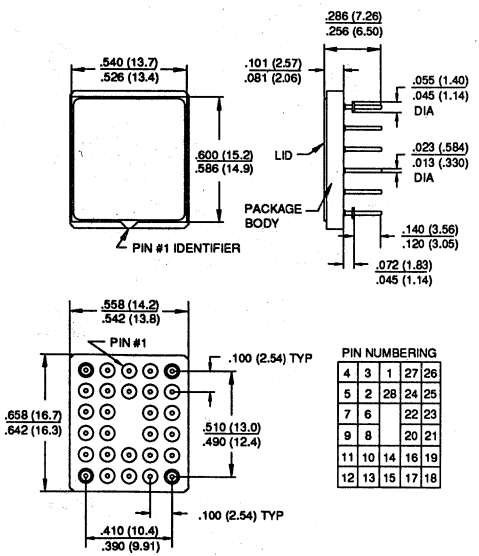
28T, 28 Lead, Thin Small Outline Package (TSOP)
Dimensions in Inches and (Millimeters)



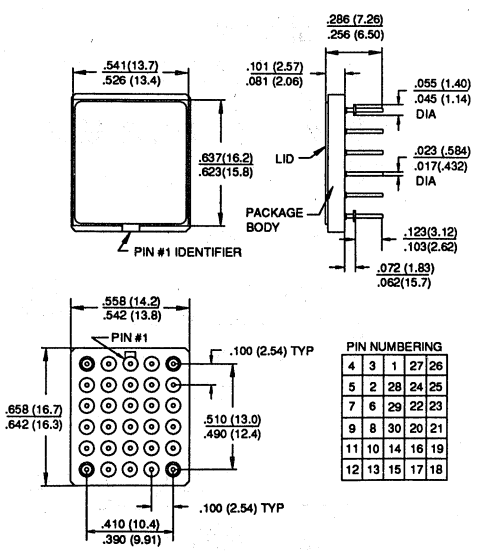
32T, 32 Lead, Thin Small Outline Package (TSOP)
Dimensions in Inches and (Millimeters)



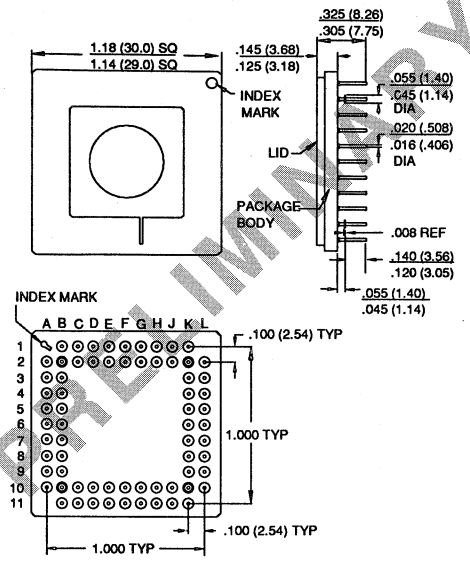
28U, 28 Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



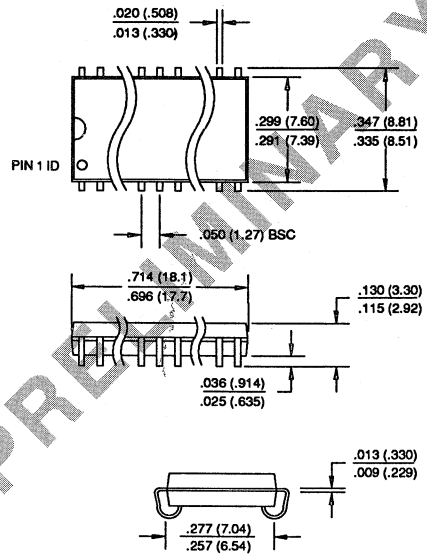
30U, 30 Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



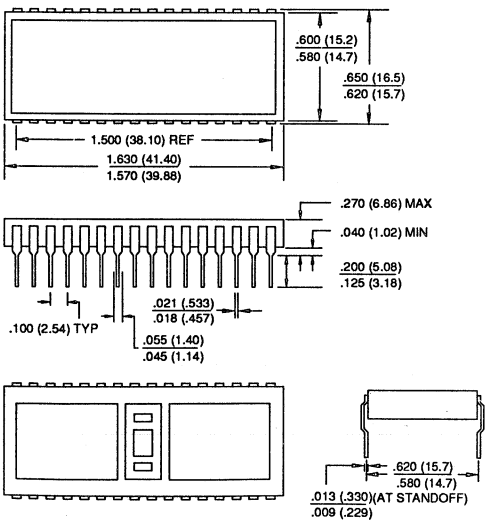
68UW, 68 Pin, Windowed, Ceramic
Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



28X, 28 Lead, 0.300" Wide,
Plastic J-Leaded Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



32Z, 32 Lead, Non-Windowed, Ceramic Dual Inline
32D6 Compatible Multi-Chip Module (MCM)
Dimensions in Inches and (Millimeters)



16

Thermal Characteristics of Atmel Packages

The thermal performance of the semiconductor package is a very important consideration for the board designer. The reliability and functional life of the device is directly related to its junction operating temperature. As the temperature of the device increases, the stability of its junctions decline, as does its reliable life. The thermal performance is also important to the board design, because it may limit the board density, or dictate the board location of high power-dissipating devices, or require expensive cooling methods for the system. As devices have become more complex and boards have become denser, the need to account for the thermal characteristics of packages have shifted from being a minor consideration to being a necessary consideration.

The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has a corresponding "resistance" to the heat flow, which is given the value θ, the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are θ_{JA} (junction to ambient air), θ_{JC} (junction to package case), and θ_{CA} (case to ambient air).

An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation,

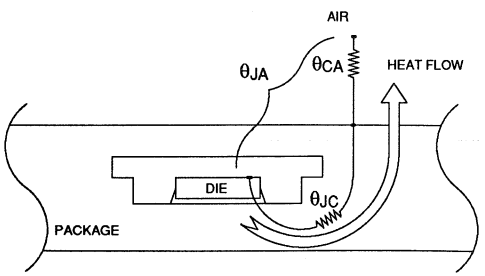
$$Tj - Ta = P \times \theta_{JA}$$

where,

P = Device operating power [watts]
Tj = Temperature of a junction on the device [°C]
Ta = Temperature of the surrounding ambient air [°C]

Two conclusions can be made after examining this analogy. First, the lower the value of θ_{JA}, the better the heat dissipation of the package. Secondly, the value of θ_{JA} is directly dependent upon both the conductive (θ_{JC}) and convective (θ_{CA}) properties of the package. θ_{JC} is a function of the package material, the adhesion between the package materials, and device size. θ_{CA} is a function of the package size and configuration, package mounting method, and air flow across the package. Lower θ_{JA} values can be achieved by specifying ceramic packages instead of plastic packages, choosing larger packages, or improving air flow across the package.

The thermal resistance values of Atmel standard packages are listed on the following page. The figures shown are maximum values for θ, typical values are lower dependent upon the device type.



Thermal Resistance Coefficients

		θ_{JC} [°C/W]	θ_{JA} [°C/W]		
			Airflow=0 ft/min	Airflow=100 ft/min	Airflow=500 ft/min
Ceramic DIP	24D3/DW3	9	65	50	35
	24D6/DW6	10-15	45	35	20
	28D6/DW6	10-15	45	35	30
	32D6/DW6	10	45	35	30
	40D6/DW6	7	40	30	25
Plastic DIP	24P3	22	82	72	60
	24P6	39	82	72	60
	28P6	36	77	68	56
	32P6	34	72	64	53
	40P6	30	68	60	49
Leadless Chip Carrier	28L/LW	12	68	56	48
	32L/LW	10	65	55	47
	44L/LW	4	60	49	40
Plastic Leaded Chip Carrier	28J	16	60	50	40
	32J	16	60	50	40
	44J	14	50	44	35
JLCC	28K/KW	16	72	64	53
	32K/KW	16	72	64	53
	44K/KW	16	68	60	49
Cerpack	24C/CW	15	81	72	63

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Pittsford, NY 11534
(716) 381-9700

New York (cont'd)

Nu Horizons
6000 New Horizons Blvd.
Amityville, NY 11701
(516) 226-6000

100 Bluff Drive
E. Rochester, NY 14445
(716) 248-5980

Phase I Technology
1110 Route 109
N. Lindenhurst, NY 11757
(516) 957-4900

Time Electronics
415 Oser Avenue
Hauppauge, NY 11788
(516) 434-3344

Time Electronics
6311 Fly Road
Suite C
East Syracuse, NY 13057
(315) 432-0355

Time Electronic Sales
70 Marcus Boulevard
Hauppauge, NY 11788
(516) 273-0100

North Carolina

Milgray/Raleigh
2925 Huntleigh Drive
Suite 101
Raleigh, NC 27604-3374
(919) 790-8094

Time Electronics
9800 L Southern Pine Blvd
Charlotte, NC 28217
(800) 824-6598

Ohio

Bell Industries
Dayton Industrial
444 Windsor Park Drive
Dayton, OH 45459
(513) 435-8660

Dayton Military
446 Windsor Park Drive
Dayton, OH 45459
(513) 434-8231

Milgray/Cleveland
6155 Rockside Road
Suite 206
Cleveland, OH 44131
(216) 447-1520

Time Electronics
2580 Oakstone Drive
Suite A
Columbus, OH 43231
(614) 794-3301

Oregon

Bell Industries
6024 Southwest Jean Rd.
Lake Oswego, OR 97035
(503) 635-6500

Time Electronics
15688 S.W. 72nd Avenue
Portland, OR 97224
(503) 684-3782

Western Micro Technologies Inc.
1800 N.W. 169th Place
Suite B300
Beaverton, OR 97006
(503) 629-2082

Domestic Distributors, cont'd

Texas

All American
1819 Firman Dr. #127
Richardson, TX 75081
(214) 231-5300

Bell Industries
1701 Greenville Avenue #306
Richardson, TX 75081
(214) 690-0466

Insight Electronics Inc.
1778 Plano Rd.
Suite 320
Richardson, TX 75081
(214) 783-0800

12703 A Research Blvd.
Suite 1
Austin, TX 78759
(512) 335-3707

Milgray/Dallas
16610 North Dallas Parkway
Suite 1300
Dallas, TX 75248
(214) 248-1603

Milgray/Houston
12919 Southwest Freeway
Suite 130
Stafford, TX 77477
(713) 240-5360

Omni-Pro Electronics
4141 Billy Mitchell
Dallas, TX 75244
(214) 233-0500

7719 Wood Hollow Drive
Suite 210
Austin, TX 78731
(512) 794-9200

Texas (cont'd)

Time Electronics
1876 Firman Drive
Richardson, TX 75081
(214) 644-4644

9300 Jollyville Road #100
Austin, TX 78759
(512) 339-3054

10250 Bissonette #330
Houston, Texas 77036
(713) 530-0800

Utah

Added Value
1836 West Parkway Blvd.
Salt Lake City, UT 84119
(801) 975-9500

Bell Industries
6912 South 185 West
Suite B
Midvale, UT 84047
(801) 255-9611

Milgray
310 E. 4500 South
Suite 111
Murray, UT 84107
(801) 261-4999

Time Electronics
2446 Progress Drive
West Valley, UT 84119
(801) 973-8494

Washington

Bell Industries
16650 N.E. 79th St.
Suite 103
Redmond, WA 98052
(206) 867-5410

Insight Electronics
12002 115th Ave. N.E.
Kirkland, WA 98034
(206) 820-8100

Western Micro Technologies, Inc.
14636 N.E. 95th Street
Redmond, WA 98052
(206) 881-6737

Time Electronics
8601 Willows Road
Redmond, WA 98052
(206) 882-1600

Wisconsin

Bell Industries
W. 226 N. 900 Eastmound Ave.
Waukesha, WI 53186
(414) 547-8879

Domestic Distributors, cont'd

Canada

Milgray/Toronto
150 Consumer Road
Suite 502
Willowdale, Ontario M2J 1P9
Tel. (416) 756-4481
Fax. (416) 756-2598

ITT Multicomponents
300 North Rivermede Road
Concord, Ontario L4K 2Z4
Tel. (416) 736-1144
Fax. (416) 736-4831

Suite 506 Bell Mews
39 Robertson Road
Nepean, Ontario K2H 8R2
Tel. (613) 596-6980
Fax. (613) 596-6987

5713 Chemin St. Francois
St. Laurent, Quebec H4S 1W9
Tel. (514) 335-7697
Fax. (514) 335-9330

3455 Gardner Court
Burnaby, B.C., V5G 4J7
Tel. (604) 291-8866
Fax: (604) 291-1227

#3 9840 47th Avenue
Edmonton, Alberta T6E 5P3
Tel. (403) 436-9555
Fax. (403) 438-4983

#210, 3015-5th Ave. N.E.
Calgary, Alberta T2A 6T8
Tel. (403) 273-2780
Fax. (403) 273-7458

760 Century Street
Winnipeg, Manitoba R3H 0M1
Tel. (204) 786-8401
Fax. (204) 889-5357

Time Electronics
6291 Dornan Road
Unit #5 Building 301
Mississauga, Ontario L4T 4E8
Tel. (416) 601-4368

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Fax. 719-540-1759

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Hanover, MD 21076
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Fax. 301-796-0117

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Dallas, TX 75252
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